Intel® Acceleration Stack for Intel® Xeon® CPU with FPGAs Version 1.3.1 Release Notes

Intel FPGA Programmable Acceleration Card N3000-N

Updated for Intel® Acceleration Stack for Intel® Xeon® CPU with FPGAs: **1.3.1**

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Notice

Please note that the Intel® Acceleration Stack for Intel Xeon® CPU with FPGAs **DOES NOT** include mitigations for the exploits known as Spectre (CVE-2017-5753, CVE-2017-5715) and Meltdown (CVE-2017-5754). These exploits require that malware runs locally on the system, which is not normally possible in a closed environment where the system's software is centrally controlled. Intel does not recommend that an un-mitigated version of the Intel Acceleration Stack for Intel Xeon CPU with FPGAs be used in an environment that is not a closed system environment.

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Intel Acceleration Stack for Intel Xeon CPU with FPGAs Version 1.3.1 Release Notes

This document provides up-to-date information about the Intel Acceleration Stack for Intel Xeon CPU with FPGAs version 1.3.1 for the Intel FPGA Programmable Acceleration Card N3000-N.

Note: The Intel Acceleration Stack v1.3.1 is built upon v1.3 with the following additions:

- Extended support to RedHat 8.2 kernel 4.18
- Improved OPAE FPGA Driver
- PACSign Tool support to newer OpenSSL library

Minimum Requirements

The minimum requirements for the Intel FPGA PAC N3000-N must include:

- Intel Xeon Scalable processor
- A PCI Express* x16 Slot
- 48 GB of free memory (Intel Quartus® Prime Pro Edition software requires at least 48 GB for compiling a design targeting an Intel Arria® 10 FPGA device)
- Operating System:
  - CentOS Linux* version 7.6 kernel 4.19
  - Red Hat Enterprise Linux (RHEL*) version 8.2 kernel 4.18
- OPAE Software Stack requires Python 3
- PACsign requires Python 3.6

Supported Features

Table 1. Features of the Intel Acceleration Stack v1.3.1 for Intel FPGA PAC N3000-N

Feature	Description
OPAE	• FPGA enumeration • FME device access • AFU device access • FPGA memory-mapped I/O (MMIO) register access • Access Intel MAX® 10 board management controller (BMC) over SPI bus • A bitstreaminfo tool that displays authentication information for `*.bin` files. • Voltage and power monitoring through OPAE commands • Memory test over DMA

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Feature	Description
	• Network loopback (NLB) test • Graceful shutdown support using the `fpgad` tool • OPAE software RPMs for use with yum install
Runtime and Development Installers	Enables easy installation of the release package for Intel FPGA PAC N3000-N
Security	• Intel MAX 10 Root-of-Trust Implementation • Support for Intel MAX 10 BMC firmware, Intel MAX 10 FPGA images and FPGA static region user image signing • OPAE security tools: — FPGA secure update (`fpgasupdate`): Remotely updates bitstreams securely. — PACSign: Enables signing of bitstreams. To use this tool, you must have the capability to generate a public/private key pair and your hardware security module (HSM) must support a Public-Key Cryptography Standards (PKCS)#11 compatible application programming interface (API) to the PACSign tool. — `fpgainfo security` command identifies root entry hashes, BMC and user image update counter values and cancelled CSK IDs.
Extended Operating Range	Platform and telemetry support for applications requiring Telcordia Network Equipment-Building System (NEBS) compliance. • Board component temperature ratings reviewed and updated • Improved heatsink • Board Management Controller (BMC) board temperature thresholds modified: — Upper warning threshold now 85°C — Upper fatal threshold now 100°C

Intel FPGA PAC N3000-N Reference Table

The following table provides key firmware (FW) versions for this release. To identify the current firmware version in your Intel FPGA PAC N3000-N, use the OPAE command: `fpgainfo fme`.

Note: Only install OPAE tools and drivers that correspond to your specific software package.

Table 2. Intel FPGA PAC N3000-N FPGA Flash User and Factory Partition

Production boards come with an FPGA flash programmed with Intel-provided manufacturing test images in the user and factory partition. You must flash the card with your own user image.

FPGA Flash	Configuration	Bitstream ID
User Partition	4x25 GbE	0x23000110010310
Factory Partition	2x2x25 GbE	0x23000410010310

Table 3. Intel FPGA PAC N3000-N Board Management Controller Firmware and RTL Reference Table

Intel Acceleration Stack Version	Intel MAX 10 Nios® FW	Intel MAX 10 Build
1.3.1	D.2.1.24	D.2.0.7

Note: Non-production (ES) Intel FPGA PAC N3000-N is shipped with Intel MAX 10 Nios firmware and Intel MAX 10 RTL build version D.2.0.21 and D.2.0.6 respectively. Between ES and Production versions, two MAX10 BMC updates have been released, D.2.1.23/D.2.0.7 and 2.1.24/D.2.0.7. These Intel MAX 10 BMC updates are available on the Intel Resource and Design Center. Contact your Intel support representative to access these updates.

Known Issues

Table 4. Known Issues in Intel Acceleration Stack v1.3.1 for Intel FPGA PAC N3000-N

Known Issue	Details
DDR4 accesses with a burstcount of 64 are not supported.	• Burstcounts of 1, 2, 4, 8, 16 and 32 are supported. • Workaround: None. • Status: No planned fix.
Intel provided factory FPGA images may incur packet loss in FPGA when all ports are active and the packet size is not a multiple of 64.	• The provided FPGA factory images are intended to demonstrate all interfaces. The internal clock rate is not set for dropless packet transfer for all packet sizes. For more details on expected packet drop measurements for the baseline images, refer to Intel Provided FPGA Factory Image Packet Drop on page 12. • Workaround: While using an aggregated internal packet bus for your Intel FPGA PAC N3000-N design, set the clock rate to 285 MHz to have no packet drops for all packet sizes. The disaggregated and lightweight packet bus implementation options do not have this issue. • Status: No planned fix.
`fpgainfo bmc` may not return QSFP Supply Voltage if your QSFP module does not support supply voltage and temperature registers.	• The Intel MAX 10 BMC obtains the QSFP module voltage sensor value from the Supply Voltage registers beginning at offset 26, as listed in the Free Side Monitoring Values, Table 6-7, of the SFF-8636 Specification for Management Interface for 4-lane Modules and Cables, rev 2.10a. If the QSA cable is used, it should comply with SFF-8472 standard. • Workaround: If your QSFP module does not support this register, please disregard the value returned by the Intel MAX 10 BMC when using the `fpgainfo bmc` command. • Status: No planned fix.
The Intel MAX 10 BMC drops MCTP packets when SOM bit is 1 and Pkt_seq# is nonzero.	• The DSP0236 MCTP Base Specification states the that the packet sequence number can be any value 0-3 if the SOM bit is set. • Workaround: None. • Status: This limitation will be fixed in a future version of the Intel Acceleration Stack for the Intel FPGA PAC N3000-N.
The PLDM `GetPDRRepositoryInfo` command reports a constant `updateTime` field.	• When the `SetSensorThresholds` command is issued to update the threshold values, the `GetPDRRepositoryInfo` updateTime field does not update. Instead the updateTime field always reports July 4th 2018. • Workaround: None. • Status: No planned fix.
When using the `fpgastats` command, the Rx Broadcast OK counter (`CNTR_RX_BCAST_DATA_OK`) increments when oversized packets are received.	• According to the *IEEE 802.3 2018 Specification*, only the Rx Oversize Counter (`CNTR_RX_OVERSIZE`) increments when oversized packets are received. • Workaround: None. • Status: No planned fix.

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Known Issue	Details
Running the `fpgastats -B` command in a two card system results in inconsistent ordering of MAC wrapper information.	• When the `fpgastats -B <bus>` command is issued in a two card system, one card displays *MAC wrapper 1* first and the other card displays *MAC wrapper 0* first. In either case, the counter information is correct. • Workaround: None. • Status: This limitation will be fixed in a future version of the Intel Acceleration Stack for the Intel FPGA PAC N3000-N.
The PCIe link between the Broadcom* PEX8747 PCIe Switch and the Intel Ethernet Controller XL710 downgrades to Gen1 width=0.	• Include a check for the expected PCIe link speed and width between the PEX8747 PCIe Switch and the downstream Intel XL710. If one of the links reports Width x0, then apply the workaround. • Workaround: Issue the `rsu bmcimg <bdf>` command to power cycle the board. • Status: This limitation is fixed in NVM Update 8.10 (ETrackID = 0x8000a3e9) for PCIe Device 0D58.
During the server power-down process, PCIe errors may be reported between the PEX8747 PCIe ports and the downstream XL710 Ethernet Controllers. This issue has been observed during AC Power Cycle stress testing.	• The issue is intermittent with a very low probability of occurring. The issue is only observed during the power-down phase. During the power-up phase, these PCIe errors are not present. • After confirming the errors during server power-down, if the PCIe errors cannot be masked, then system should ignore these errors. • Workaround: None. • Status: No planned fix.

Component Information

Ensure you review the reference materials for the following Intel FPGA PAC N3000-N components.

Broadcom* PEX8747 PCIe* Switch

Intel performs PCIe* compliance testing for all Intel FPGA PAC N3000-N variations. The following PCIe compliance tests are known to start in an invalid state.

Note: None of the following PCIe compliance test failures affect the PCIe functionality or the Intel FPGA PAC functionality.

Table 5. PCIe Compliance Test Failures

PCIe Compliance Test	Test Failure Reference
TD_1_42_ACS Extended Cap Structure Test	-
TD_1_50 Slot Capabilities2, Control2, and Status2 Registers Test	-
TD_2_7_Link Speed Test (2.5, 5.0, 8.0)	Broadcom* PEX 8749/48/47/33/32/25/24/23/17/16/13/12 Errata Refer to ***1.32*** *PEX 87xx Downstream Port Incorrectly Sets Link Status Register's "Link Autonomous Bandwidth Status" Bit for any Successful Speed Change Event*.
TD_2_9 Software Requested Link Equalization Test (2.5, 5.0, 8.0)	Broadcom PEX 8749/48/47/33/32/25/24/23/17/16/13/12 Errata Refer to ***1.32*** *PEX 87xx Downstream Port Incorrectly Sets Link Status Register's "Link Autonomous Bandwidth Status" Bit for any Successful Speed Change Event*.
Preset Configuration Test	Broadcom PEX 8749/48/47/33/32/25/24/23/17/16/13/12 Errata Refer to ***1.19*** *PEX 87xx Port Does Not Reject Illegal Coefficients for the Specified Condition*.
Gen 1 Rx Test	-

Related Information

- PCI*Express Architecture Configuration Space Test Specification Revision 3.0
  For more information about specific PCIe compliance tests.
- PCI*Express Architecture Link Layer and Transaction Layer Test Specification Revision 3.0
  For more information about specific PCIe compliance tests.

Intel Ethernet Controller XL710

Limitation	Details
For packets below 160 bytes, there is a hardware packet processing limit for the entire device of ~37 Mpps.	Refer to section *Intel® Ethernet Controller X710/XXV710/XL710 Throughput Limit* in document: Intel® Ethernet Controller X710/ XXV710/XL710 Specification Update.
The Intel XL710 Ethernet controller on all Intel FPGA PAC N3000-N variations do not support Wake-On-LAN.	If your BIOS or OS enables Wake-On-LAN PCIe errors during a power down may be logged. You must disable Wake-On-LAN on your system.

Supported Software

The following software packages support the Intel FPGA PAC N3000-N. Ensure that you review the following references to comprehend any known issues.

Intel Network Adapter Drivers

Intel provides drivers for the Intel Ethernet Controller XL710-BM2.

Table 6. Intel Ethernet Controller XL710-BM2 Driver Versions

This table lists the XL710 driver versions which are shipped with the Intel FPGA PAC N3000-N.

Driver	Version
Intel Network Adapter Driver for PCIe 40 Gigabit Ethernet Network Connections under Linux	2.10.19.82
Intel Network Adapter Virtual Function Driver for Intel 40 Gigabit Ethernet Network Connections	3.7.61.20

Related Information

- Network Adapter Driver for PCIe 40 Gigabit Ethernet Network Connections Under Linux Support Page
- Intel Network Adapter Virtual Function Driver for Intel 40 Gigabit Ethernet Network Connections Support Page
- Intel Acceleration Stack User Guide: Intel FPGA Programmable Acceleration Card N3000-N
  For details on the supported XL710-BM2 Firmware and Driver versions.

Revision History for Intel Acceleration Stack for Intel Xeon CPU with FPGAs v1.3.1 Release Notes

Document Version	Intel Acceleration Stack Version	Changes
2021.06.16	1.3.1	Updated the issue status in section: *Known Issues*.
2020.09.08	1.3.1	Updated the following sections: • *Minimum Requirements* • *Supported Features*
2020.06.15	1.3	Initial release.

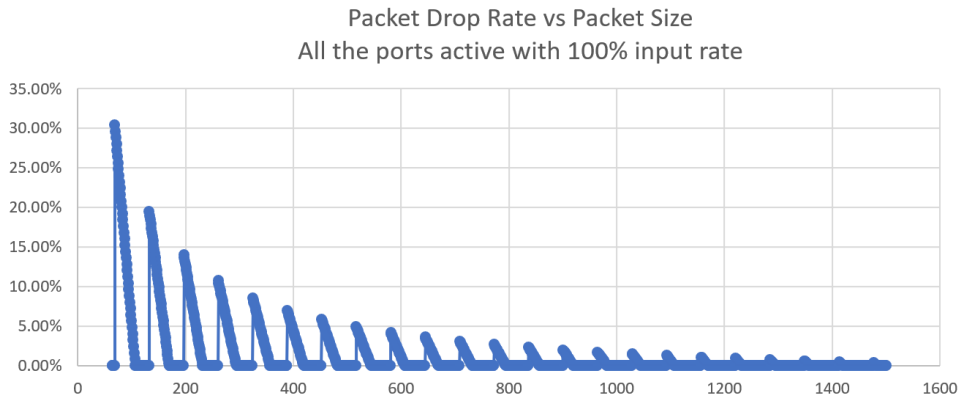
Intel Provided FPGA Factory Image Packet Drop

The FPGA factory image multiplexes all the Ethernet ports into one 512-bit (64 byte) bus. This bus has enough bandwidth to transport all the Ethernet ports when the packet size is a multiple of 64 bytes. When packet sizes are not multiples of 64 bytes, the last transfer of the packet on the bus carries the remainder of packet and the unused byte lanes do not carry valid data. For these packets, the bus does not have sufficient bandwidth to carry all traffic for some packet sizes. As a result of lack of bandwidth, the packet drops.

During internal tests, if all ports are active with fixed size packets that are not multiples of 64 bytes, some packet loss may occur. The worst case is 69-byte packets where the cyclic redundancy check (four bytes) is stripped off, resulting in 65 bytes transferred on the internal bus. This packet transfer takes two clock cycles. The first clock cycle transfers 64 bytes and the second clock cycle transfers one byte.

The following figure shows the predicted packet loss rate for the 2x2x25G and 4x25G network configurations when all the ports have 100% input capacity and same packet size.

Figure 1. Predicted Packet Loss Rate for 2x2x25G and 4x25G Configurations



Migrating your FPGA RTL Design from Intel Acceleration Stack v1.1 to Intel Acceleration Stack v1.3.1

The Intel FPGA PAC N3000-N supports operation at higher temperatures. The v1.3.1 RTL package, provided in the Acceleration Stack for Development, has updated the DDR4 IP core settings to refresh at a faster rate to maintain data integrity at higher temperatures. For your existing 1.1 FPGA design to work in the higher temperature environment supported by Intel FPGA PAC N3000-N, you must perform the following steps:

1. Port your 1.1 FPGA design to work in v1.3.1 RTL. Edit the `ccip_std_afu.sv` file, change line 52:

   From:

   ```
   localparam int TIMESTAMP_WIDTH              = 96
   ```

   To:

   ```
   parameter TIMESTAMP_WIDTH                   = 96
   ```

2. Recompile your RTL using the make flow as described in the Acceleration Functional Unit Developer Guide.