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# Intel FPGA Programmable Acceleration Card N3000-N Data Sheet

Updated for Intel® Acceleration Stack for Intel® Xeon® CPU with FPGAs: **1.3.1**

# Contents

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# 1. Introduction

**Figure 1.** **Intel FPGA Programmable Acceleration Card N3000-N**



This data sheet describes the Intel FPGA Programmable Acceleration Card N3000-N, featuring the Intel® Arria® 10 GT FPGA. This document provides electrical, mechanical, thermal, and other key specifications. The Intel FPGA Programmable Acceleration Card N3000-N is an enhanced version of the Intel FPGA PAC N3000-2 with changes for systems requiring Telcordia* Network Equipment Building System (NEBS) compliance. This data sheet assists network operators and system integrators to properly deploy this Intel FPGA PAC into their servers. This document describes the FPGA power envelope, connectivity speeds to memory, and network connectivity, so that accelerator function unit (AFU) developers can properly design and test their IP.

The Intel FPGA PAC N3000-N is supported by the Intel Acceleration Stack for Intel Xeon® CPU with FPGAs. The Intel Acceleration Stack provides a common developer interface to both application and acceleration function developers and includes drivers, Application Programming Interfaces (APIs) and an FPGA factory image.

For information about using the Intel Acceleration Stack for Intel Xeon CPU with FPGAs, refer to the *Intel Acceleration Stack User Guide for Intel FPGA Programmable Acceleration Card N3000-N*.

Intel validates each Intel FPGA PAC N3000-N to support large scale deployments requiring FPGA acceleration. This platform is targeted for market-specific acceleration in applications such as:

- Network Function Virtualization (NFV)
- Multi-Access Edge Computing (MEC)
- Video Transcoding
- Cyber Security
- High-Performance Computing
- Finance

**Related Information**

Intel Acceleration Stack User Guide for Intel FPGA Programmable Acceleration Card N3000-N

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# 2. Overview

This chapter provides an overview of the programmable acceleration card and describes the board architecture and its components.

## 2.1. Intel FPGA PAC N3000-N Block Diagram

**Figure 2.    Intel FPGA PAC N3000-N Functional Components**
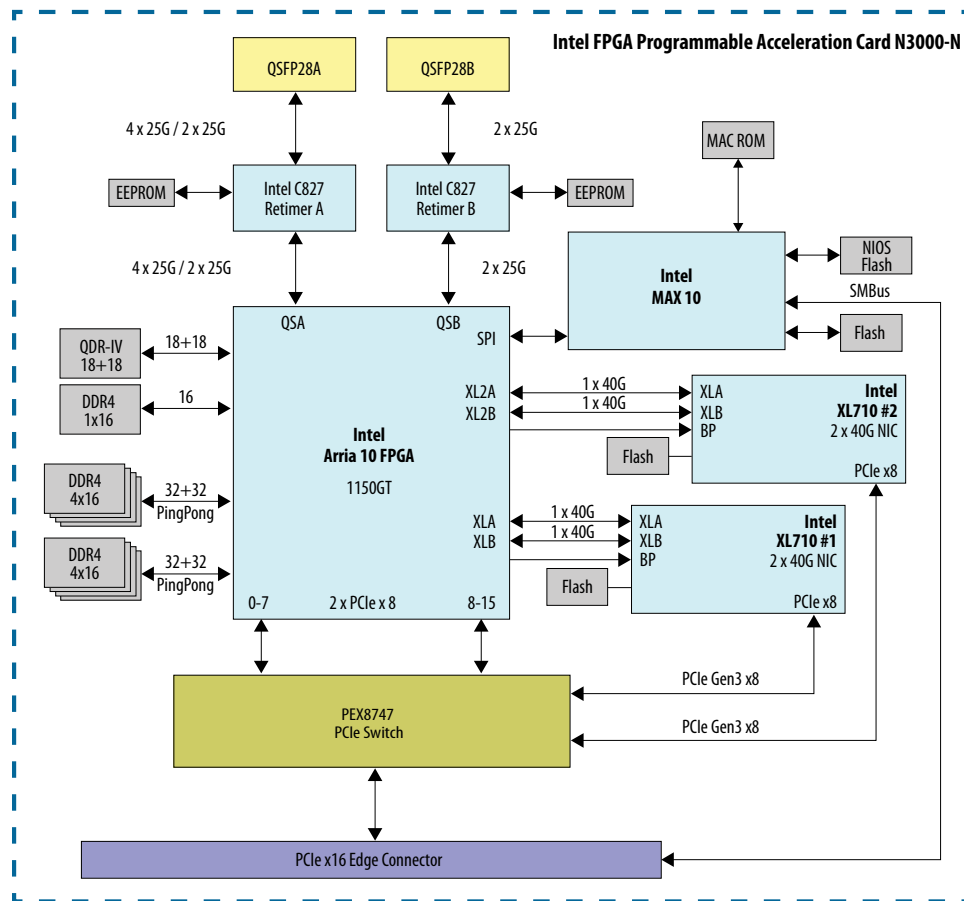


The Intel FPGA PAC N3000-N supports the following network configurations:

| Network Configuration | QSFP28 A | QSFP28 B | Intel XL710 #1 | Intel XL710 #2 |
|---|---|---|---|---|
| 2 x 2 x 25GbE | 2 x 25GbE | 2 x 25GbE | 2 x 40GbE | 2 x 40GbE |
| 4 x 25GbE | 4 x 25GbE | Not Used | 2 x 40GbE | 2 x 40GbE |

**ISO 9001:2015 Registered**

## 2.2. Overview of Product Features

### 2.2.1. Intel Arria 10 GT FPGA

The Intel Arria 10 FPGAs feature industry-leading programmable logic built on 20 nm process technology that integrates a rich feature set of embedded peripherals, embedded high-speed transceivers, hard memory controllers and IP protocol controllers. Variable-precision digital signal processing (DSP) blocks integrated with hardened floating point (IEEE 754-compliant) arithmetic blocks enable the Intel Arria 10 FPGAs to deliver floating point performance of up to 1.5 TFLOPS. Intel Arria 10 FPGAs have a comprehensive set of power-saving features. Combined, these features allow developers to build a versatile set of acceleration solutions.

**Table 1.       Intel Arria 10 GT FPGA**

| Device | Logic Elements (LE) | Adaptive Logic Modules (ALMs) | Registers | M20K Memory Blocks | M20K Memory (Mb) | MLAB Memory (Mb) | 18 x 19 Multipliers |
|---|---|---|---|---|---|---|---|
| GT 1150 | 1,150K | 427,200 | 1,708K | 2713 | 53 | 12.7 | 3036 |

When developing the accelerator function for the Intel FPGA PAC N3000-N, select the 10AT115S1F45E1SG device.

#### Related Information

- Intel FPGA Devices
    Detailed information about features of the Intel Arria 10 FPGA family

- Intel Arria 10 Device Data Sheet
    This data sheet describes the electrical characteristics, switching characteristics, configuration specifications, and I/O timing for Intel Arria 10 devices.

- Intel Arria 10 Device Overview
    This device overview provides information about known device issues affecting Intel Arria 10 GX/GT devices. It also offers design recommendations you should follow when using Intel Arria 10 GX/GT devices.

### 2.2.2. Intel Ethernet Controller XL710-BM2 Network Interface Controller

The Intel Ethernet Controller XL710-BM2 network interface controller (NIC) provides a hardware compatible interface with Linux drivers for networking software stacks. In addition, the Data Plane Development Toolkit (DPDK) interfaces directly through PCI Express* to the Intel Ethernet Controller XL710-BM2 NIC to provide queues for high performance networking applications. With data traffic traversing the Intel Arria 10 GT to and from the Intel Ethernet Controller XL710-BM2 NIC, you can use the Intel Arria 10 GT to perform ingress packet policing and ingress queuing, packet manipulation and addition of user defined packet tags. Similarly, the Intel Arria 10 GT can perform egress traffic shaping, queuing, and packet manipulation.

Since the XL710-BM2 NIC is not directly connected to the Ethernet interface, some traditional NIC card functionality is not supported:

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- Power Management functions such as Wake on LAN (WoL)

- Dynamic Port Speed (1, 10, 25 GbE)

- NC-SI and NIC SMBus access

- Preboot Execution Environment (PXE)

The XL710-BM2 only works with Intel FPGA PAC N3000-N specific firmware and best-known non-volatile memory (NVM) images as defined in the *Intel Acceleration Stack User Guide for Intel FPGA Programmable Acceleration Card N3000-N*.

**Related Information**

- Intel XL710-BM2 Device Information

- Intel Acceleration Stack User Guide for Intel FPGA Programmable Acceleration Card N3000-N

## 2.2.3. On-Board Memory

- 8 gigabyte (GB) DDR4 memory
  - 2133 Mbps
  - Two 4 GB DDR4 memory banks, part number: MT40A512M16JY-083E:B
  - Physical Interface Data Width: The Intel Arria 10 GT FPGA connects to each 4 GB memory bank with a Ping Pong PHY interface. The Ping Pong PHY interface functions as two separate 32 bit interfaces per memory bank. The Ping Pong PHY IP allows two Avalon® memory mapped interfaces to share address/command buses using time division multiplexing.

- 1 GB DDR4 memory, part number: MT40A512M16JY-083E:B
  - 2133 Mbps
  - Width: 16 bits

- One 144 megabit (Mb) QDR-IV memory, part number: CY7C4122KV13-106FCXC
  - 1066 MHz
  - 8M × 18

- Two 1 Gbit flash, part number: MT25QU01GBBB8E12-0SIT

## 2.2.4. Software and Firmware

- Intel Acceleration Stack for Intel Xeon CPU with FPGAs
- Intel Ethernet Controller XL710-BM2 NIC firmware for data rate configuration
- Intel MAX® 10 Board Management Controller Nios® II firmware
- Supports Data Plane Development Kit (DPDK)

**Related Information**

Data Plane Development Kit

## 2.2.5. Power

The Intel FPGA PAC N3000-N source power must be provided from both the 12 V PCIe slot and the 12 V Auxiliary 2×3 power connector. The Intel FPGA PAC does not power up if either power source is disconnected. The PCIe specifications define the 12 V Auxiliary power connector pin assignment.

The Intel FPGA PAC N3000-N follows PCIe standards for 150 W add-in cards where maximum current from the 12 V slot power source is 5.5 A (max) and the 12 V Auxiliary connector is 6.25 A (max). As a developer or solution provider, you must design and operate the FPGA workload within these power guides. If the FPGA workload exceeds the limits provided by the server vendor, server safeguards may shut down the Intel FPGA PAC N3000-N. Your FPGA workload must operate within the thermal specifications defined in this data sheet. The Intel FPGA PAC N3000-N is equipped with thermal protection circuitry that turns off board power if the FPGA junction temperature reaches 100 °C.

*Note:* The Intel FPGA PAC N3000-N does not support Wake-On LAN (WOL).

The figure below shows the pin-out for the PCIe 150W-ATX power connector.

**Figure 3.   Auxiliary Power Connector**
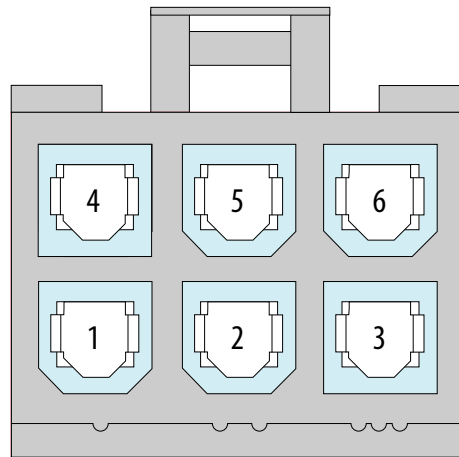


**Figure 4.   Auxiliary Power Connector Pin-out Table**

| Pin | Signal |
|-----|--------|
| 1 | +12 V |
| 2 | +12 V |
| 3 | +12 V |
| 4 | Ground |
| 5 | Sense |
| 6 | Ground |

## 2.2.6. Network Interface

The Intel FPGA PAC N3000-N has two Quad Small Form-Factor Pluggable (QSFP) 28 cages on the faceplate panel.

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25GbE network features:

- 2 x 25 GbE per QSFP28

- 4 X 25 GbE on QSFP A, QSFP B is disabled

- Programmable Forward Error Correction (FEC) including Reed-Solomon Forward Error Correction (RS-FEC), BASE-R FEC (also known as Firecode) and no FEC

  *Note:* Support is provided for IEEE 802.3 clause 108 and clause 74. Clause 91 is not supported.

- Supports 25GBASE-CR and 25GBASE-SR

The Intel FPGA PAC N3000-N supports Short Reach (SR) optical transceivers and Direct Attached Copper (DAC) cables up to 3m in length. QSFP modules must consume no more than 3.5 watts. The table below lists Ethernet cables, QSFP modules and Ethernet switches known to work with the Intel FPGA PAC N3000-N. Solution providers must validate Ethernet connectivity for the application.

**Table 2.     QSFP28 Support for the Intel FPGA PAC N3000-N using 25GbE Network Configuration**

| Module | Manufacturer | Part Number |
|---|---|---|
| QSFP28 Loopback Adapter Module, 100 Gb Ethernet, copper | Amphenol | SF-100GLB3.5W-0DB |
| 100GBASE-SR4 QSFP28 850nm 100m DOM Transceiver Module | FS.com | QSFP28-SR4-100G |
| 12-Fibers MTP/MPO Female Type 1 OM4 50/125 Multimode Fiber Loopback Module | FS.com | LPM-OM4-12MTP |
| QSFP28-to-2xQSFP28 25 GbE copper breakout cable | Mellanox | MCP7H00-G01AR (1.5m) MCP7H00-G02AR (2.5m) |
| 5m (16ft) MTP Female 12 Fibers Type B Plenum (OFNP) OM4 (OM3) 50/125 Multimode Elite Trunk Cable | FS.com | 68023 |
| Ethernet Switch | Cisco | N9K-93180YC-FX |
| Ethernet Switch | Mellanox | MSN2410-CB2R |

*Note:*       The Intel FPGA PAC N3000-N is delivered with a sample FPGA workload that supports simple pass through functionality to demonstrate Ethernet functionality with the following capabilities:

- User configurable pause frame flow control generation

- User configurable maximum packet size up to 9600 bytes

- Per port Ethernet statistics

The Intel provided sample FPGA workload does not support the following:

- Pausing of transmitted traffic in response to received pause frame

- Auto-negotiation

You can create FPGA workloads that support these functions, if required.

### 2.2.6.1. Intel Ethernet Connection C827 Retimer

All network interfaces pass through the Intel Ethernet Connection C827 Retimer device. This device provides tightly controlled network timing performance for Ethernet. The Intel Ethernet Connection C827 Retimer also provides forward error correction (FEC) functionality to support 25GBASE-R.

The Intel Arria 10 FPGA image configures the Intel Ethernet Connection C827 Retimer device.

## 2.3. PCIe Overview

The communication link between the Intel FPGA PAC N3000-N and a local host server is through a PCIe Gen3 x16 Edge Connector. The card contains a PEX8747 PCIe switch with one upstream port (x16) on the edge connector, and four downstream ports (all x8) connected to Intel Arria 10 FPGA (two x8 ports) and one x8 port per Intel Ethernet Controller XL710 device.

The Intel FPGA PAC N3000-N supports PCIe* Gen3 speed. The PEX8747 PCIe switch links between Intel Arria10 and XL710 run at Gen3 speed, whereas the upstream port on the edge connector runs the highest speed supported by the host up to Gen3 speed.

The PCIe edge connector SMBus is connected to the Intel MAX 10 BMC.

| PCIe Device Description | PCIe Vendor ID (VID) | PCIe Device ID (DID) | PCIe Sub-Vendor ID (SVID) | PCIe Sub-Device ID (SDID) | Class |
|---|---|---|---|---|---|
| Intel Arria 10 FPGA PCIe Management Interface | | 0x0B30 | | | 0x1200 |
| Intel Arria 10 FPGA Secondary PCIe Interface | 0x8086 | 0x0B32 | 0x8086 | 0000 | 0x1200 |
| XL710 Ethernet NIC (25G) | | 0x0D58 | | | 0x0200 |

## 2.4. Board Management Controller Overview

The Intel FPGA PAC N3000-N contains an Intel MAX 10 Board Management Controller (BMC). This BMC is responsible for controlling, monitoring and giving low-level access to board features. The Intel MAX 10 BMC interfaces with on-board sensors, the FPGA and the flash, and controls power-on/power-off sequences, FPGA configuration and telemetry data polling. The BMC communicates with the server system controller using either Platform Level Data Model (PLDM) version 1.1.1 protocol or I$^2$C through the PCIe SMBus.

An external Quad SPI flash stores the BMC firmware and the BMC firmware for the Nios II is field upgradeable over the PCIe using the remote system update feature. Only Intel provided BMC firmware is permitted.

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**BMC Features**

- Supports FPGA configuration and reconfiguration.

- Supports Secure Remote System Update for Intel MAX 10 BMC FPGA update image, Intel Arria 10 GT FPGA user image, and Nios firmware image.

- Monitors telemetry data for board temperature, voltage, and current.

- Reports telemetry data to host BMC through Platform Level Data Model (PLDM) over Management Component Transport Protocol (MCTP) SMBus.

- Provides protective action when temperature and auxiliary power readings are outside of critical thresholds.

- Provides power up/down sequencing and fault detection with automatic shut-down protection.

- Interfaces with sensors, FPGA, flash, and QSFPs.

**Sensor Monitoring Features**

The Intel FPGA PAC N3000-N incorporates sensor monitoring that allow the host server to read telemetry data such as voltage, current, power, and temperature information from various components on the board. The host system controller accesses these sensors using either PLDM over MCTP or I$^2$C through the PCIe SMBus.

**Table 3.    PDRs Sensor Names and Record Handle**

| Function | Sensor Name | Sensor Information | | PLDM | | |
|---|---|---|---|---|---|---|
| | | Sensor Reading Source (Component) | PDR Record Handle | Thresholds in PDR | Threshold changes allowed through PLDM | |
| Total Intel FPGA PAC input power | Board Power | Calculate from PCIe fingers 12V Current and Voltage | 1 | 0 | No | |
| PCIe fingers 12 V Current | 12 V Backplane Current | PAC1932 SENSE1 | 2 | 0 | No | |
| PCIe fingers 12 V Voltage | 12 V Backplane Voltage | PAC1932 SENSE1 | 3 | 0 | No | |
| 1.2 V Rail Voltage | 1.2 V Voltage | MAX10 ADC | 4 | 0 | No | |
| 1.8 V Rail Voltage | 1.8 V Voltage | MAX 10 ADC | 6 | 0 | No | |
| 3.3 V Rail Voltage | 3.3 V Voltage | MAX 10 ADC | 8 | 0 | No | |
| FPGA Core Voltage | FPGA Core Voltage | LTC3884 (U44) | 10 | 0 | No | |
| FPGA Core Current | FPGA Core Current | LTC3884 (U44) | 11 | 0 | No | |
| FPGA Core Temperature | FPGA Core Temperature | FPGA temp diode through TMP411 | 12 | Upper Warning: 90 Upper Fatal: 100 | Yes | |
| Board Temperature | Board Temperature | TMP411 (U65) | 13 | Upper Warning: 85 Upper Fatal: 100 | Yes | |
| QSFP A Voltage | QSFP A Voltage | External QSFP module (J4) | 14 | 0 | No | |
| QSFP A Temperature | QSFP A Temperature | External QSFP module (J4) | 15 | Upper Warning: Value set by QSFP Vendor Upper Fatal: Value set by QSFP Vendor | No | |
| PCIe Auxiliary 12V Current | 12 V AUX | PAC1932 SENSE2 | 24 | 0 | No | |
| PCIe Auxiliary 12V Voltage | 12 V AUX Voltage | PAC1932 SENSE2 | 25 | 0 | No | |
| QSFP B Voltage | QSFP B Voltage | External QSFP module (J5) | 37 | 0 | No | |
| QSFP B Temperature | QSFP B Temperature | External QSFP module (J5) | 38 | Upper Warning: Value set by QSFP Vendor Upper Fatal: Value set by QSFP Vendor | No | |
| Intel C827) Retimer A Core Temperature | Retimer A Core Temperature | Intel C827) Retimer chip (88EC055) (U18A) | 44 | 0 | No | |
| Intel C827) Retimer A Serdes Temperature | Retimer A Serdes Temperature | Intel C827) Retimer chip (88EC055) (U18A) | 45 | 0 | No | |
| Intel C827) Retimer B Core Temperature | Retimer B Core Temperature | Intel C827) Retimer chip (88EC055) (U23A) | 46 | 0 | No | |
| Intel C827) Retimer B Serdes Temperature | Retimer B Serdes Temperature | Intel C827) Retimer chip (88EC055) (U23A) | 47 | 0 | No | |

Refer to the *Board Monitoring through I²C SMBus* section of the *Board Management Controller User Guide: Intel FPGA Programmable Acceleration Card N3000-N* for information on telemetry data register map.

The BMC shuts down power to the board under the following conditions:

- 12 V Auxiliary or 12 V backplane supply voltage is below 10.46 V

- FPGA core temperature reaches 100 °C

- Board temperature reaches 100 °C

*Note:*         All faceplate LEDs blink yellow to indicate a card has shutdown due to one of the above conditions.

**Related Information**

Board Management Controller User Guide: Intel FPGA Programmable Acceleration Card N3000-N

## 2.4.1. Field Replaceable Unit Identification (FRUID) EEPROM

A Field Replaceable Unit Identification (FRUID) EEPROM (Microchip 24AA024-I/SN) located at default SMBUS address `0xA0` is connected to the SMBUS of the PCIe interface. This FRUID EEPROM is powered by the PCIe 3.3 V Auxiliary power provided at the PCIe slot connector of the host server. This allows the FRUID EEPROM to be readable even when 12 V power to the slot is not provided by the host server.

This FRUID contains board specific information that identify the card installed into the PCIe slot. The FRUID contains the following information:

- Board Manufacturer

- Board Model Number

- Board Serial Number

- Location of Manufacturer

- Date of Manufacture

**Related Information**

Board Management Controller User Guide: Intel FPGA Programmable Acceleration Card N3000-N

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# 3. System Compatibility

This chapter provides information about the supported Linux distribution and kernel combination.

**Table 4.    Operating System Compatibility**

| Distribution Version | Kernel |
|---|---|
| Red Hat Enterprise Linux (RHEL) 8.2 | Kernel 4.18RT |
| CentOS Linux version 7.6 | Kernel 4.19 |

OEM partners validate server platforms. Solution providers must verify if the server and Intel FPGA PAC N3000-N meets application requirements.

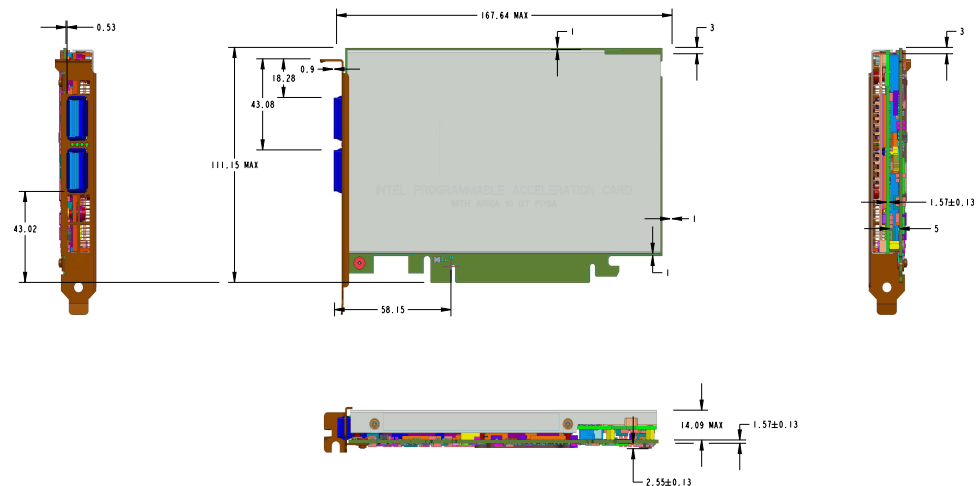**Related Information**

Intel FPGA PAC N3000-N Ordering Information

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# 4. Mechanical Information

**Intel FPGA PAC N3000-N Dimensions**

*Note:*     All dimensions are in mm.

- Standard height, half length PCIe card
- Maximum component height: 14.47 mm
- PCIe x16 mechanical
- Tested to withstand Non-Operational Square Wave Shock Test of 32 G
- Card dimension tolerance: +/- 0.13 mm
- QSFP connector protrusion: 5.2 +/- 0.50 mm

**Figure 5.      Intel FPGA PAC N3000-N Dimensions**

**Intel FPGA PAC N3000-N Port and LED Information**

**Figure 6.     Intel FPGA PAC N3000-N Port Information**



QSFP – B
2 x 2 x 25G
Ports 2 and 3

QSFP – B
4 x 25G
Not Used

QSFP – B  Activity LED

QSFP – A Connectivity LED

QSFP – B Connectivity LED

QSFP – A Activity LED

QSFP – A
2 x 2 x 25G
Ports 0 and 1

QSFP- A
4 x 25G
Ports 3 - 0
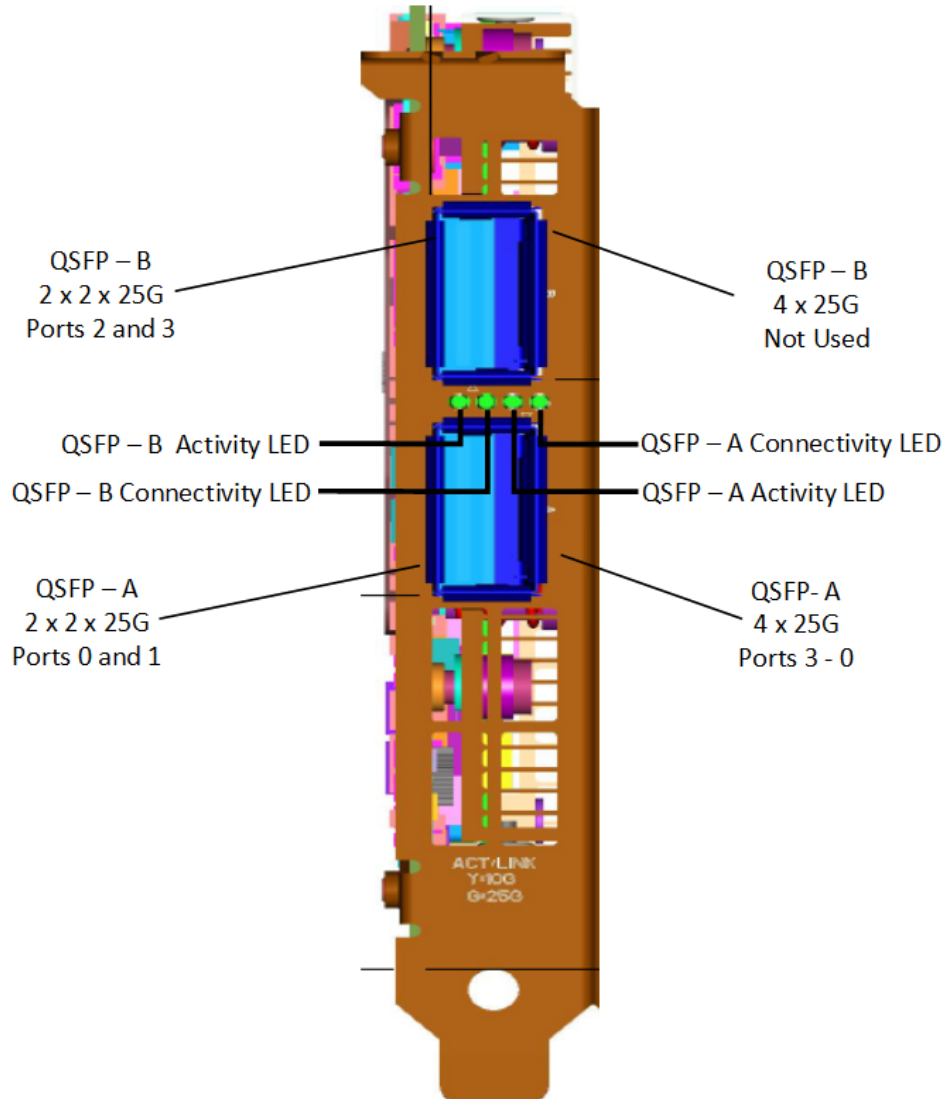
**Table 5.     OPN Information**

| OPN | Net Weight (Kg) | Gross Weight (Kg) | Description |
|-----|-----------------|-------------------|-------------|
| BD-NVV-N3000-3ES | 0.450 | 1.28 | Engineering Sample 25 GbE, thermally enhanced |
| BD-NVV-N3000-3 | 0.450 | 1.28 | Production 25 GbE, thermally enhanced |

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### Intel FPGA PAC N3000-N LEDs

**Table 6.     LED Behavior**

| LED Type | Description |
|---|---|
| Connectivity LED | Green means link is up with link speed of 25 G. |
| | Off means link is down. |
| Activity LED | Green blinking at 1 Hz means link activity present. |
| | Off means link is down or no activity. |
| All LEDs blinking yellow | Issue with power.<br>Check card insertion in PCIe card slot, PCIe edge connector 12 V and auxiliary 12 V power. |

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# 5. Thermal Specifications

The high performance devices installed on the Intel FPGA PAC N3000-N require server based forced air cooling to maintain proper operating temperature. This section provides air flow requirements for the Intel FPGA PAC N3000-N. Intel recommends that sufficient air flow be provided to the Intel Arria 10 GT FPGA to maintain junction temperature below 95 °C.

**Figure 7.    Air Flow Pattern**

**Table 7.    Thermal Terms and Descriptions**

| Term | Description |
|------|-------------|
| Cubic Feet per Minute (CFM) | Volumetric airflow rate, in cubic feet per minute, of air passing through the PCIe faceplate of the Intel FPGA PAC N3000-N. |
| $T_j$ | FPGA Junction Temperature |
| $T_{LA}$ | Local Ambient temperature. Temperature of forced air as it enters the Intel FPGA PAC N3000-N.<br>*Note:* In many systems, this is higher than the room ambient due to heating effects of chassis components. |

The Intel FPGA PAC N3000-N uses a passive heatsink. The server must provide sufficient forced airflow to keep the FPGA and board components within the following operating conditions:

**Table 8.    Power/Thermal Requirements**

| Parameter | Value |
|-----------|-------|
| Intel Arria 10 FPGA Thermal Design Power | ≤ 71 W |
| Intel FPGA PAC N3000-N Thermal Design Power | ≤ 131 W |
| Recommended FPGA Maximum Operating Temperature* | 95 °C |
| FPGA $T_j$ Max / Thermal protection shutdown | 100 °C |
| Max $T_{LA}$ (Forward Airflow) | up to 61 °C depending on cooling flow available |
| Max $T_{LA}$ (Reverse Airflow) | up to 61 °C depending on cooling flow available |
| Recommended Board Max Operating Temp* | 95 °C |
| Board $T_j$ Max / Thermal protection shutdown | 100 °C |
| Min $T_{LA}$ | -5 °C[1] |
| Max QSFP Power (each) | 3.5 W |
| Max 12 V PCIe Slot current* | 5.5 A |
| Max 12 V AUX current* | 6.25 A |
| Max FPGA core current* | 50 A |

\* Values can be read at runtime using the `fpgainfo` command.

*Note:*    The Intel FPGA PAC N3000-N supports cold start from 0 °C and an operating temperature range of -5 °C to +55 °C, according to Telcordia GR63-CORE and GR-3108 Class 1 range. Altitude simulation testing may be performed using a temperature compensation method of 1 °C for every 1000 feet up to 61 °C. Intel FPGA PAC N3000-N supports inlet temperatures (during operation) of less than 0 °C. The minimum inlet temperature depends on fan speed control settings of the host server as well as the power scenario that needs to be supported at lower inlet temperatures. It is expected that a -5 °C inlet operating temperature would be supported as the operating temperature of the FPGA and other components should be over 0 °C due to component operational heating.

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[1]    Actual FPGA assumed to be greater than or equal to 0 °C.

Note:
Intel Arria 10 FPGA total power consumption cannot be obtained from on-board BMC sensors. Use the Intel Quartus® Prime Power Analyzer to verify compliance with this value for your design.

**Related Information**

Power Analysis and Optimization User Guide: Intel Quartus Prime Pro Edition
The Intel Quartus Prime Pro Edition software provides a complete design environment for FPGA and SoC designs. The Power Analyzer is described in the Power Analysis and Optimization User Guide: Intel Quartus Prime Pro Edition.

# 5.1. Cooling Requirements

**Figure 8.    Forward and Reverse Flow Cooling Curve**
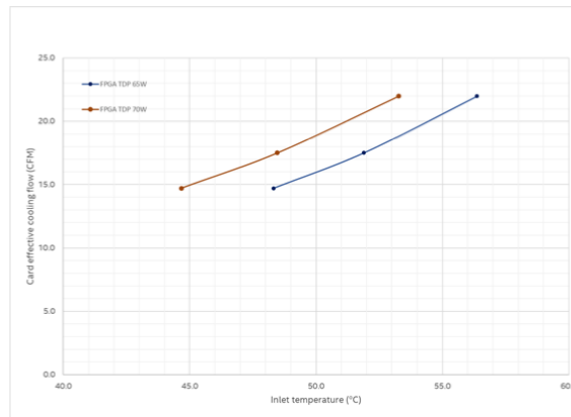


Note:
Cooling curve generated in a ducted wind-tunnel configuration using 2 x 2 x 25G configuration with 5 C FPGA junction temperature margin.

Note:
Your in-system testing is required to confirm cooling capability of server and Intel FPGA PAC N3000-N installation.

**Table 9.    Local Air Inlet Temperature and Air Flow Values for Forward and Reverse Cooling**

| FPGA Power = 65 W | | FPGA Power = 70 W | |
|---|---|---|---|
| $T_{LA}$ (°C) | Air Flow (CFM) | $T_{LA}$ (°C) | Air Flow (CFM) |
| 48 | 14.7 | 45 | 14.7 |
| 52 | 17.5 | 49 | 17.5 |
| 56 | 22.0 | 53 | 22.0 |

Note:
$T_{LA}$ values shown in the tables and charts of this section are informational for maintaining junction temperature and board temperature within thermal limits, and may represent conditions outside of the supported operating range.

*Note:* These flow curves are based on numerical analysis and wind tunnel testing and should be used as a starting point for thermal design estimation. Thermal performance of host systems may vary. Therefore, you should perform in-system thermal validation using the thermal power load (TPL) FPGA workload provided with the *Intel FPGA Programmable Acceleration Card N3000-N Platform Qualification Guidelines*. Contact your Intel Sales representative to obtain this guide and TPL FPGA workload.

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# 6. Intel Provided FPGA Image

The Intel Arria 10 FPGA factory image includes the following Intellectual Property (IP) to support in the development of function accelerators:

- The PCIe IP core

- The Core Cache Interface protocol (CCI-P) fabric

- DDR4 memory interface controller IP

- QDR4 memory interface controller IP

- 25 GbE physical interface and MACs with pass-through connectivity between Intel Ethernet Connection C827 Retimer and Intel Ethernet Controller XL710-BM2

- FPGA Management Engine (FME)

- Nios core to configure the Intel Ethernet Connection C827 Retimers

Specific features of the factory image are listed in the following document:

- *Intel Acceleration Stack User Guide for Intel FPGA Programmable Acceleration Card N3000-N.*

The 1024 Mb FPGA flash memory stores two FPGA images. One image is the user image and the other image is a backup factory image. The factory image is only loaded when the user image fails to load from flash to the FPGA.

The Intel FPGA PAC N3000-N does not support partial reconfiguration. The FPGA image is a full-device bit stream that is loaded when the system is powered up or after you enter a remote system update command.

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# A. References

**Related Information**

Intel Arria 10 GX/GT Device Errata and Design Recommendations

This errata sheet provides information about known device issues affecting Intel Arria 10 GX/GT devices. It also offers design recommendations you should follow when using Intel Arria 10 GX/GT devices.

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# B. Safety and Regulatory Information

## B.1. Regulatory Compliance

### Regulatory Model Number: BD-NVV-N3000-N

### United States Federal Communications Commission (FCC) Class A User Information

The Class A Product: Intel FPGA Programmable Acceleration Card N3000-N complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.

2. This device must accept the interference received, including interference that may cause undesired operation.

***Attention:*** This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with other instructions, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference is at his/her own expense.

***Caution:*** If this device is changed or modified without permission from Intel, the user may void his or her authority to operate the equipment.
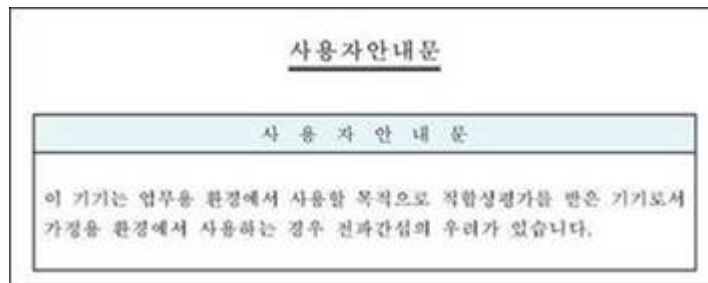
### VCCI Class A Statement

この装置は、クラスA情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。この場合には使用者が適切な対策を講ずるよう要求されることがあります。　VCCI－A

### BSMI Class A Statement

警告使用者:
此為甲類資訊技術設備，於居住環境中使用時，
可能會造成射頻擾動，在此種情況下，使用者會
被要求採取某些適當的對策。

**Republic of Korea KCC Notice Class A**



**European Community Manufacturer Declaration**



**Belgium (French)**

Par la présente, Intel Corporation déclare que la carte Intel FPGA Programmable Acceleration Card N3000-N est conforme aux directives 2014/30/UE, 2014/35/UE et 2011/65/UE.

Att. Corp Quality, Intel Deutschland GmbH, Am Campeon 10-12, Neubiberg, 85579 - Germany

Le texte intégral en anglais de la déclaration européenne de conformité est disponible à l'adresse suivante:
https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

**Germany**

Hiermit erklärt die Intel Corporation, dass die Intel FPGA Programmable Acceleration Card N3000-N for Networking den Richtlinien 2014/30/EU, 2014/35/EU und 2011/65/EU entspricht.

Att. Corp Quality, Intel Deutschland GmbH,

Am Campeon 10-12, Neubiberg, 85579 - Germany

Die vollständige EU-Konformitätserklärung ist in englischer Sprache unter der folgenden URL einsehbar:
https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

**Denmark**

Intel Corporation erklærer hermed, at Intel FPGA Programmable Acceleration Card N3000-N for Networking overholder direktiverne 2014/30/EU, 2014/35/EU og 2011/65/EU.

Att. Corp Quality, Intel Deutschland GmbH,

Am Campeon 10-12, Neubiberg, 85579 - Germany

Den fulde tekst for EUs overensstemmelseserklæring findes på engelsk på følgende adresse:

https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

### Dutch

Intel Corporation verklaart hierbij dat Intel FPGA Programmable Acceleration Card N3000-N for Networking in overeenstemming is met de richtlijnen 2014/30/EU, 2014/35/EU en 2011/65/EU.

Att. Corp Quality, Intel Deutschland GmbH,

Am Campeon 10-12, Neubiberg, 85579 - Germany

De volledige Engelse tekst van de EU-conformiteitsverklaring is hier beschikbaar: https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

### Spain

Por la presente, Intel Corporation declara que Intel FPGA Programmable Acceleration Card N3000-N for Networking cumple las directivas 2014/30/UE, 2014/35/UE y 2011/65/UE.

Att. Corp Quality, Intel Deutschland GmbH,

Am Campeon 10-12, Neubiberg, 85579 - Germany

El texto completo (en inglés) de la declaración de conformidad de la UE está disponible en la siguiente URL: https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

### Finland

Intel Corporation vakuuttaa täten, että Intel FPGA Programmable Acceleration Card N3000-N for Networking on direktiivien 2014/30/EU, 2014/35/EU ja 2011/65/EU määräysten mukainen.

Att. Corp Quality, Intel Deutschland GmbH,

Am Campeon 10-12, Neubiberg, 85579 - Germany

EU-vaatimustenmukaisuusvakuutuksen koko englanninkielinen teksti on saatavilla osoitteessa: https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

### France

Par la présente, Intel Corporation déclare que la carte Intel FPGA Programmable Acceleration Card N3000-N for Networking est conforme aux directives 2014/30/UE, 2014/35/UE et 2011/65/UE.

Att. Corp Quality, Intel Deutschland GmbH,

Am Campeon 10-12, Neubiberg, 85579 - Germany

Le texte intégral en anglais de la déclaration européenne de conformité est disponible à l'adresse suivante :

https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

### United Kingdom

Hereby, Intel Corporation declares that the Intel FPGA Programmable Acceleration Card N3000-N for Networking is in compliance with Directives 2014/30/EU, 2014/35/EU and 2011/65/EU.

Att. Corp Quality, Intel Deutschland GmbH,

Am Campeon 10-12, Neubiberg, 85579 - Germany

The full text of the EU declaration of conformity is available at the following URL:

https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

### Ireland

Hereby, Intel Corporation declares that the Intel FPGA Programmable Acceleration Card N3000-N for Networking is in compliance with Directives 2014/30/EU, 2014/35/EU and 2011/65/EU.

Att. Corp Quality, Intel Deutschland GmbH,

Am Campeon 10-12, Neubiberg, 85579 - Germany

The full text of the EU declaration of conformity is available at the following URL:

https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

### Italy

Con il presente documento, Intel Corporation dichiara che la scheda di accelerazione Intel FPGA Programmable Acceleration Card N3000-N for Networking è conforme alle direttive 2014/30/EU, 2014/35/EU e 2011/65/EU.

Att. Corp Quality, Intel Deutschland GmbH,

Am Campeon 10-12, Neubiberg, 85579 - Germany

Il testo completo della dichiarazione di conformità UE in lingua inglese è disponibile al seguente indirizzo:
https://www.intel.com/content/www/us/en/declaration-of-conformity/cprs-doc/homepage.html

### End-of-Life/ Product Recycling

Product recycling and end-of-life take-back systems and requirements vary by country.

Contact the retailer or distributor of this product for information about product recycling and take-back.

**Canada EMC Compliance Statement**

This Class A digital apparatus complies with Canadian ICES-003.

Cet appareil numérique de la classe A est conforme à la norme NMB-003 du Canada.

**Regulatory Markings**

D33025
RoHS



R-R-CPU-BD-NVV-N3000

CAN ICES-3 (A)/NMB-3(A)

## Hazardous Substances Table

| 部件名称<br>Component Name | 有毒有害物质或元素 Hazardous Substance | | | | | |
|---|---|---|---|---|---|---|
| | 铅<br>Pb | 汞<br>Hg | 镉<br>Cd | 六价铬<br>Cr (VI) | 多溴联苯<br>PBB | 多溴二苯醚<br>PBDE |
| 金属部件<br>Metal Parts | ○ | ○ | ○ | ○ | ○ | ○ |
| 印刷电路板组件<br>Printed Board Assemblies (PBA) | X | ○ | ○ | ○ | ○ | ○ |
| ○：表示该有毒有害物质在该部件所有均质材料中的含量均在 GB/T 26572 标准规定的限量要求以下。<br>○：Indicates that this hazardous substance contained in all homogeneous materials of such component is within the limits specified in GB/T 26572.<br>×：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 GB/T 26572 标准规定的限量要求。<br>×：Indicates that the content of such hazardous substance in at least a homogeneous material of such component exceeds the limits specified in GB/T 26572.<br>　对销售之日的所售产品,本表显示我公司供应链的电子信息产品可能包含这些物质。注意：在所售产品中可能会也可能不会含有所列的部件。<br>This table shows where these substances may be found in the supply chain of our electronic information products, as of the date of sale of the enclosed product. Note that some of the component types listed above may or may not be a part of the enclosed product. | | | | | | |
| 　除非另外特别的标注,此标志为针对所涉及产品的环保使用期限标志. 某些可更换的零部件可能会有一个不同的环保使用期限(例如,电池单元模块).<br>　此环保使用期限只适用于产品在产品手册中所规定的条件下工作. | | | | | | |

**intel.**

# C. Document Revision History for the Intel FPGA Programmable Acceleration Card N3000-N Data Sheet

| Document Version | Intel Acceleration Stack Version | Changes |
|---|---|---|
| 2020.12.11 | 1.3.1 | Updated the "Auxiliary Power Connector" figure. |
| 2020.09.08 | 1.3.1 | • Added Red Hat Enterprise Linux 8.2 to the "Operating System Compatibility" table in the *System Compatibility* section.<br>• Added Card dimension tolerance and QSFP connector protrusion to the Intel FPGA PAC N3000-N Dimensions list in the *Mechanical Information* section. |
| 2020.06.15 | 1.3 | Initial release. |

**ISO 9001:2015 Registered**