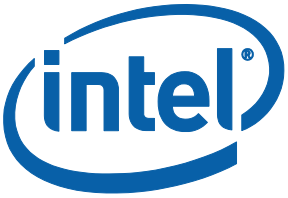


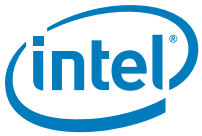
Alpine-Ridge DP

Thunderbolt Interface Controller

Datasheet

Revision 1.03
October 2015

Intel confidential



Legal Statements

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS OTHERWISE AGREED IN WRITING BY INTEL, THE INTEL PRODUCTS ARE NOT DESIGNED NOR INTENDED FOR ANY APPLICATION IN WHICH THE FAILURE OF THE INTEL PRODUCT COULD CREATE A SITUATION WHERE PERSONAL INJURY OR DEATH MAY OCCUR.

Intel may make changes to specifications and product descriptions at any time, without notice. Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. The information here is subject to change without notice. Do not finalize a design with this information.

The products described in this document may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an order number and are referenced in this document, or other Intel literature, may be obtained by calling 1-800-548-4725, or go to: http://www.intel.com/#/en_US_01

Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

This document contains information on products in the design phase of development.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

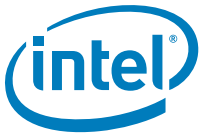
Thunderbolt, Intel and the Intel logo are trademarks or registered trademarks of Intel Corporation or its subsidiaries in the United States and other countries.

***Other names and brands may be claimed as the property of others.**

For more information go to http://www.intel.com/technology/io/thunderbolt.

Revision History

Date	Revision	Description
December 9, 2013	0.3	Initial revision of Alpine Ridge Datasheet
March 5, 2014	0.5	Change where made in: Electrical Specifications chapter, Pin Interface chapter, Introduction chapter, Board Schematics chapter, Mechanical Specification chapter.
March 10, 2014	0.51	Change where made in: Mechanical Specification chapter.
March 26, 2014	0.52	Change where made in: Electrical Specifications chapter, Pin Interface chapter, Board Schematics chapter, Mechanical Specification chapter.
April 13, 2014	0.53	Change where made in: Pin Interface chapter, Mechanical Specification chapter.
May 15, 2014	0.54	Change where made in: Introduction chapter, Board Schematics chapter, Testability chapter, Pin Interface chapter- the following ball manes were changed : PA_RX0_DPSRC2, changed to - PA_RX1 PA_TX0_DPSRC3, changed to - PA_TX1 PA_TX1_DPSRC0, changed to - PA_TX0 PA_RX1_DPSRC1, changed to - PA_RX0 (similarly to PB)
May 18, 2014	0.55	Change where made in: Introduction chapter
June 26, 2014	0.7	Change where made in: Security Levels and Lane Bonding chapters where removed and converged to a new In-line functionality chapter Introduction chapter - updated block diagram figures Electrical Specification - updated power on sequence Testability - chapter update Flash Memory - chapter update Chapters not included in this revision - Programing Interface, Appendices
August 3, 2014	0.85	Change where made in: Introduction Pin interface Programming Interface Mechanical Specification Power up and Wake sequences Testability Board schematics



Date	Revision	Description
September 22, 2014	0.89	Change where made in: Inline functionality - added QoS description, added eye monitor for DP and PCIe Phys Programming interface - registers updates Pin interface Flash Memory Power up and Wake sequences
November 09, 2014	0.9	Change where made in: Pin interface Programming interface - registers updates Inline functionality Electrical Specifications Board Schematics Appendices
November 17, 2014	0.91	Change where made in: Pin interface Programming interface Inline functionality Board Schematics
February 12, 2015	0.95	Change where made in: Introduction Pin interface Flash Memory Programming interface Power Up and Wake Flows Appendices added CDR mode chapter
June 14, 2015	0.99	Change where made in: Electrical Spec Appendices Flash Memory Programing Interface Board Schematics Inline Functionality Introduction
July 28th, 2015	1.0	Updates in Programming Interface Updates in Pin Interface Updates in Electrical Specifications Fixing of Unresolved Cross-References

Date	Revision	Description
September 20th, 2015	1.01	Updates in Programming Interface Updates in Pin Interface Updates in Electrical Specifications
October 7th, 2015	1.02	Updates in Programming Interface Updates in Pin Interface Updates in Appendices
October 12th, 2015	1.03	Updates in Programming Interface

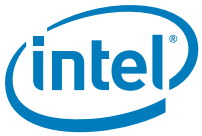
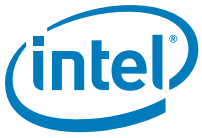
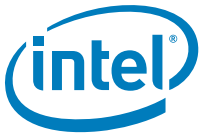


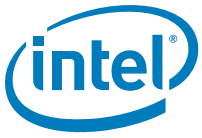
Table of Contents

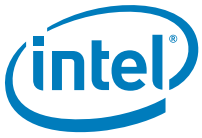


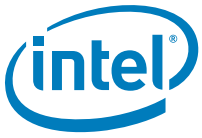
List of Figures

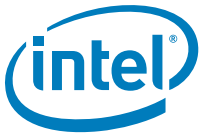


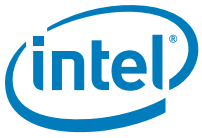
List of Tables

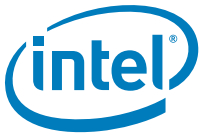












1.0 Introduction

The Alpine-Ridge DP is a Thunderbolt controller (see block diagram in Figure 1 and Figure 2) that acts as a point of entry or a point of exit in the Thunderbolt domain. The Thunderbolt domain is built as a daisy chain of Thunderbolt enabled products for the encapsulated protocols - PCIe and DisplayPort. These protocols are encapsulated into the Thunderbolt fabric and can be tunneled across the Thunderbolt domain. The Alpine-Ridge DP Thunderbolt controller also acts as a flexible re-driver for DP protocol.

Alpine-Ridge DP, as a host, deploys an internal connection manager for the Thunderbolt cloud which removes the need of a software driver, or predefined mapping.

Alpine-Ridge DP can be implemented in various systems such as PCs, laptops and tablets, or devices such as storage, docks, displays, home entertainment, cameras, computer peripherals, high end video editing systems, and any other PCIe based device that can be used to extend system capabilities outside of the system's box.

Alpine-Ridge DP Thunderbolt connection data rate is 20Gbps per lane and is compatible with Thunderbolt 3 specification enabling Thunderbolt link at up to 2x20Gbps, as well as backward compatible with Thunderbolt 1 (10Gbps) and Thunderbolt 2 (2x10Gbps) specifications.

Alpine-Ridge DP supports the following standard protocol IOs:

- PCIe Gen3
- DisplayPort (DP) 1.2
- DP++ (Dual mode DisplayPort)
- USB 3.1
- USB 2.0
- SPI
- JTAG
- I2C

Alpine-Ridge DP port connectivity is through USB-C connector supporting the following modes:

Connection Type	Mode	USB-C Port Details
USB	Native	Single SSP/SS + Single HS/FS/LS USB connection

Connection Type	Mode	USB-C Port Details
Thunderbolt	Alternate	Dual Thunderbolt lanes running at 10Gpbs/ 20Gbps
Display Port	Alternate	x1/x2/x4 Display Port running at 1.62Gbps/ 2.7Gbpshz/5.4Gbps signaling rate
MultiFunction DP	Alternate	Single SSP/SS + Single HS/FS/LS USB connection + x2 Display Port running at 1.62Gbps/2.7Gbps/5.4Gbps signaling rate

Figure 1. Alpine-Ridge DP Controller Block Diagram (Host view)

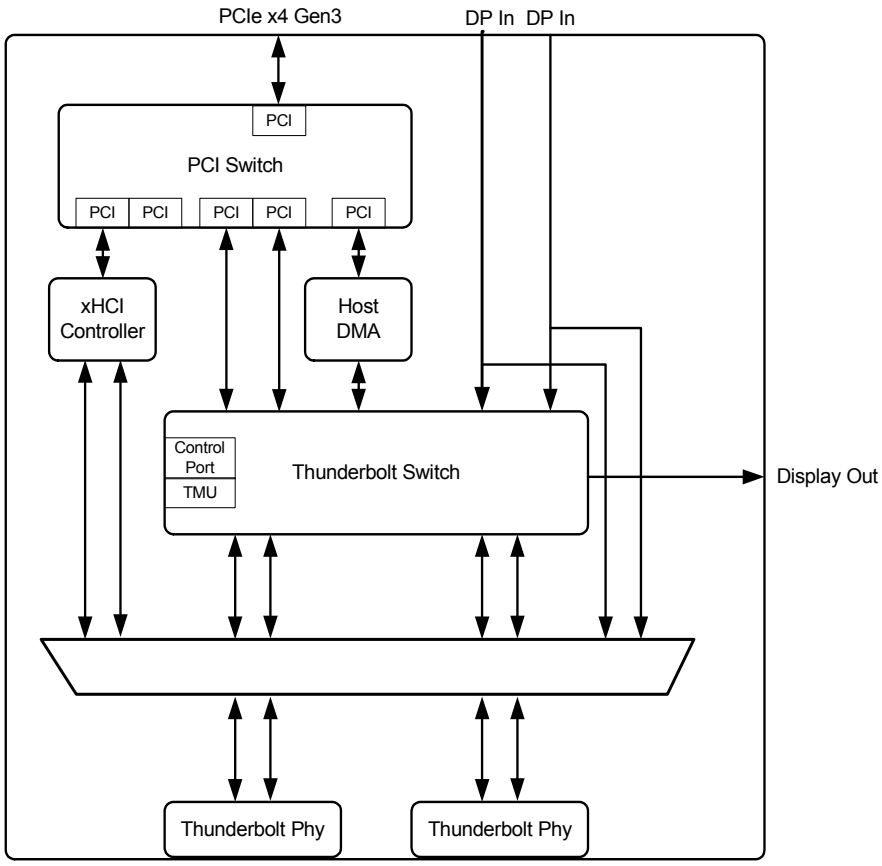
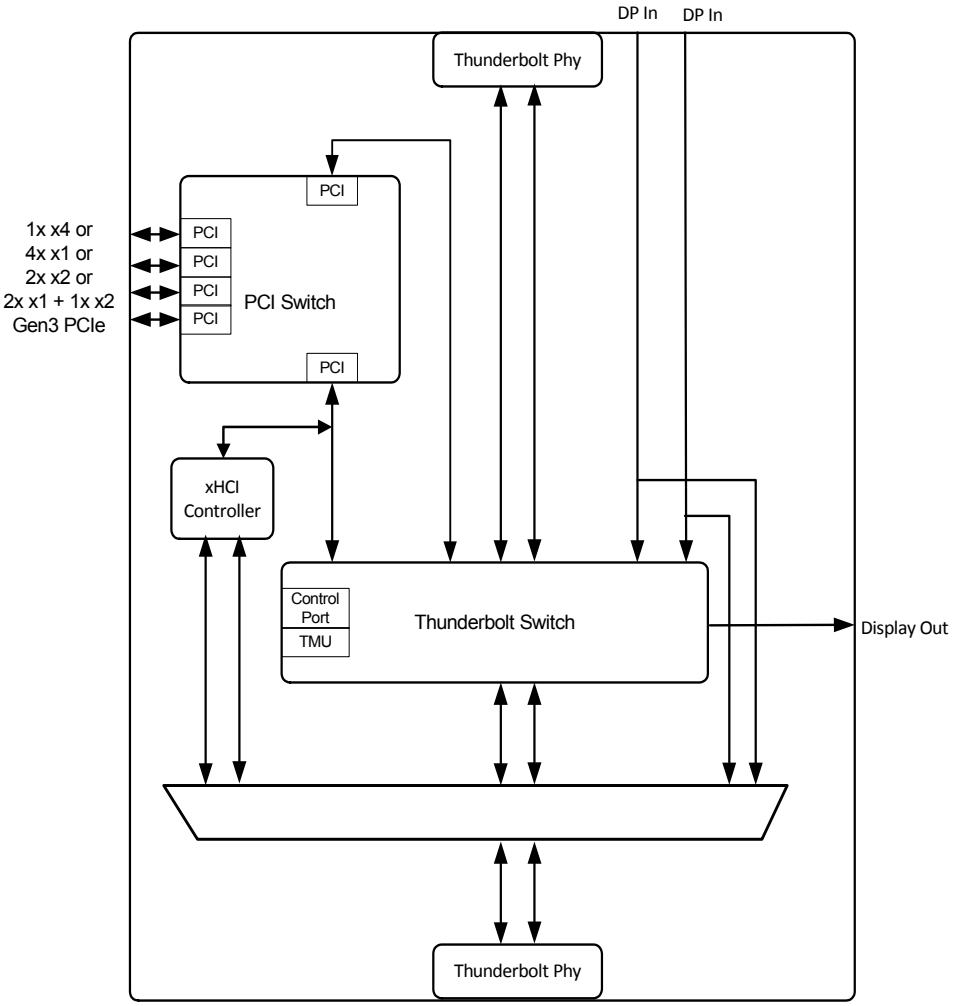


Figure 2. Alpine-Ridge DP Controller Block Diagram (Device view)



1.1 Router/EndPoint Chip Specifications

Alpine-Ridge DP implements the following channels.

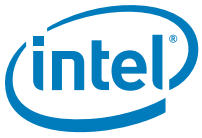
- 2 DisplayPort sink interfaces connected on board or through a cable each one compliant with either:
  - The DisplayPort 1.2 specification for tunneling:
    - 1.62 Gbps or 2.7 Gbps or 5.4 Gbps signaling rate
    - x1, x2 or x4 lane operation
    - Support for HDCP content protection

    OR
  - The DP++ sink in Re-drive mode (not driven to the Thunderbolt cloud)
    - Dual-mode DisplayPort
    - High Bit Rate: 5.4 Gbps
    - Note - this mode works on sink0 only.
- 1 Display Source interface compliant with either:
  - DisplayPort 1.2 specification 1.62 Gbps or 2.7 Gbps or 5.4Gbps signaling rate
  - x1, x2 or x4 lane operation
  - Support for HDCP content protection

    OR
  - DP++ (Dual mode DisplayPort)
  - Support for HDCP content protection
  - 4 lane PCI Express interface
  - PCI Express 3.0 compliant @ 8.0 GT/s
  - In Host Router mode, interface acts as 1 interface
  - In Device mode, interface can be configured to one of the following:
    - 1x4 - One Device of four lanes
    - 4x1 - Four Devices of one lane each
    - 2x2 - Two devices of two lanes each
    - 1x2 + 2x1 - One device of two lanes and two devices of one lane each
  - Each separate link can be Gen3 or Gen2 or Gen1
- 2 USB-C connectors, each one with either:
  - Thunderbolt alternate mode - 2x2 CIO channels:
    - 16 paths per port target
    - Each port streams x2 SERDES with 20.625 Gbps or 10.3125 Gbps signaling rate
    - 16 counters per port

    OR
  - 2 Display Port alternate mode
    - High Bit Rate: 5.4 Gbps

    OR
  - 2x USB3.1 Gen1/Gen2 channel and USB2 channel



    - —Each high speed channel can operate at USB3.1 Gen1 (SS) or Gen2 (SSP)
    - —Each low speed channel can operate at USB HS, FS, LS
  - — 2Multi function DP alternate mode
    - —Host only functionality
- CIO Host Interface:
  - — PCI Express 3.0 compliant endpoint
  - — Supports simultaneous transmit and receive on 16 paths
  - — Raw mode and frame mode operation configurable on a per-path basis
  - — MSI and MSI-X support
  - — Interrupt moderation support
- CIO Time Management Unit (TMU):
  - — Router implements a time synchronization protocol based on 802.1AS
  - — Time accuracy between adjacent routers: 8ns
  - — Hardware support in the form of an input pin to enable the TMU to be slaved to an external Grand Master clock
  - — Hardware support in the form of an output pin to enable the TMU clock to provide time reference to an external device
- 3.3V supply
  - — 7 internal power domains

2.0 Pin Interface

Signal names are subject to change without notice. Verify with your local Intel sales office that you have the latest information before finalizing a design.

2.1 Signal Description

2.1.1 Signal Type Definitions

The signals are electrically defined in Table 1

Table 1. Signal Definitions

Name	Definition
In	Input Pin
Out	Output Pin
I/O	Bi-directional Input / Output Pin
OD O	Open Drain Output Pin
I/OD	Bi-directional Input/Open Drain Output Pin
A-in	Analog input signals
A-out	Analog output signals
A-inout	Bi-directional analog signals
LC	Link Controller power domain
POC	Power on Control power domain
ANA	Analog common power domain
PCIe	PCIe power domain
DP	Display Port power domain
USB	USB power domain

2.1.2 PCIe Interface

Table 2. PCIe Signal and Pin Information

Signal	Pin Number	Type	Power domain	Description
PCIE_RX3_N	H22	A-in		PCIe Receiver Differential Pair Lane 3
PCIE_RX3_P	H23	A-in		PCIe Receiver Differential Pair Lane 3
PCIE_RX2_N	M22	A-in		PCIe Receiver Differential Pair Lane 2
PCIE_RX2_P	M23	A-in		PCIe Receiver Differential Pair Lane 2
PCIE_RX1_N	T22	A-in		PCIe Receiver Differential Pair Lane 1
PCIE_RX1_P	T23	A-in		PCIe Receiver Differential Pair Lane 1
PCIE_RX0_N	Y22	A-in		PCIe Receiver Differential Pair Lane 0
PCIE_RX0_P	Y23	A-in		PCIe Receiver Differential Pair Lane 0

Signal	Pin Number	Type	Power domain	Description
PCIE_TX3_N	F22	A-out		PCIe Transmitter Differential Pair Lane 3
PCIE_TX3_P	F23	A-out		PCIe Transmitter Differential Pair Lane 3
PCIE_TX2_N	K22	A-out		PCIe Transmitter Differential Pair Lane 2
PCIE_TX2_P	K23	A-out		PCIe Transmitter Differential Pair Lane 2
PCIE_TX1_N	P22	A-out		PCIe Transmitter Differential Pair Lane 1
PCIE_TX1_P	P23	A-out		PCIe Transmitter Differential Pair Lane 1
PCIE_TX0_N	V22	A-out		PCIe Transmitter Differential Pair Lane 0
PCIE_TX0_P	V23	A-out		PCIe Transmitter Differential Pair Lane 0
PERST_N	L4	In	POC	PCIE reset (host -input, device -output)
PCIE_CLKREQ_N	AC5	OD O	LC	PCIe CLKREQ

2.1.3 Thunderbolt Ports

Table 3. Thunderbolt Ports Signal and Pin Information

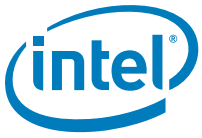
Signal	Pin Number	Type	Power domain	Description
PA_DPSRC_AUX_N	W15	A-inout		Port A : DP Source Aux Channel Differential Pair
PA_DPSRC_AUX_P	Y15	A-inout		Port A : DP Source Aux Channel Differential Pair
PA_RX1_N	B15	A-inout		Port A: TBT Lane 1 Receiver Differential Pair, DP source Main Link 0 Transmitter Differential Pair (In reverse rotation: TBT Lane 0 RX, USB SS RX, DP Source ML 3 TX)
PA_RX1_P	A15	A-inout		Port A: TBT Lane 1 Receiver Differential Pair, DP source Main Link 0 Transmitter Differential Pair (In reverse rotation: TBT Lane 0 RX, USB SS RX, DP Source ML 3 TX)
PA_RX0_N	A21	A-inout		Port A: TBT Lane 0 Receiver Differential Pair, USB SS Receiver Differential Pair, DP Source Main Link 3 Transmitter Differential Pair (In reverse rotation: TBT Lane 1 Rx, DP Source ML 0 TX)
PA_RX0_P	B21	A-inout		Port A: TBT Lane 0 Receiver Differential Pair, USB SS Receiver Differential Pair, DP Source Main Link 3 Transmitter Differential Pair (In reverse rotation: TBT Lane 1 Rx, DP Source ML 0 TX)
PA_TX1_N	B17	A-output		Port A: TBT Lane 1 Transmitter Differential Pair, DP Source Main Link 1Transmitter Differential Pair (In reverse rotation: TBT Lane 0 TX, USB SS TX, DP Source ML 2 TX)
PA_TX1_P	A17	A-output		Port A: TBT Lane 1 Transmitter Differential Pair, DP Source Main Link 1 Transmitter Differential Pair (In reverse rotation: TBT Lane 0 TX, USB SS TX, DP Source ML 2 TX)
PA_TX0_N	B19	A-output		Port A: TBT Lane 0 Transmitter Differential Pair, USB SS Transmitter Differential Pair, DP Source Main Link 2 Transmitter Differential Pair (In reverse rotation: TBT Lane 1 TX, DP Source ML 1 TX)

Signal	Pin Number	Type	Power domain	Description
PA_TX0_P	A19	A-output		Port A: TBT Lane 0 Transmitter Differential Pair, USB SS Transmitter Differential Pair, DP Source Main Link 2 Transmitter Differential Pair (In reverse rotation: TBT Lane 1 TX, DP Source ML 1 TX)
PB_DPSRC_AUX_N	W16	A-inout		Port B : DP Source Aux Channel Differential Pair
PB_DPSRC_AUX_P	Y16	A-inout		Port B : DP Source Aux Channel Differential Pair
PB_RX1_N	A7	A-inout		Port B: TBT Lane 1 Receiver Differential Pair, DP source Main Link 0 Transmitter Differential Pair (In reverse rotation: TBT Lane 0 RX, USB SS RX, DP Source ML 3 TX)
PB_RX1_P	B7	A-inout		Port B: TBT Lane 1 Receiver Differential Pair, DP source Main Link 0 Transmitter Differential Pair (In reverse rotation: TBT Lane 0 RX, USB SS RX, DP Source ML 3 TX)
PB_RX0_N	B13	A-inout		Port B: TBT Lane 0 Receiver Differential Pair, USB SS Receiver Differential Pair, DP Source Main Link 3 Transmitter Differential Pair (In reverse rotation: TBT Lane 1 Rx, DP Source ML 0 TX)
PB_RX0_P	A13	A-inout		Port B: TBT Lane 0 Receiver Differential Pair, USB SS Receiver Differential Pair, DP Source Main Link 3 Transmitter Differential Pair (In reverse rotation: TBT Lane 1 Rx, DP Source ML 0 TX)
PB_TX1_N	B9	A-output		Port B: TBT Lane 1 Transmitter Differential Pair, DP Source Main Link 1 Transmitter Differential Pair (In reverse rotation: TBT Lane 0 TX, USB SS TX, DP Source ML 2 TX)
PB_TX1_P	A9	A-output		Port B: TBT Lane 1 Transmitter Differential Pair, DP Source Main Link 1 Transmitter Differential Pair (In reverse rotation: TBT Lane 0 TX, USB SS TX, DP Source ML 2 TX)
PB_TX0_N	B11	A-output		Port B: TBT Lane 0 Transmitter Differential Pair, USB SS Transmitter Differential Pair, DP Source Main Link 2 Transmitter Differential Pair (In reverse rotation: TBT Lane 1 TX, DP Source ML 1 TX)
PB_TX0_P	A11	A-output		Port B: TBT Lane 0 Transmitter Differential Pair, USB SS Transmitter Differential Pair, DP Source Main Link 2 Transmitter Differential Pair (In reverse rotation: TBT Lane 1 TX, DP Source ML 1 TX)

2.1.4 Display Port

Table 4. Display Port Signal and Pin Information

Signal	Pin Number	Type	Power domain	Description
DPSNK0_ML3_N	AC13	A-in		DP Sink 0 Main Link Receiver Differential Pair Lane 3
DPSNK0_ML3_P	AB13	A-in		DP Sink 0 Main Link Receiver Differential Pair Lane 3
DPSNK0_ML2_N	AC11	A-in		DP Sink 0 Main Link Receiver Differential Pair Lane 2



Signal	Pin Number	Type	Power domain	Description
DPSNK0_ML2_P	AB11	A-in		DP Sink 0 Main Link Receiver Differential Pair Lane 2
DPSNK0_ML1_N	AC9	A-in		DP Sink 0 Main Link Receiver Differential Pair Lane 1
DPSNK0_ML1_P	AB9	A-in		DP Sink 0 Main Link Receiver Differential Pair Lane 1
DPSNK0_ML0_N	AC7	A-in		DP Sink 0 Main Link Receiver Differential Pair Lane 0
DPSNK0_ML0_P	AB7	A-in		DP Sink 0 Main Link Receiver Differential Pair Lane 0
DPSNK0_AUX_N	W11	A-inout		DP Sink 0 Aux Channel Differential Pair
DPSNK0_AUX_P	Y11	A-inout		DP Sink 0 Aux Channel Differential Pair
DPSNK0_DDC_CLK	Y5	I/O	LC	DP sink 0 DDC clock. connect to 2k PU if SRC0 is connected to HDMI or DP++ connector. Otherwise 100k PD.
DPSNK0_DDC_DATA	R4	I/O	LC	DP sink 0 DDC data. connect to 2k PU if SRC0 is connected to HDMI or DP++ connector. Otherwise 100k PD.
DPSNK0_HPD	AA2	Out	LC	Hot plug detect Output from DP Sink 0
DPSNK1_ML3_N	AC21	A-in		DP Sink 1 Main Link Receiver Differential Pair Lane 3
DPSNK1_ML3_P	AB21	A-in		DP Sink 1 Main Link Receiver Differential Pair Lane 3
DPSNK1_ML2_N	AC19	A-in		DP Sink 1 Main Link Receiver Differential Pair Lane 2
DPSNK1_ML2_P	AB19	A-in		DP Sink 1 Main Link Receiver Differential Pair Lane 2
DPSNK1_ML1_N	AC17	A-in		DP Sink 1 Main Link Receiver Differential Pair Lane 1
DPSNK1_ML1_P	AB17	A-in		DP Sink 1 Main Link Receiver Differential Pair Lane 1
DPSNK1_ML0_N	AC15	A-in		DP Sink 1 Main Link Receiver Differential Pair Lane 0
DPSNK1_ML0_P	AB15	A-in		DP Sink 1 Main Link Receiver Differential Pair Lane 0
DPSNK1_AUX_N	W12	A-inout		DP Sink 1 Aux Channel Differential Pair
DPSNK1_AUX_P	Y12	A-inout		DP Sink 1 Aux Channel Differential Pair
DPSNK1_DDC_CLK	Y8	I/O	LC	unused. connect to 100k PD.
DPSNK1_DDC_DATA	N4	I/O	LC	DP sink 0 CONFIG1 signal. connect to 100k PD. If SRC0 support HDMI, connect as GPU's CONFIG1 or to appropriate AUX/DDC mux for SNK0
DPSNK1_HPD	Y6	Out	LC	Hot plug detect Output from DP Sink 1
DPSRC_ML3_N	J1	A-out		DP Source 0 Main Link transmitter Differential Pair Lane 3
DPSRC_ML3_P	J2	A-out		DP Source 0 Main Link transmitter Differential Pair Lane 3
DPSRC_ML2_N	L1	A-out		DP Source 0 Main Link transmitter Differential Pair Lane 2
DPSRC_ML2_P	L2	A-out		DP Source 0 Main Link transmitter Differential Pair Lane 2
DPSRC_ML1_N	N1	A-out		DP Source 0 Main Link transmitter Differential Pair Lane 1

Signal	Pin Number	Type	Power domain	Description
DPSRC_ML1_P	N2	A-out		DP Source 0 Main Link transmitter Differential Pair Lane 1
DPSRC_ML0_N	R1	A-out		DP Source 0 Main Link transmitter Differential Pair Lane 0
DPSRC_ML0_P	R2	A-out		DP Source 0 Main Link transmitter Differential Pair Lane 0
DPSRC_AUX_N	Y19	A-inout		DP Source 0 Aux Channel Differential Pair
DPSRC_AUX_P	W19	A-inout		DP Source 0 Aux Channel Differential Pair
DPSRC_HPD	G1	I/O	LC	Hot plug detect Input

2.1.5 USB Interface

Table 5. USB Signal and Pin Information

Signal	Pin Number	Type	Power domain	Description
PA_USB2_D_N	D20	A-inout		Port A: USB2 Differential Pair
PA_USB2_D_P	E20	A-inout		Port A: USB2 Differential Pair
PB_USB2_D_N	D19	A-inout		Port B: USB2 Differential Pair
PB_USB2_D_P	E19	A-inout		Port B: USB2 Differential Pair

2.1.6 JTAG Interface

Table 6. JTAG and TEST Signal and Pin Information

Signal	Pin Number	Type	Power domain	Description
TDI	Y4	In	LC	JTAG Test Data Input
TMS	V4	In	LC	JTAG Test Mode Select
TCK	T4	In	LC	JTAG Test Clock
TDO	W4	OD O	LC	JTAG Test Data Output
TEST_EN	E1	In	POC	Test Enable (Connected to GND on func Board)
TEST_PWR_GOOD	AB5	In	LC	Add an external 100 OHm to GND
USB2_ATEST	E18	A-out		Testability for US2B analog
PCIE_ATEST	V18	A-out		Testability for PCIE analog
MONDC_SVR	D6	A-inout		Force/monitor options in the SVR analog
MONDC_DPSRC	AB2	A-inout		Force/monitor options in the DPSRC analog
MONDC_DPSNK_1	W18	A-inout		Force/monitor options in the DPSNK analog
MONDC_DPSNK_0	W13	A-inout		Force/monitor options in the DPSNK analog
MONDC_CIO_1	C22	A-inout		Force/monitor options in the CIO analog
MONDC_CIO_0	C23	A-inout		Force/monitor options in the CIO analog
ATEST_P	A23	A-out		Testability for analog
ATEST_N	B23	A-out		Testability for analog

2.1.7 Flash Memory Interface

Table 7. Flash Memory Signal and Pin Information

Signal	Pin Number	Type	Power domain	Description
EE_DI	AB3	Out	LC	Data in to Flash device
EE_DO	AC4	In	LC	Data out from FLASH device

Signal	Pin Number	Type	Power domain	Description
EE_CS_N	AC3	Out	LC	FLASH chip select
EE_CLK	AB4	Out	LC	FLASH clock

2.1.8 Clocks

Table 8. Clocks Signal and Pin Information

Signal	Pin Number	Type	Power domain	Description
PCIE_REFCLK_100_IN_N	T19	A-in		100 MHz Ref Clock for both CIO and PCIe sub-units
PCIE_REFCLK_100_IN_P	V19	A-in		100 MHz Ref Clock for both CIO and PCIe sub-units
XTAL_25_IN	D22	A-in		Input clock 25 MHz
XTAL_25_OUT	D23	A-inout		Output 25 MHz clock in XTal mode, Input in external differential clock mode

2.1.9 Miscellaneous

Table 9. Miscellaneous Signal and Pin Information

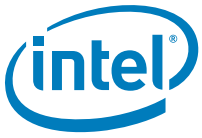
Signal	Pin Number	Type	Power domain	Description
POC_GPIO_0	J4	I/O	POC	Host/Device: pa_pps_int_n (input) - interrupt from port power switch
POC_GPIO_1	E2	I/O	POC	Host/Device: pb_pps_int_n (input) - interrupt from port power switch
POC_GPIO_2	D4	I/O	POC	Host: rtd3_usb_pwr_en (input) - rtd3 power enable for USB mode Device: reserved
POC_GPIO_3	H4	I/O	POC	Host/Device: force_pwr (input) - force full power on
POC_GPIO_4	F2	I/O	POC	Host: batlow_n (input) - battery low indication Device: wake_n (input) - pcie wake_n
POC_GPIO_5	D2	I/O	POC	Host: slp_s3_n (input) - slp_s3 system indication Device: pm_s0_en (output) - device s0 indication
POC_GPIO_6	F1	I/O	POC	Host: rtd3_cio_pwr_en (input) - rtd3 power enable for cio mode Device: pm_s3_en (output) - device s3 indication
GPIO_0	U1	I/O	LC	Host/Device: i2c_master_data (inout) - i2c master data
GPIO_1	U2	I/O	LC	Host/Device: i2c_master_clock (inout) - i2c master clock
GPIO_2	V1	I/O	LC	Host/Device: ee_wp_n (output) - flash write protect
GPIO_3	V2	I/O	LC	Host: reserved Device: tmu_clk_out (output) - tmu clock output

Signal	Pin Number	Type	Power domain	Description
GPIO_4	W1	I/O	LC	Host: wake_n (output) - pcie wake_n Device: pcie_device_rst_1_n - pcie device 1 reset
GPIO_5	W2	I/O	LC	Host: cio_plug_event_n (output) - hot plug indication Device: pcie_device_rst_2_n - pcie device 2 reset
GPIO_6	Y1	I/O	LC	Host: src0_ddc_data (inout) - src0 ddc data Device: pcie_device_rst_3_n - pcie device 3 reset
GPIO_7	Y2	I/O	LC	Host: src0_ddc_clk (inout) - src0 ddc clock Device: reserved
GPIO_8	AA1	I/O	LC	Host/Device: src0_cfg1 (input) - src0 config1 from dpp connector
RESET_N	F4	I/O	POC	Main power reset signal
RBIAS	H6	A-in		External resistor for CIO Resistor value 4.75KOhm +/- 0.5%
RSENSE	J6	A-in		External resistor for CIO/PE Resistor value 4.75KOhm +/- 0.5%
PCIE_RBIAS	N16	A-in		External resistor for pcie. Resistor value 3.01KOhm +/- 1%
DPSNK_RBIAS	Y18	A-in		External resistor for DPSNK Resistor value 14K +/- 1%
DPSRC_RBIAS	N6	A-in		External resistor for DPSRC Resistor value 14K +/- 1%
TEST_EDM	AC1	In		Testability signal, connect to GND
PB_USB2_RBIAS	F19	A-in		External resistor for USB2 Resistor value 499 Ohm +/- 1%
PB_DPSRC_HPD	G2	I	POC	Port B: DP Source HPD (Hot Plug Detect) input
PB_LSRX	B5	I	POC	Port B: TBT LSRX
PB_LSTX	B4	I/O	POC	Port B: TBT LSTX
PA_USB2_RBIAS	H19	A-in		External resistor for USB2 Resistor value 499 Ohm +/- 1%
PA_DPSRC_HPD	M4	I	POC	Port A: DP Source HPD (Hot Plug Detect) input
PA_LSRX	A4	I	POC	Port A: TBT LSRX
PA_LSTX	A5	I/O	POC	Port A: TBT LSTX
THERMDA	AB23, AC23	A-out	LC	Thermal Diode pin (anode)

2.1.10 Power and Ground

Table 10. Power and Ground Signals

Name	Pin number	Description
VCC3P3_SX	F8	VCC 3.3v Power in SX mode
VCC3P3_S0	R13	VCC 3.3v main Power
VCC3P3_LC	R6	VCC 3.3v for LC domain, can be used for FLASH. Total capacitance on this pins must not exceed 1uF.



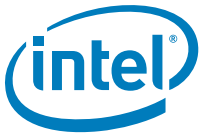
Name	Pin number	Description
VCC3P3A	H9	VCC 3.3v for SVR
VCC3P3_SVR	A2, A3, B3	VCC 3.3v from SVR
SVR_IND	C1, C2, D1	Connect via inductor to VCC0P9_SVR_SENSE
FUSE_VQPS_64	L15	Testability signal, connect to GND
FUSE_VQPS_128	N15	Testability signal, connect to GND
VCC3P3_ANA_USB2	J16	VCC 3.3v for USB2 analog
VCC3P3_ANA_PCIE	L16	VCC 3.3v for PCIE analog
VCC0P9_SVR_SENSE	J9	VCC 0.9v feedback to SVR
VCC0P9_PCIE	M13, M15, M16	VCC 0.9v for PCIE domain
VCC0P9_CIO	R11, R12, R8, R9	VCC 0.9v for CIO domain
VCC0P9_ANA_PCIE_2	L18, M18, N18	VCC 0.9v for PCIE analog
VCC0P9_ANA_PCIE_1	L19, N19	VCC 0.9v for PCIE analog
VCC0P9_ANA_DPSRC	L6, M6	VCC 0.9v for DPSRC analog
VCC0P9_ANA_DPSNK	V11, V12, V13	VCC 0.9v for DPSNK analog
VCC0P9_LVR	F18, H18, J11	VCC 0.9v from LVR
VCC0P9_LVR_SENSE	H11	Connect to VCC0P9_SVR
VCC0P9_SVR_ANA	E12, E13, F11, F12, F13, F15	VCC 0.9v for ana_common domain
VCC0P9_SVR	L9, M9	VCC 0.9v from SVR
VCC0P9_DP	L11, L12, L8, M8, T11, T12	VCC 0.9v for DP domain
VCC0P9_USB	R15, R16	VCC 0.9v for USB domain
SVR_VSS	A1, B1, B2	VSS for SVR
VSS	AB1, AC2, D5, E4, E5, E6, F5, F6, H5, H8, J12, J13, J15, J8, L13, M11, M12, N11, N12, N13, N8, N9, T13, T15, T16, T18, T6, T8, T9	VSS for digital
VSS_ANA	A10, A12, A14, A16, A18, A20, A22, A6, A8, AA22, AA23, AB10, AB12, AB14, AB16, AB18, AB20, AB22, AB6, AB8, AC10, AC12, AC14, AC16, AC18, AC20, AC22, AC6, AC8, B10, B12, B14, B16, B18, B20, B22, B6, B8, D11, D12, D13, D15, D16, D18, D8, D9, E11, E15, E16, E22, E23, E8, E9, F16, F20, F9, G22, G23, H1, H12, H13, H15, H16, H2, H20, J18, J19, J20, J22, J23, J5, K1, K2, L20, L22, L23, L5, M1, M19, M2, ,M20 ,M5, N20, N22, N23, N5, P1, P2, R18, R19, R20, R22, R23, R5, T1, T2, T20, T5, U22, U23, V15, V16, V20, V5, V6, V8, V9, W20, W22, W23, W5 ,W6, W8, W9, Y13, Y20, Y9	VSS for analog

2.1.11 Alphabetical Pinout/Signal Name

Table 11. Signal Name Associated with Each Pin

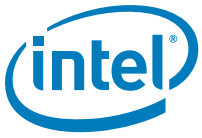
Pin Name	Signal Name	Pin Name	Signal Name
A1	SVR_VSS	H6	RBIAS
A10	VSS_ANA	H8	VSS
A11	PB_TX0_P	H9	VCC3P3A
A12	VSS_ANA	J1	DPSRC_ML3_N

Pin Name	Signal Name	Pin Name	Signal Name
A13	PB_RX0_P	J11	VCC0P9_LVR
A14	VSS_ANA	J12	VSS
A15	PA_RX1_P	J13	VSS
A16	VSS_ANA	J15	VSS
A17	PA_TX1_P	J16	VCC3P3_ANA_USB2
A18	VSS_ANA	J18	VSS_ANA
A19	PA_TX0_P	J19	VSS_ANA
A2	VCC3P3_SVR	J2	DPSRC_ML3_P
A20	VSS_ANA	J20	VSS_ANA
A21	PA_RX0_N	J22	VSS_ANA
A22	VSS_ANA	J23	VSS_ANA
A23	ATEST_P	J4	POC_GPIO_0
A3	VCC3P3_SVR	J5	VSS_ANA
A4	PA_LSRX	J6	RSENSE
A5	PA_LSTX	J8	VSS
A6	VSS_ANA	J9	VCC0P9_SVR_SENSE
A7	PB_RX1_N	K1	VSS_ANA
A8	VSS_ANA	K2	VSS_ANA
A9	PB_TX1_P	K22	PCIE_TX2_N
AA1	GPIO_8	K23	PCIE_TX2_P
AA2	DPSNK0_HPD	L1	DPSRC_ML2_N
AA22	VSS_ANA	L11	VCC0P9_DP
AA23	VSS_ANA	L12	VCC0P9_DP
AB1	VSS	L13	VSS
AB10	VSS_ANA	L15	FUSE_VQPS_64
AB11	DPSNK0_ML2_P	L16	VCC3P3_ANA_PCIE
AB12	VSS_ANA	L18	VCC0P9_ANA_PCIE_2
AB13	DPSNK0_ML3_P	L19	VCC0P9_ANA_PCIE_1
AB14	VSS_ANA	L2	DPSRC_ML2_P
AB15	DPSNK1_ML0_P	L20	VSS_ANA
AB16	VSS_ANA	L22	VSS_ANA
AB17	DPSNK1_ML1_P	L23	VSS_ANA
AB18	VSS_ANA	L4	PERST_N
AB19	DPSNK1_ML2_P	L5	VSS_ANA
AB2	MONDC_DPSRC	L6	VCC0P9_ANA_DPSRC
AB20	VSS_ANA	L8	VCC0P9_DP
AB21	DPSNK1_ML3_P	L9	VCC0P9_SVR
AB22	VSS_ANA	M1	VSS_ANA
AB23	THERMDA	M11	VSS
AB3	EE_DI	M12	VSS



Pin Name	Signal Name	Pin Name	Signal Name
AB4	EE_CLK	M13	VCC0P9_PCIE
AB5	TEST_PWR_GOOD	M15	VCC0P9_PCIE
AB6	VSS_ANA	M16	VCC0P9_PCIE
AB7	DPSNK0_ML0_P	M18	VCC0P9_ANA_PCIE_2
AB8	VSS_ANA	M19	VSS_ANA
AB9	DPSNK0_ML1_P	M2	VSS_ANA
AC1	TEST_EDM	M20	VSS_ANA
AC10	VSS_ANA	M22	PCIE_RX2_N
AC11	DPSNK0_ML2_N	M23	PCIE_RX2_P
AC12	VSS_ANA	M4	PA_DPSRC_HPD
AC13	DPSNK0_ML3_N	M5	VSS_ANA
AC14	VSS_ANA	M6	VCC0P9_ANA_DPSRC
AC15	DPSNK1_ML0_N	M8	VCC0P9_DP
AC16	VSS_ANA	M9	VCC0P9_SVR
AC17	DPSNK1_ML1_N	N1	DPSRC_ML1_N
AC18	VSS_ANA	N11	VSS
AC19	DPSNK1_ML2_N	N12	VSS
AC2	VSS	N13	VSS
AC20	VSS_ANA	N15	FUSE_VQPS_128
AC21	DPSNK1_ML3_N	N16	PCIE_RBIAS
AC22	VSS_ANA	N18	VCC0P9_ANA_PCIE_2
AC23	THERMDA	N19	VCC0P9_ANA_PCIE_1
AC3	EE_CS_N	N2	DPSRC_ML1_P
AC4	EE_DO	N20	VSS_ANA
AC5	PCIE_CLKREQ_N	N22	VSS_ANA
AC6	VSS_ANA	N23	VSS_ANA
AC7	DPSNK0_ML0_N	N4	DPSNK1_DDC_DATA
AC8	VSS_ANA	N5	VSS_ANA
AC9	DPSNK0_ML1_N	N6	DPSRC_RBIAS
B1	SVR_VSS	N8	VSS
B10	VSS_ANA	N9	VSS
B11	PB_TX0_N	P1	VSS_ANA
B12	VSS_ANA	P2	VSS_ANA
B13	PB_RX0_N	P22	PCIE_TX1_N
B14	VSS_ANA	P23	PCIE_TX1_P
B15	PA_RX1_N	R1	DPSRC_ML0_N
B16	VSS_ANA	R11	VCC0P9_CIO
B17	PA_TX1_N	R12	VCC0P9_CIO
B18	VSS_ANA	R13	VCC3P3_S0
B19	PA_TX0_N	R15	VCC0P9_USB

Pin Name	Signal Name	Pin Name	Signal Name
B2	SVR_VSS	R16	VCC0P9_USB
B20	VSS_ANA	R18	VSS_ANA
B21	PA_RX0_P	R19	VSS_ANA
B22	VSS_ANA	R2	DPSRC_ML0_P
B23	ATEST_N	R20	VSS_ANA
B3	VCC3P3_SVR	R22	VSS_ANA
B4	PB_LSTX	R23	VSS_ANA
B5	PB_LSRX	R4	DPSNK0_DDC_DATA
B6	VSS_ANA	R5	VSS_ANA
B7	PB_RX1_P	R6	VCC3P3_LC
B8	VSS_ANA	R8	VCC0P9_CIO
B9	PB_TX1_N	R9	VCC0P9_CIO
C1	SVR_IND	T1	VSS_ANA
C2	SVR_IND	T11	VCC0P9_DP
C22	MONDC_CIO_1	T12	VCC0P9_DP
C23	MONDC_CIO_0	T13	VSS
D1	SVR_IND	T15	VSS
D11	VSS_ANA	T16	VSS
D12	VSS_ANA	T18	VSS
D13	VSS_ANA	T19	PCIE_REFCLK_100_IN_N
D15	VSS_ANA	T2	VSS_ANA
D16	VSS_ANA	T20	VSS_ANA
D18	VSS_ANA	T22	PCIE_RX1_N
D19	PB_USB2_D_N	T23	PCIE_RX1_P
D2	POC_GPIO_5	T4	TCK
D20	PA_USB2_D_N	T5	VSS_ANA
D22	XTAL_25_IN	T6	VSS
D23	XTAL_25_OUT	T8	VSS
D4	POC_GPIO_2	T9	VSS
D5	VSS	U1	GPIO_0
D6	MONDC_SVR	U2	GPIO_1
D8	VSS_ANA	U22	VSS_ANA
D9	VSS_ANA	U23	VSS_ANA
E1	TEST_EN	V1	GPIO_2
E11	VSS_ANA	V11	VCC0P9_ANA_DPSNK
E12	VCC0P9_SVR_ANA	V12	VCC0P9_ANA_DPSNK
E13	VCC0P9_SVR_ANA	V13	VCC0P9_ANA_DPSNK
E15	VSS_ANA	V15	VSS_ANA
E16	VSS_ANA	V16	VSS_ANA
E18	USB2_ATEST	V18	PCIE_ATEST

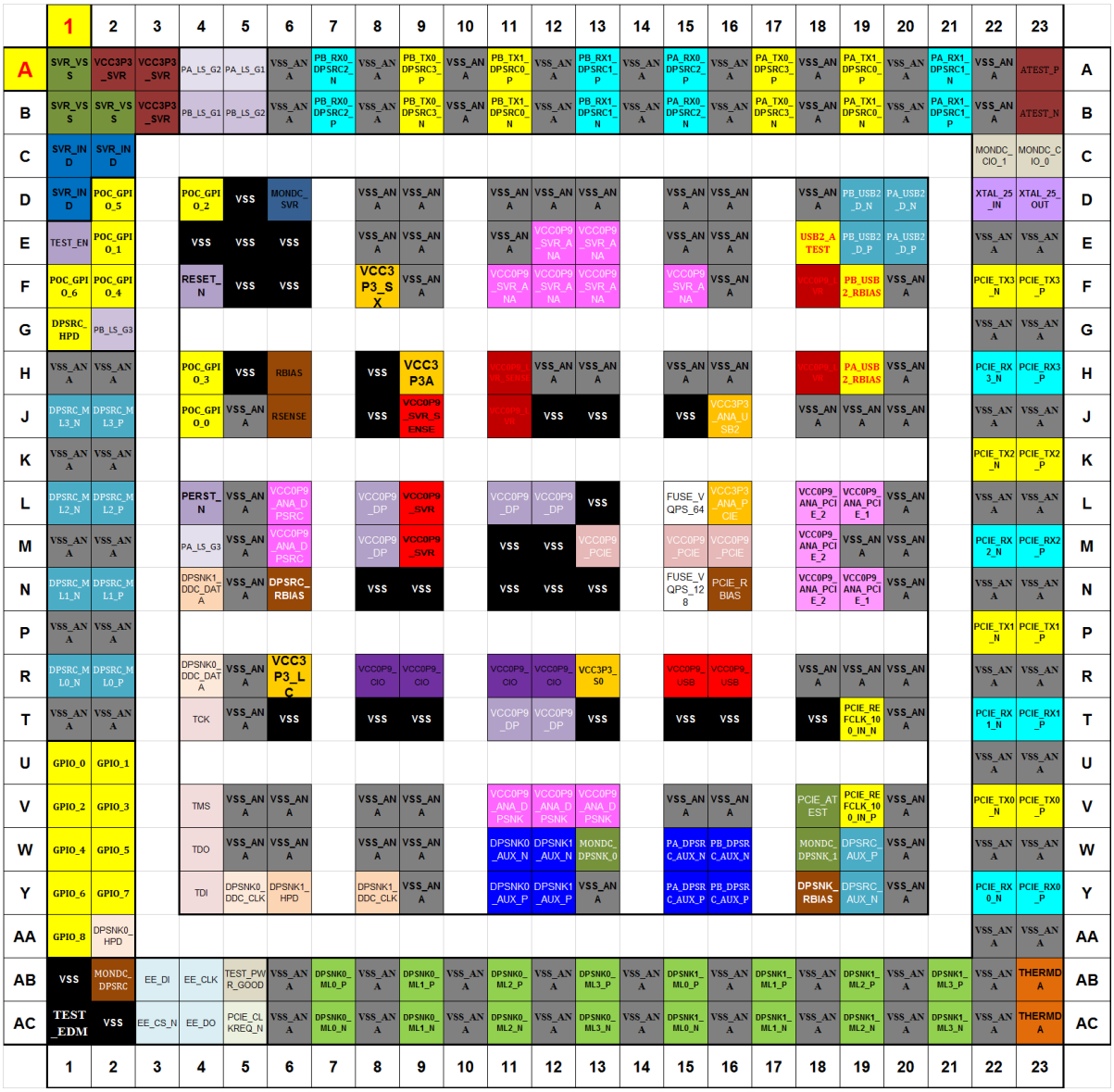


Pin Name	Signal Name	Pin Name	Signal Name
E19	PB_USB2_D_P	V19	PCIE_REFCLK_100_IN_P
E2	POC_GPIO_1	V2	GPIO_3
E20	PA_USB2_D_P	V20	VSS_ANA
E22	VSS_ANA	V22	PCIE_TX0_N
E23	VSS_ANA	V23	PCIE_TX0_P
E4	VSS	V4	TMS
E5	VSS	V5	VSS_ANA
E6	VSS	V6	VSS_ANA
E8	VSS_ANA	V8	VSS_ANA
E9	VSS_ANA	V9	VSS_ANA
F1	POC_GPIO_6	W1	GPIO_4
F11	VCC0P9_SVR_ANA	W11	DPSNK0_AUX_N
F12	VCC0P9_SVR_ANA	W12	DPSNK1_AUX_N
F13	VCC0P9_SVR_ANA	W13	MONDC_DPSNK_0
F15	VCC0P9_SVR_ANA	W15	PA_DPSRC_AUX_N
F16	VSS_ANA	W16	PB_DPSRC_AUX_N
F18	VCC0P9_LVR	W18	MONDC_DPSNK_1
F19	PB_USB2_RBIAS	W19	DPSRC_AUX_P
F2	POC_GPIO_4	W2	GPIO_5
F20	VSS_ANA	W20	VSS_ANA
F22	PCIE_TX3_N	W22	VSS_ANA
F23	PCIE_TX3_P	W23	VSS_ANA
F4	RESET_N	W4	TDO
F5	VSS	W5	VSS_ANA
F6	VSS	W6	VSS_ANA
F8	VCC3P3_SX	W8	VSS_ANA
F9	VSS_ANA	W9	VSS_ANA
G1	DPSRC_HPD	Y1	GPIO_6
G2	PB_DPSRC_HPD	Y11	DPSNK0_AUX_P
G22	VSS_ANA	Y12	DPSNK1_AUX_P
G23	VSS_ANA	Y13	VSS_ANA
H1	VSS_ANA	Y15	PA_DPSRC_AUX_P
H11	VCC0P9_LVR_SENSE	Y16	PB_DPSRC_AUX_P
H12	VSS_ANA	Y18	DPSNK_RBIAS
H13	VSS_ANA	Y19	DPSRC_AUX_N
H15	VSS_ANA	Y2	GPIO_7
H16	VSS_ANA	Y20	VSS_ANA
H18	VCC0P9_LVR	Y22	PCIE_RX0_N
H19	PA_USB2_RBIAS	Y23	PCIE_RX0_P
H2	VSS_ANA	Y4	TDI

Pin Name	Signal Name	Pin Name	Signal Name
H20	VSS_ANA	Y5	DPSNK0_DDC_CLK
H22	PCIE_RX3_N	Y6	DPSNK1_HPD
H23	PCIE_RX3_P	Y8	DPSNK1_DDC_CLK
H4	POC_GPIO_3	Y9	VSS_ANA
H5	VSS		

Figure 3 shows the pin assignments for the package. This is a top view, looking from the die to the PCB.

Figure 3. Alpine-Ridge DP Pin Map



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
A	SVR_VSS	VCC3P3_SVR	VCC3P3_SVR	PA_LS_G2	PA_LS_G1	VSS_ANA	PB_RX0_DPSRC2_N	VSS_ANA	PB_TX0_DPSRC3_P	VSS_ANA	PB_TX1_DPSRC0_P	VSS_ANA	PB_RX1_DPSRC1_P	VSS_ANA	PA_RX0_DPSRC2_P	VSS_ANA	PA_TX0_DPSRC3_P	VSS_ANA	PA_TX1_DPSRC0_P	VSS_ANA	PA_RX1_DPSRC1_N	VSS_ANA	ATEST_P	A
B	SVR_VSS	SVR_VSS	VCC3P3_SVR	PB_LS_G1	PB_LS_G2	VSS_ANA	PB_RX0_DPSRC2_P	VSS_ANA	PB_TX0_DPSRC3_N	VSS_ANA	PB_TX1_DPSRC0_N	VSS_ANA	PB_RX1_DPSRC1_N	VSS_ANA	PA_RX0_DPSRC2_N	VSS_ANA	PA_TX0_DPSRC3_N	VSS_ANA	PA_TX1_DPSRC0_N	VSS_ANA	PA_RX1_DPSRC1_P	VSS_ANA	ATEST_N	B
C	SVR_IND	SVR_IND																				MONDC_CIO_1	MONDC_CIO_0	C
D	SVR_IND	POC_GPIO_5		POC_GPIO_2	VSS	MONDC_SVR		VSS_ANA	VSS_ANA		VSS_ANA	VSS_ANA	VSS_ANA		VSS_ANA	VSS_ANA		VSS_ANA	PB_USB2_D_N	PA_USB2_D_N		XTAL_25_IN	XTAL_25_OUT	D
E	TEST_EN	POC_GPIO_1		VSS	VSS	VSS		VSS_ANA	VSS_ANA		VSS_ANA	VCC0P9_SVR_ANA	VCC0P9_SVR_ANA		VSS_ANA	VSS_ANA		USB2_ATEST	PB_USB2_D_P	PA_USB2_D_P		VSS_ANA	VSS_ANA	E
F	POC_GPIO_6	POC_GPIO_4		RESET_N	VSS	VSS		VCC3P3_SX	VSS_ANA		VCC0P9_SVR_ANA	VCC0P9_SVR_ANA	VCC0P9_SVR_ANA		VCC0P9_SVR_ANA	VSS_ANA		VCC0P9_VR	PB_USB2_RBIAS	VSS_ANA		PCIE_TX3_N	PCIE_TX3_P	F
G	DPSRC_HPD	PB_LS_G3																				VSS_ANA	VSS_ANA	G
H	VSS_ANA	VSS_ANA		POC_GPIO_3	VSS	RBIAS		VSS	VCC3P3A		VCC0P9_VR_SENS	VSS_ANA	VSS_ANA		VSS_ANA	VSS_ANA		VCC0P9_VR	PA_USB2_RBIAS	VSS_ANA		PCIE_RX3_N	PCIE_RX3_P	H
J	DPSRC_ML3_N	DPSRC_ML3_P		POC_GPIO_0	VSS_ANA	RSENSE		VSS	VCC0P9_SVR_SENSE		VCC0P9_VR	VSS	VSS		VSS	VCC3P3_ANA_USB2		VSS_ANA	VSS_ANA	VSS_ANA		VSS_ANA	VSS_ANA	J
K	VSS_ANA	VSS_ANA																				PCIE_TX2_N	PCIE_TX2_P	K
L	DPSRC_ML2_N	DPSRC_ML2_P		PERST_N	VSS_ANA	VCC0P9_ANA_DPSRC		VCC0P9_DP	VCC0P9_SVR		VCC0P9_DP	VCC0P9_DP	VSS		FUSE_VQPS_64	VCC3P3_ANA_PCIE		VCC0P9_ANA_PCIE_2	VCC0P9_ANA_PCIE_1	VSS_ANA		VSS_ANA	VSS_ANA	L
M	VSS_ANA	VSS_ANA		PA_LS_G3	VSS_ANA	VCC0P9_ANA_DPSRC		VCC0P9_DP	VCC0P9_SVR		VSS	VSS	VCC0P9_PCIE		VCC0P9_PCIE	VCC0P9_PCIE		VCC0P9_ANA_PCIE_2	VSS_ANA	VSS_ANA		PCIE_RX2_N	PCIE_RX2_P	M
N	DPSRC_ML1_N	DPSRC_ML1_P		DPSNK1_DDC_DATA	VSS_ANA	DPSRC_RBIAS		VSS	VSS		VSS	VSS	VSS		FUSE_VQPS_128	PCIE_RBIAS		VCC0P9_ANA_PCIE_2	VCC0P9_ANA_PCIE_1	VSS_ANA		VSS_ANA	VSS_ANA	N
P	VSS_ANA	VSS_ANA																				PCIE_TX1_N	PCIE_TX1_P	P
R	DPSRC_ML0_N	DPSRC_ML0_P		DPSNK0_DDC_DATA	VSS_ANA	VCC3P3_LC		VCC0P9_CIO	VCC0P9_CIO		VCC0P9_CIO	VCC0P9_CIO	VCC3P3_50		VCC0P9_USB	VCC0P9_USB		VSS_ANA	VSS_ANA	VSS_ANA		VSS_ANA	VSS_ANA	R
T	VSS_ANA	VSS_ANA		TCK	VSS_ANA	VSS		VSS	VSS		VCC0P9_DP	VCC0P9_DP	VSS		VSS	VSS		VSS	PCIE_REFCLK_100_IN_N	VSS_ANA		PCIE_RX1_N	PCIE_RX1_P	T
U	GPIO_0	GPIO_1																				VSS_ANA	VSS_ANA	U
V	GPIO_2	GPIO_3		TMS	VSS_ANA	VSS_ANA		VSS_ANA	VSS_ANA		VCC0P9_ANA_DPSNK	VCC0P9_ANA_DPSNK	VCC0P9_ANA_DPSNK		VSS_ANA	VSS_ANA		PCIE_ATEST	PCIE_REFCLK_100_IN_P	VSS_ANA		PCIE_TX0_N	PCIE_TX0_P	V
W	GPIO_4	GPIO_5		TDO	VSS_ANA	VSS_ANA		VSS_ANA	VSS_ANA		DPSNK0_AUX_N	DPSNK1_AUX_N	MONDC_DPSNK_0		PA_DPSRC_AUX_N	PB_DPSRC_AUX_N		MONDC_DPSNK_1	DPSRC_AUX_P	VSS_ANA		VSS_ANA	VSS_ANA	W
Y	GPIO_6	GPIO_7		TDI	DPSNK0_DDC_CLK	DPSNK1_HPD		DPSNK1_DDC_CLK	VSS_ANA		DPSNK0_AUX_P	DPSNK1_AUX_P	VSS_ANA		PA_DPSRC_AUX_P	PB_DPSRC_AUX_P		DPSNK_RBIAS	DPSRC_AUX_N	VSS_ANA		PCIE_RX0_N	PCIE_RX0_P	Y
AA	GPIO_8	DPSNK0_HPD																				VSS_ANA	VSS_ANA	AA
AB	VSS	MONDC_DPSRC	EE_DI	EE_CLK	TEST_PWR_GOOD	VSS_ANA	DPSNK0_ML0_P	VSS_ANA	DPSNK0_ML1_P	VSS_ANA	DPSNK0_ML2_P	VSS_ANA	DPSNK0_ML3_P	VSS_ANA	DPSNK1_ML0_P	VSS_ANA	DPSNK1_ML1_P	VSS_ANA	DPSNK1_ML2_P	VSS_ANA	DPSNK1_ML3_P	VSS_ANA	THERMDA	AB
AC	TEST_EDM	VSS	EE_CS_N	EE_DO	PCIE_CLKREQ_N	VSS_ANA	DPSNK0_ML0_N	VSS_ANA	DPSNK0_ML1_N	VSS_ANA	DPSNK0_ML2_N	VSS_ANA	DPSNK0_ML3_N	VSS_ANA	DPSNK1_ML0_N	VSS_ANA	DPSNK1_ML1_N	VSS_ANA	DPSNK1_ML2_N	VSS_ANA	DPSNK1_ML3_N	VSS_ANA	THERMDA	AC
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	

3.0 Flash Memory

3.1 Flash Types Supported

Table 12. Supported types of Flash Memory

Manufacturer	Type	Volume, Mbit	Supply, V
AMIC	A25L080	8.0	3.0-3.6
Spansion	S25FL208K	8.0	2.7-3.6
Winbond	W25Q80DV	8.0	2.7-3.6
Matronix	MX25R8035FM2IHH	8.0	2.3-3.6

Additional requirements:

- At least 50.0 MHz clock rate support
- 3.3 V operating voltage
- 4KB sector size
- Minimum instruction set list required:
    - 0x06 - Write Enable (WREN)
    - 0x04 - Write Disable (WRDI)
    - 0x05 – Read Status Register (RDSR)
    - 0x0B – Fast Read (FR)
    - 0x02 – Page Program (PP)
    - 0x20 – Sector Erase (SE)

3.2 Flash Memory Map

The Alpine-Ridge DP uses flash memory for initialization of various internal parameters, enable/ disable bits, analog modules configuration, and internal microcontrollers' ucode patches.

The flash memory map is divided into sections, which are contiguous and expected in the defined order. Each section starts with a length (length units are different for each section) and is followed by data.

The flash memory map is described in Figure 4 and Table 13.

Figure 4. Flash Content Structure

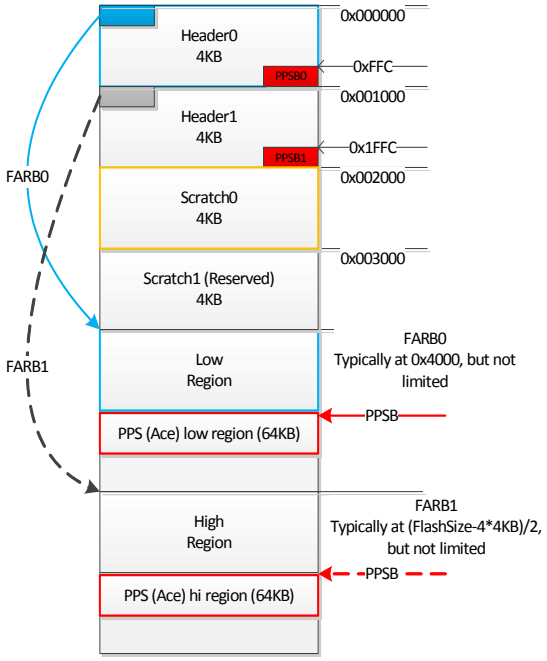


Table 13. Flash Memory Map

ADDRESS, B	DATA	COMMENT
0x000000	FARB0	Flash Active Region Base Pointer 0 – contains **Digital_Base_Pointer** (if doesn't equal to 0x000000 or 0xFFFFFF)
0x000004…..	Security FW	If security enabled – Security FW
0x1FFC	PPSB0	Pointer to PPS section in relative active region
0x001000	FARB1	Flash Active Region Base Pointer 1 – contains **Digital_Base_Pointer** (if doesn't exist FARB1 or doesn't equal to 0x000000 or 0xFFFFFF)
0x001004…..	Security FW	If security enabled – Security FW
0x2FFC	PPSB1	Pointer to PPS section in relative active region
0x2000	Scratch_region_0 (4KB)	Scratch section
0x3000	Scratch_region_1 (4KB)	Scratch section
Digital_Base_Pointer = FARB0/FARB1	Digital section Size Byte 0	Contains **Digital_section_Size[7:0]** (Digital Section Size)
Digital_Base_Pointer + 1	Digital section Size Byte 1	Contains **Digital_section_Size[15:8]** (Digital Section Size)
Digital_Base_Pointer + 2	Start of Digital Section Data	
….	Digital Section Data	
Digital_Base_Pointer + Digital_Size + 1	End of Digital Section Data	

Table 13. Flash Memory Map

ADDRESS, B	DATA	COMMENT
SVR_Ana_Base_Pointer = Digital_Base_Pointer + Digital_Size + 2	SVR_ANASection Size Byte 0	Contains SVR_Ana_Size[7:0] (SVR Analog Section Size)
SVR_Ana_Base_Pointer + 1	SVR_ANA Section Size Byte 1	Contains **Svr_Ana_Size[15:8]** (Switch voltage Regulator Analog Section Size)
SVR_Ana_Base_Pointer + 2	Start of SVR_ANA Section Data	
…	SVR_ANA Section Data	
Svr_Ana_Base_Pointer + Svr_Ana_Size * 2 + 1	End of SVR_ANA Section Data	
…	Don’t care data	
EE2TAR_*_Base_pointer = ee_to_tar_*_base[23:0] + Digital_Base_Pointer	Start of EE2TAR_* Section Data	"*" = { CIO, PCIE, DMA, USB_PA/PB, P2P_PA/PB, PCIE_PHY, ANA_COMM, DP}
…..	EE2TAR_* section data	
EE2TAR_*_Base_pointer + (ee_to_tar_*_size[7:0] * 2 * 4)-1	End of EE2TAR_* Section Data	EE_2_TAR's sections Size in amount of tuples (tuple = two Dword)
…	Don’t care data	
Arc_param_base_pointer = ee_arc_ee_base[31:0] + Digital_Base_Pointer	arc_param Size Byte 0,1,2,3	Contains arc_param_Size[31:0] (arc_param Section Size)
Arc_param_base_pointer + 4	Start of arc_param Section Data	
…	Arc_param section data	
Arc_param_base_pointer + 4 + (4 x arc_param_size)-1	End of arc_param Section Data	Arc_param Size in amount of Dword's
…	Don’t care data	
DP_param_base_pointer = ee_hdp_out_region_addr0/1/2[23:0] + Digital_Base_Pointer	DP_param Size Byte 0,1	Contains dp_param_Size[15:0] (dp_param Section Size)
DP_param_base_pointer + 2	Start of dp_param Section Data	
…	dp_param section data	
DP_param_base_pointer + (2 X dp_param_size)-1	end of dp_param Section Data	dp_param Size in amount of Dword's
…	Don’t care data	
DROM_base_pointer = ee_drom_start_addr[32:0] + Digital_Base_Pointer	DP_param Size Byte 0,1,2,3	Contains DROM_Size[31:0] (DROM Section Size)
DROM_base_pointer + 4	Start of DROM Section Data	

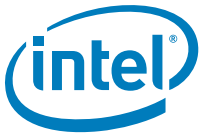


Table 13. Flash Memory Map

ADDRESS, B	DATA	COMMENT
…..	DROM section data	
DROM_base_pointer + (4 X DROM_size)-1	end of DROM Section Data	DROM Size in amount of Dword's
Cp_Ucode_Base_Pointer = ee_ucode_start_addr + Digital_Base_Pointer	CP_UCODE Section Size Byte 0	Contains **Cp_Ucode_Size[7:0]** (Control Port uCode Patch Section Size), **ee_ucode_start_addr[15:0]** – relative pointer from Digital Section
Cp_Ucode_Base_Pointer + ee_read_ctrl_ucode	CP_UCODE Section Size Byte 1	Contains **Cp_Ucode_Size[15:8]** (Control Port uCode Patch Section Size)
Cp_Ucode_Base_Pointer + 2 * ee_read_ctrl_ucode	Start of CP_UCODE Section Data	
…	CP_UCODE Section Data	
Cp_Ucode_Base_Pointer + (Cp_Ucode_Size * 4 + 1) * ee_read_ctrl_ucode	End of CP_UCODE Section Data	
Hdp_Out_Ucode_Base_Pointer = Cp_Ucode_Base_Pointer + (Cp_Ucode_Size * 4 + 2) * ee_read_ctrl_ucode	HDP_OUT_UCODE Section Size Byte 0	Contains **Hdp_Out_Ucode_Size[7:0]** (Display Port Out uCode Patch Section Size)
Hdp_Out_Ucode_Base_Pointer + ee_read_dp_out_ucode	HDP_OUT_UCODE Section Size Byte 1	Contains **Hdp_Out_Ucode_Size [15:8]** (Display Port Out uCode Patch Section Size)
Hdp_Out_Ucode_Base_Pointer + 2 * ee_read_dp_out_ucode	Start of HDP_OUT_UCODE Section Data	
…	HDP_OUT_UCODE Section Data	
Hdp_Out_Ucode_Base_Pointer + (Hdp_Out_Ucode_Size * 4 + 1) * ee_read_dp_out_ucode	End of HDP_OUT_UCODE Section Data	
Hdp_In_Ucode_Base_Pointer = Hdp_Out_Ucode_Base_Pointer + (Hdp_Out_Ucode_Size * 4 + 2) * ee_read_dp_out_ucode	HDP_IN_UCODE Section Size Byte 0	Contains **Hdp_Out_Ucode_Size[7:0]** (Display Port Out uCode Patch Section Size)
Hdp_In_Ucode_Base_Pointer + ee_read_dp_in_ucode	HDP_IN_UCODE Section Size Byte 1	Contains **Hdp_In_Ucode_Size [15:8]** (Display Port In uCode Patch Section Size)
Hdp_In_Ucode_Base_Pointer + 2 * ee_read_dp_in_ucode	Start of HDP_IN_UCODE Section Data	
…	HDP_IN_UCODE Section Data	
Hdp_In_Ucode_Base_Pointer + (Hdp_In_Ucode_Size * 4 + 1) * ee_read_dp_in_ucode	End of HDP_IN_UCODE Section Data	
Lc_Ucode_Base_Pointer = Hdp_In_Ucode_Base_Pointer + (Hdp_In_Ucode_Size * 4 + 2) * ee_read_dp_in_ucode	LC_UCODE Section Size Byte 0	Contains **Lc_Ucode_Size[7:0]** (Display Link Controller uCode Patch Section Size)
Lc_Ucode_Base_Pointer + ee_read_clc_ucode	LC_UCODE Section Size Byte 1	Contains **Lc_Ucode_Size [15:8]** (Link Controller uCode Patch Section Size)
Lc_Ucode_Base_Pointer + 2 * ee_read_clc_ucode	Start of LC_UCODE Section Data	
…	LC_UCODE Section Data	

Table 13. Flash Memory Map

ADDRESS, B	DATA	COMMENT
Lc_Ucode_Base_Pointer + (Lc_Ucode_Size * 4 + 1) * ee_read_clc_ucode	End of LC_UCODE Section Data	
Arc_Ucode_Base_Pointer = Lc_Ucode_Base_Pointer + (Lc_Ucode_Size * 4 + 2) * ee_read_clc_ucode	ARC_UCODE Section Size Byte 0	Contains **Arc_Ucode_Size[7:0]** (Display Arc Controller uCode Patch Section Size)
Arc_Ucode_Base_Pointer + ee_read_arc_ucode	ARC_UCODE Section Size Byte 1	Contains **Arc_Ucode_Size [15:8]** (Arc Controller uCode Patch Section Size)
Arc_Ucode_Base_Pointer + 2 * ee_read_arc_ucode	Start of ARC_UCODE Section Data	
…	ARC_UCODE Section Data	
Arc_Ucode_Base_Pointer + (Arc_Ucode_Size * 4 + 1) * ee_read_arc_ucode	End of ARC_UCODE Section Data	
cio_iram_Ucode_Base_Pointer = Arc_Ucode_Base_Pointer + (arc_Ucode_Size * 4 + 2) * ee_read_arc_ucode	CIO_IRAM_UCODE Section Size Byte 0	Contains cio_iram_Ucode_Size[7:0] (Display cio_iram Controller uCode Patch Section Size)
cio_iram_Ucode_Base_Pointer + ee_read_cio_iram_ucode	CIO_IRAM_UCODE Section Size Byte 1	Contains cio_iram_Ucode_Size [15:8] (cio_iram Controller uCode Patch Section Size)
cio_iram_Ucode_Base_Pointer + 2 * ee_read_cio_iram_ucode	Start of CIO_IRAM_UCODE Section Data	
…	CIO_IRAM_UCODE Section Data	
cio_iram_Ucode_Base_Pointer + (cio_iram_Ucode_Size * 4 + 1) * ee_read_cio_iram_ucode	End of CIO_IRAM_UCODE Section Data	
cio_dram_Ucode_Base_Pointer = cio_iram_Ucode_Base_Pointer + (cio_iram_Ucode_Size * 4 + 2) * ee_read_cio_iram_ucode	CIO_DRAM_UCODE Section Size Byte 0	Contains cio_dram_Ucode_Size[7:0] (Display cio_dram Controller uCode Patch Section Size)
cio_dram_Ucode_Base_Pointer + ee_read_cio_dram_ucode	CIO_DRAM_UCODE Section Size Byte 1	Contains cio_dram_Ucode_Size [15:8] (cio_dram Controller uCode Patch Section Size)
cio_dram_Ucode_Base_Pointer + 2 * ee_read_cio_dram_ucode	Start of CIO_DRAM_UCODE Section Data	
…	CIO_DRAM_UCODE Section Data	
cio_dram_Ucode_Base_Pointer + (cio_dram_Ucode_Size * 4 + 1) * ee_read_cio_dram_ucode	End of CIO_DRAM_UCODE Section Data	
…	Don’t care data	
Arc_Cache_Base_Pointer = arc_cache_rd_addr	Start of ARC_CACHE Data	**arc_cache_rd_addr[23:0]** – absolute pointer from Arc Cache Read i/f
…	ARC_CACHE Data	

Table 13. Flash Memory Map

ADDRESS, B	DATA	COMMENT
Arc_Cache_Base_Pointer + Arc_Cache_Size - 1	End of ARC_CACHE Data	Arc_Cache_Size = **arc_cache_rd_length[15:0]** – data from Arc Cache Read i/f
…	Don’t care data	
pps_Base_Pointer = PPSB0/PPSB1	PPS section	

3.2.1 Flash memory Read Flow

The Flash memory read procedure is as follows:

- LC domain Auto-load data caused by car_power_good_e (power good reset) de-assertion
  - — Detection of valid data recorded in the Flash Memory
    - —Read the first 24 bits from Flash Memory
      - — If 0xFFFFFF, no FARB (Flash Active Base Pointer) found ' try to read from 4K offset (Flash Address 0x1000)
      - — Else the content reflects FARB ' go start to read Digital section from this pointer
    - —Read 24 bits from 4K offset (Flash Address 0x1000)
      - — If 0xFFFFFF, no FARB (Flash Active Base Pointer) found, no valid Flash memory attached or no valid data recorded on Flash Memory ' done
      - — Else the content reflects FARB ' go start to read Digital section from this pointer
  - — Read Digital section according to section size (length (16 bits) is number of bytes)
  - — Read SVR Analog section according to section size (length (16 bits) is number of address (8 bits)/data (8 bits) tuples)
  - — - If enabled by repressive bit in digital section, read the scratch ram section from flash to internal memory, size 256 bytes.
  - — If enabled by the respective bit in the digital section, read the CLC ucode patch section, according to section size (length in DWs - 16bit field).
- Read upon request, per each power_domain above LC domain (such as: ana_comm, dp, pcie, cio and usb), LC FW request relevant section to be loaded from flash. Section includes (uCode's and ee2tars'), ee2tar's are loaded upon triggers align to domain power_up.
- Ucode load sections are:
  - — If enabled by the respective bit in the digital section and requested by LC FW, read the "*_ucode" patch section, according to section size (length in DWs - 16bit field).
  - — "*" = {CP, DP_OUT, DP_IN, LC, ARC, CIO_IRAM, CIO_DRAM},
  - — Both CIO_IRAM and CIO_DRAM must load together
- Ee2tar's load sections are:
  - — If triggered by the respective reset in the ee2tar_fsm, read the "*_ee2tar" section, according to section address and size (length in amount of tuples = two Dword).
  - — "*" = { CIO, PCIE, DMA, USB_PA/PB, P2P_PA/PB, PCIE_PHY, ANA_COMM, DP }.
- After any CIO Reset de-assertion
  - — Control Port initializes PCIe and other parameters from the ee_to_tar section, according to section length (length (8 bits) is number of data (32 bits)/ address (32 bits) tuples)

3.3 Target Bus Access via Flash Memory (ee to tar Section)

As part of the Control Port initialization sequence after CIO Reset, the set of registers pre-configured in the flash memory can be written. This can be done to fix default values or execute a custom workaround/configuration.

In steady state (after initial read), the flash block is ready to accept "by address" reads from the ee2tar_fsm (DW aligned offset, DW per read). These are used for reading address/data tuples from flash memory and writing them onto the Target Bus.

ee_to_tar_base - Base address from which the address/data tuples are read by the ee2tar_fsm.

ee_to_tar_size[7:0] - Size in amount of tuples; 0 = nothing to do.

Note: As the ee_to_tar_size is 8 bit wide, this mechanism is limited to 255 data / command tuples.

The command register parameters are decoded by the Control Port as shown in Table 14:

Table 14. Command Register Parameters

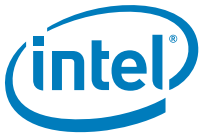
31 24	23 21	20 19	18 13	12 0
Reserved	CMD	CS	Port#	DW Index

Field	Bit(s)	Description	
DW Index	12:0	Sets DW Index Target bus value	
Port#	18:13	Sets Port# Target bus value	
CS	20:19	Sets CS Target bus value, as follows:	
		CS Value	**Configuration space**
		00	Path Config. Space
		01	Port Config. Space
		10	Device Config. Space
		11	Counters Config. Space
CMD	21	0: Read command 1: Write command	
	22	0: Regular Target bus access 1: Access to CIO Switch registers – See below	
	23	0: Regular Target bus access 1: Access to PCIe Switch registers – See below	
Reserved	31:24	Reserved – set to 0	

For PCIe Switch register configuration, the lower 21 bits of the command are regarded in a different fashion than they are at regular Target Access via Flash ():

Table 15. PCIe Switch Command Register Parameters

31 24	23 21	20 19	18 10	9 6	5 0
Rsvd	CMD	Rsvd	Choose Bridge	Ex Reg #	Reg #



Each write access can be made to several ports simultaneously. For this, use encoding of chosen ports, where:

- DMA EMEP_cnfg= Choose_bridge[8]
- xHC EMEP_cnfg = Choose_bridge[6]
- Dn4_cnfg = Choose_bridge[5]
- Dn0_cnfg = Choose_bridge[1]
- Up0_cnfg = Choose_bridge[0]

3.4 Flash Programming Interface

SW fills SPI command, address and [write/read data] using below registers in the below order (i.e. data first, control last).

HW shifts them out accordingly, where data is either shifted out [write] or in [read].

3.4.1 Registers

- SPI_DATA<15:0> // 16 * 32bit registers - total 64B
  - SPI_DATA<15>
  - SPI_DATA<14>
  - . . .
  - SPI_DATA<1>
  - SPI_DATA<0>

  Plain RW registers that either shift-in or shift-out depending on spi_shift_in1_out0
- SPI_CMD_ADDR
  - [23:0] - SPI 24bit address
  - [31:24] - command
- SPI_CONTROL
  - [7:0] spi_data_bytes_amount // amount of bytes to shift in/out
  - [11:8] spi_dummy_bytes_amount // amount of dummy bytes to shift out after 24bit address, before shifting in/out the data
  - [28] nvm_accesses_allowed // secure_en indication read-only value
  - at should be an input signal from flash controller common logic
  - [29] spi_address_present // 1: need to shift out address from SPI_CMD_ADDR after command; 0: command without address
  - [30] spi_shift_in1_out0 // in: read, out:write
  - [31] req1_ack0 // SW to set to 1, HW to clear upon completion
  - Remaining bits are plain r/w for future use

The registers are mapped to flash_ctrl_reg16…flash_ctrl_reg33 (0x40F…0x421 of Flash Controller area in Device Space) in the above order, at consecutive offsets, so that multiple-DW access from CIO will fill it in one single write packet.

Before any write or erase operation, SW/FW should ensure that HW accesses to NVM (thru ee_read_arbiter) are stalled. That is done by setting EEC.bitbang_request and polling EEC.bitbang_ready. After write/erase is completed, EEC.bitbang_request should be cleared.

3.4.2 Examples (based on Winbond W25X10BL/20BL/40BL)

3.4.2.1 Example 1: Read ID - (0x90)

a. Write (possibly using single CIO packet)

SPI_CMD_ADDR = 0x90_000000 // opcode_addr

SPI_CONTROL = 0x00000000 |

1 << 31 | // req1_ack0 = REQ

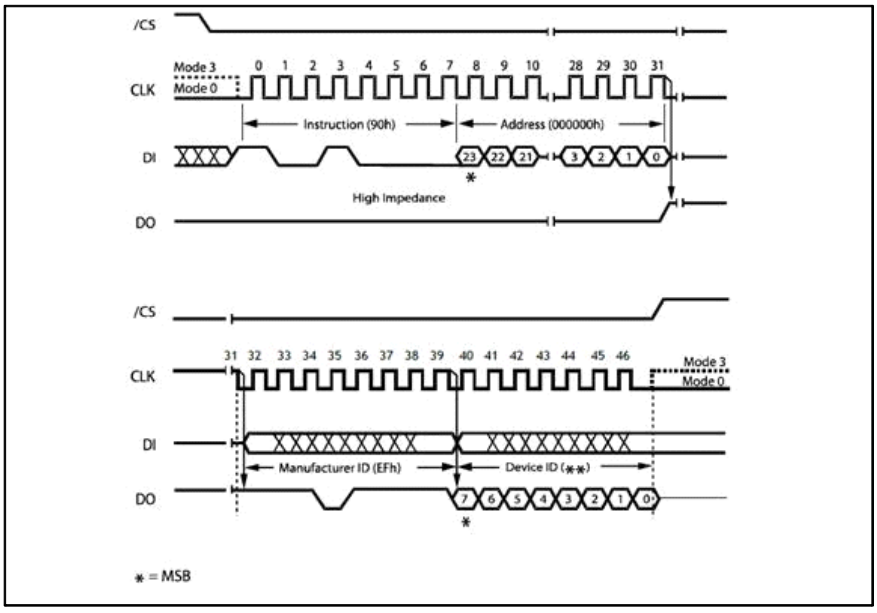
1 << 30 | // spi_shift_in1_out0 = IN/READ

1 << 29 | // spi_address_present = YES

2 << 0 | // spi_data_bytes_amount = 2

That should cause the waveforms in Figure 5.

Figure 5. Read Manufacturer/Device ID diagram



b. While (req1_ack0 from chip)=1 or timeout {

Read (possibly using single CIO packet)

SPI_DATA<0>

SPI_CMD_ADDR

SPI_CONTROL

}

c. ID's are in SPI_DATA<0>[15:0]

3.4.2.2 Example 2: Write Enable - (0x06)

a. Write (possibly using single CIO packet)

SPI_CMD_ADDR = 0x06_000000 // opcode_addr

SPI_CONTROL = 0x00000000 |

1 << 31 | // req1_ack0 = REQ

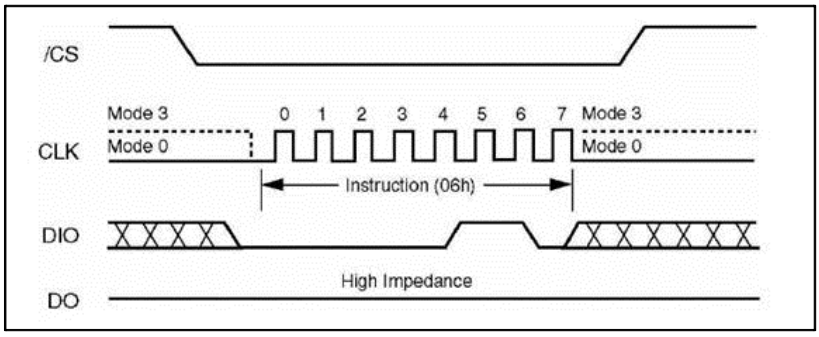
0 << 30 | // spi_shift_in1_out0 = N/A

0 << 29 | // spi_address_present = NO

0 << 0 | // spi_data_bytes_amount = 0

That should cause the waveforms in Figure 6.

Figure 6. Write Enable Instruction Sequence diagram



b. While (req1_ack0 from chip)=1 or timeout {

Read SPI_CONTROL

}

c. Flash is writeable (can be confirmed by reading status)

3.4.2.3 Example 3: Sector Erase - (0x20)

a. Write (possibly using single CIO packet)

SPI_CMD_ADDR = 0x20_000000 // opcode_addr

SPI_CONTROL = 0x00000000 |

1 << 31 | // req1_ack0 = REQ

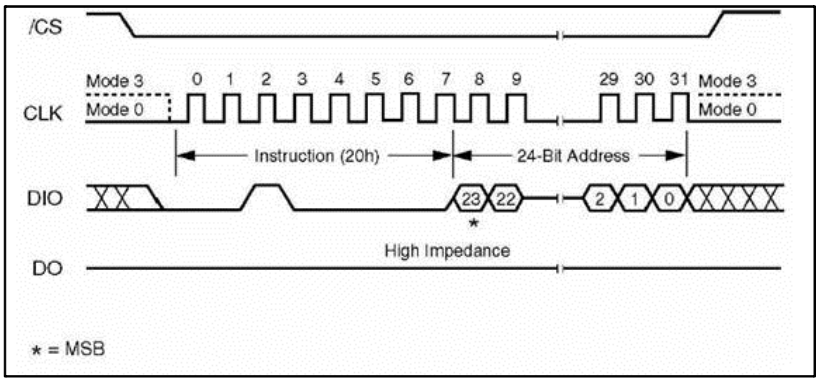
0 << 30 | // spi_shift_in1_out0 = N/A

1 << 29 | // spi_address_present = YES

0 << 0 | // spi_data_bytes_amount = 0

That should cause the waveforms in Figure 7.

Figure 7. Sector Erase Instruction Sequence diagram



b. While (req1_ack0 from chip)=1 or timeout {

Read SPI_CONTROL

}

c. Done erasing

3.4.2.4 Example 4: Page Program - (0x02)

example for 7 Bytes write

a. Write (possibly using single CIO packet)

SPI_DATA<1> = 0x00070605

SPI_DATA<0> = 0x04030201

SPI_CMD_ADDR = 0x02_A3A2A1 // opcode_addr

SPI_CONTROL = 0x00000000 |

1 << 31 | // req1_ack0 = REQ

0 << 30 | // spi_shift_in1_out0 = OUT/WRITE

1 << 29 | // spi_address_present = YES

7 << 0 | // spi_data_bytes_amount = 7

b. That should cause

<02><A3><A2><A1><01><02>...<07>

c. While (req1_ack0 from chip)=1 or timeout {

Read SPI_CONTROL

}

d. Done writing

Note: Before next operation (after write and few others), BUSY should be checked in the status register.

For example:

```
Poll_BUSY() {
SPI_CMD_ADDR = 0x05_000000
do {
   SPI_CONTROL  = 0xC0000001
   While (req1_ack0 from chip)=1 or timeout {
      Read    SPI_CONTROL
   }
   BUSY = SPI_DATA<0>[0]
} while (BUSY or timeout)
}
```

Also Write Enable should be re-issued after EACH Page Program!

3.4.2.5 Example 5: Read Data - (0x03)

Example for 7 Bytes read

a. Write (possibly using single CIO packet)

```
SPI_CMD_ADDR  = 0x03_A3A2A1  // opcode_addr
SPI_CONTROL   = 0x00000000 |
            1 << 31    | // req1_ack0 = REQ
            1 << 30    | // spi_shift_in1_out0 = IN/READ
            1 << 29    | // spi_address_present = YES
            7 << 0     | // spi_data_bytes_amount = 7
```

b. That should cause

<03><A3><A2><A1><01><02>...<07>

c. While (req1_ack0 from chip)=1 or timeout {

Read (possibly using single CIO packet)

SPI_DATA<1>

SPI_DATA<0>

SPI_CMD_ADDR

SPI_CONTROL

}

d. Read data is placed like in the write command above

3.5 Flash Programming High Level Procedure

To program the next active region, SW/FW should follow the following general procedure:

1 Compute the next (non-active) FARB pointer, next_FARB.

For example, assuming active region immediately follows the headers, that can be done in the following manner:

read Manufacturer/Device ID from the flash chip to determine its size (flash_size)

if (active FARB == 16K) // low region is active

next_FARB = (16KB+(flash_size-16KB)/2) // pointing to the middle of the flash space after headers

else // high region is active

next_FARB = 16KB // Pointing after headers

2 Make sure that next desired active region content size is <= (flash_size-16KB)/2 ; abort otherwise

3 Program the next desired active region content starting at next_FARB offset

4 Program the other (non-active) header's FARB to point to next_FARB

5 Erase the active header sector

6 New image will be used starting from the next LC domain power-cycle

3.6 Flash Active Region Byte Description

Note: updates are expected in this section.

See Table 16.

Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x0000	to 0x0001	Bytes to Read [7:0]	Length of digital configuration (number of Bytes, not including self)	N/A

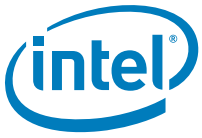


Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x0001	to 0x0001	Bytes to Read [15:8]	Length of digital configuration (number of Bytes, not including self)	N/A
0x0002	0	Read DP IN Ucode	0: Don't read ucode patch for DP in 1: Read ucode patch for DP in	N/A
0x0002	1	Read DP Out Ucode	0: Don't read ucode patch for DP out 1: Read ucode patch for DP out	N/A
0x0002	2	Read Ctrl Ucode	0: Don't read ucode patch for ctrl_port 1: Read ucode patch for ctrl_port	N/A
0x0002	3	Read ARC ucode	0: Don't read ucode patch for ARC 1: Read ucode patch for ARC	N/A
0x0002	4	Read CLC ucode	0: Don't read ucode patch for CLC 1: Read ucode patch for CLC	N/A
0x0002	5	Read CIO Ana iram ucode	0: Don't read ucode patch for CIO Ana 1: Read ucode patch for CIO Ana	N/A
0x0002	6	Read CIO Ana dram ucode	0: Don't read ucode patch for CIO Ana 1: Read ucode patch for CIO Ana	N/A
0x0003	to 0x0004	Ucode Start Address [7:0]	Base address (in Bytes) from which the ucode to the ctrl_port is being read (in bytes, points to the size field)	N/A
0x0004	0x0004	Ucode Start Address [15:8]	Base address (in Bytes) from which the ucode to the ctrl_port is being read (in bytes, points to the size field)	N/A
0x0005	to 0x0007	Used for SW	DeviceID, SI Stepping, product revision	N/A
0x0008	to 0x000A	Flash Revision [7:0]	FLASH Revision. See datasheet for field decoding. Not used by the HW	N/A
0x0009	to 0x000A	Flash Revision [15:8]	FLASH Revision. See datasheet for field decoding. Not used by the HW	N/A
0x000A	0x000A	Flash Revision [23:16]	FLASH Revision. See datasheet for field decoding. Not used by the HW	N/A
0x000B	[7:0]	ee_cp_control	Generic configuration bits for CP.	EEC[16:9]
0x000C	0x000F	Reserve	Reserve	N/A
0x0010	0	Disables MSI-x capability	0: MSI-X supported 1: MSI-X is disabled	N/A
0x0010	1	Router/Switch Config	0: chip is in switch/endpoint configuration 1: chip is in Host Router configuration	DFT1[7]
0x0010	2	Reserve	Reserve	N/A
0x0010	3	PCIe Lanes Mode	0: 4x1 - 4 Endpoints, one lane each 1: 1 x4 - 1 Endpoint of four lanes	N/A
0x0010	4	Sel Deemph Us	0:US de-emphasis setting is-6dB 1:US de-emphasis setting is-3.5dB	N/A
0x0010	5	Reserve	Reserve	N/A
0x0010	6	CIO Ctrl Rst Req Dis	0: cio ctrl reset request is enabled 1: cio ctrl reset request is disabled	N/A
0x0010	7	Reserved	Reserved	N/A
0x0011	[7:0]	Reserve	Reserve	
0x0012	[5:0]	Reserve	Reserve	N/A
0x0012	6	CIO Null Sel Pre Resume	Minimum period of LSLE pin to be low before driving a resume pulse 0: 2us 1: 15us	N/A

Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x0012	7	Enable DMA	0: DMA is gated 1: DMA is enabled	N/A
0x0013	0	ee_pcie_clk_stable	0: pcie_clocks are gated 1: pcie_clocks are ungated.	N/A
0x0013	1	CIO Perst Pwgd Sel	0: power_good only 1: power_good && perst_n	N/A
0x0013	2	PCIe Perst Pwgd Sel	0: power_good only 1: power_good && perst_n	N/A
0x0013	3	TMU Perst Pwgd Sel	0: power_good only 1: power_good && perst_n	N/A
0x0013	4	HDP IN 1 PWDN	1: HDPI_1 is disabled 0: HDPI_1 port is enabled	N/A
0x0013	5	HDP IN 0 PWDN	1: HDPI_0 is disabled 0: HDPI_0 port is enabled	N/A
0x0013	6	HDPO PWDN	1: HDPO is disabled 0: HDPO port is enabled	N/A
0x0013	7	PCIe CIO PLL Powerdown	0: PCIE active 1: PCIE not active	N/A
0x0014	[7:0]	Reserve	Reserve	N/A
0x0015	[6:0]	Reserve	Reserve	N/A
0x0015	7	ee_tl_rx_flow_ctrl_cb	When 1 will cancel tl rx flow control fix	N/A
0x0016	[6:0]	Reserve	Reserve	N/A
0x0016	7	Flash Clock Full Frequency Enable	Enables usage of full frequency for car_eep_clock. Disabled on reset. Effective in CAR after eep_done (digital section load). 0: car_eep_clk = poc_osc_50_clk/2 1: car_eep_clk = poc_osc_50_clk	N/A
0x0017	[7:0]	Reserve	Reserve	N/A
0x0018	[7:0]	US Port	Upstream Port. Bit 6 Reserved. Bit 7 is load enable	DEVICE_CS_1[13:8]
0x0019	0	Credit Sync TX Disable	0: SYNC packets are sent by spec 1: SYNC packets are NOT sent at all	DFT1[0]
0x0019	1	Tar Timeout Disable	0: Target bus transaction will auto-ack in 1msec 1: Target bus will wait for ack forever	DFT1[1]

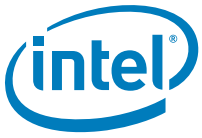


Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x0019	[6:2]	Plug Event Control	Functionality (per bit): 0. When set to 1, enables full plug events mechanism, including HDP ports. When 0, uses legacy LR implementation (CIO only) 1. if bit[0]=0 Disable plug events from CIO Port#1 (LR); if bit[0]=1 Disable plug events from any CIO null Port (1,2,3,4) 2. if bit[0]=0 Disable plug events from CIO Port#2 (LR); if bit[0]=1 Disable plug events from HDP#10 3. if bit[0]=0 Disable plug events from CIO Port#3 (LR); if bit[0]=1 Disable plug events from HDP#11 4. if bit[0]=0 Disable plug events from CIO Port#4 (LR); if bit[0]=1 Disable plug events from HDP#12	DFT1[6:2]
0x0019	7	Ctrl Ignore CRC	0: Regular mode 1: Control Port will ignore CRC result and process the packet	N/A
0x001A	[5:0]	CIO Null Phy RX Active Delay	Indicate the delay between LSOE rise and rx analog phy when exiting from CL1	N/A
0x001A	6	CIO Null Dis TL Clk Gate	Disable clock gating to cio transport layer; this will be 1 for power on only	N/A
0x001A	7	Disable Self Teardown	When set to 1, disables "self-teardown" by hardware	N/A
0x001B	0	PCIe Ad5 Rst Req Dis	0: pcie ADP5 reset request is enabled 1: pcie ADP5 reset request is disabled	N/A
0x001B	1	PCIe EP Rst Req Dis	0: pcie EP reset request is enabled 1: pcie EP reset request is disabled	N/A
0x001B	2	Security Enable	default SV image will change strapping of the security option	N/A
0x001B	3	PCIe L0 Rst Req Dis	0: pcie_l0 reset request is enabled 1: pcie_l0 reset request is disabled	N/A
0x001B	4	PCIe L1 Rst Req Dis	0: pcie_l1 reset request is enabled 1: pcie_l1 reset request is disabled	N/A
0x001B	5	PCIe L2 Rst Req Dis	0: pcie_l2 reset request is enabled 1: pcie_l2 reset request is disabled	N/A
0x001B	6	PCIe L3 Rst Req Dis	0: pcie_l3 reset request is enabled 1: pcie_l3 reset request is disabled	N/A
0x001B	7	No Port Error Event	0: Regular mode 1: Control Port will not generate error events with codes 1, 12, 13	N/A
0x001C	[2:0]	Reserve	Reserve	N/A
0x001C	3	CIO Dis FC Timer	0: default power spec 1: disable periodic CIO FC grant updates	N/A
0x001C	4	ee_pcie_two_low_lanes	0: Lanes 0,1 are 2x1 1: Lanes 0,1 are 1x2	N/A
0x001C	5	ee_pcie_two_high_lanes	0: Lanes 2,3 are 2x1 1: Lanes 2,3 are 1x2	N/A

Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x001C	6	Ctrl Ignore FC	When set, CP will ignore credits check when sending control packets	N/A
0x001C	7	Reserve	Reserve	N/A
0x001D	[7:0]	Reserve	Reserve	N/A
0x001E	0	CIO Null Dis Hec Err Retrain	0: CIO port will retrain link upon hec error 1: CIO port won't retrain link upon hec error	N/A
0x001E	1	CIO Null Force Connected	0: CIO port will behave normally 1: CIO port will skip connect detection	N/A
0x001E	2	CIO Null Force Link Up	0: CIO port will behave normally 1: CIO port will skip training	N/A
0x001E	[7:3]	CIO Null Min Os Size	Number of min OS to send in link FSM	N/A
0x001F	[2:0]	CIO Null Num RX Connect Pulse	Specify amount of connect pulses to decide on connected state	N/A
0x001F	[5:3]	Reserve	Reserve	N/A
0x001F	[7:6]	Delay to read next data for ANA section	Specify the delay before next strobe to ana regs. Supposing 60 MHz oscillator clock - d0: 0.80 us d1: 1.07 us d2: 1.34 us d3: 1.60 us	N/A
0x0020	to 0x0021	TMU TX Time To Wire Port 1 [7:0]	Specify the time duration between the instant the timestamp is taken and when the first bit of the TSNOS is received/transmitted on the wire	port 1, TMU_PORT_CS_1[27:16]
0x0021	to 0x0021	TMU TX Time To Wire Port 1 [11:8]	Specify the time duration between the instant the timestamp is taken and when the first bit of the TSNOS is received/transmitted on the wire	port 1, TMU_PORT_CS_1[27:16]
0x0021	[7:4]	Reserve	Reserve	N/A
0x0022	to 0x0023	TMU TX Time To Wire Port 2 [7:0]	Specify the time duration between the instant the timestamp is taken and when the first bit of the TSNOS is received/transmitted on the wire	port 2, TMU_PORT_CS_1[27:16]
0x0023	to 0x0023	TMU TX Time To Wire Port 2 [11:8]	Specify the time duration between the instant the timestamp is taken and when the first bit of the TSNOS is received/transmitted on the wire	port 2, TMU_PORT_CS_1[27:16]
0x0023	7:4	Reserved	Reserved	N/A
0x0024	to 0x0025	TMU TX Time To Wire Port 3 [7:0]	Specify the time duration between the instant the timestamp is taken and when the first bit of the TSNOS is received/transmitted on the wire	port 3, TMU_PORT_CS_1[27:16]
0x0025	to 0x0025	TMU TX Time To Wire Port 3 [11:8]	Specify the time duration between the instant the timestamp is taken and when the first bit of the TSNOS is received/transmitted on the wire	port 3, TMU_PORT_CS_1[27:16]
0x0025	7:4	4	Reserved	N/A
0x0026	to 0x0027	TMU TX Time To Wire Port 4 [7:0]	Specify the time duration between the instant the timestamp is taken and when the first bit of the TSNOS is received/transmitted on the wire	port 4, TMU_PORT_CS_1[27:16]

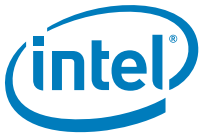


Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x0027	to 0x0027	TMU TX Time To Wire Port 4 [11:8]	Specify the time duration between the instant the timestamp is taken and when the first bit of the TSNOS is received/transmitted on the wire	port 4, TMU_PORT_ CS_1[27:16]
0x0027	7:4	4	Reserved	N/A
0x0028	to 0x0029	TMU RX Time To Wire Port 1 [7:0]	Specify the time duration between the instant the timestamp is taken and when the first bit of the TSNOS is received/transmitted on the wire	port 1, TMU_PORT_ CS_2[27:16]
0x0029	to 0x0029	TMU RX Time To Wire Port 1 [11:8]	Specify the time duration between the instant the timestamp is taken and when the first bit of the TSNOS is received/transmitted on the wire	port 1, TMU_PORT_ CS_2[27:16]
0x0029	7:4	4	Reserved	N/A
0x002A	to 0x002B	TMU RX Time To Wire Port 2 [7:0]	Specify the time duration between the instant the timestamp is taken and when the first bit of the TSNOS is received/transmitted on the wire	port 2, TMU_PORT_ CS_2[27:16]
0x002B	to 0x002B	TMU RX Time To Wire Port 2 [11:8]	Specify the time duration between the instant the timestamp is taken and when the first bit of the TSNOS is received/transmitted on the wire	port 2, TMU_PORT_ CS_2[27:16]
0x002B	7:4	4	Reserved	N/A
0x002C	to 0x002D	TMU RX Time To Wire Port 3 [7:0]	Specify the time duration between the instant the timestamp is taken and when the first bit of the TSNOS is received/transmitted on the wire	port 3, TMU_PORT_ CS_2[27:16]
0x002D	to 0x002D	TMU RX Time To Wire Port 3 [11:8]	Specify the time duration between the instant the timestamp is taken and when the first bit of the TSNOS is received/transmitted on the wire	port 3, TMU_PORT_ CS_2[27:16]
0x002D	7:4	4	Reserved	N/A
0x002E	to 0x002F	TMU RX Time To Wire Port 4 [7:0]	Specify the time duration between the instant the timestamp is taken and when the first bit of the TSNOS is received/transmitted on the wire	port 4, TMU_PORT_ CS_2[27:16]
0x002F	to 0x002F	TMU RX Time To Wire Port 4 [11:8]	Specify the time duration between the instant the timestamp is taken and when the first bit of the TSNOS is received / transmitted on the wire	port 4, TMU_PORT_ CS_2[27:16]
0x002F	4	ee_dp_in_enf_cap	DP_IN Enhanced-Framing capability: 0: no supported 1: supported	Reg in DP IN 8051 subsystem space. Address 0xd252
0x002F	5	ee_dp_out_enf_cap	DP_OUT Enhanced-Framing capability: 0: no supported 1: supported	Reg in DP OUT 8051 subsystem space. Address 0xd252
0x002F	6	ee_dp_in_tps3_cap	DP_IN TPS3 capability: 0: no supported 1: supported	Reg in DP IN 8051 subsystem space. Address 0xd252

Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x002F	7	ee_dp_out_tps3_cap	DP_OUT TPS3 capability: 0: no supported 1: supported	Reg in DP OUT 8051 subsystem space. Address 0xd252
0x0030	[7:0]	HDMI In Frequency restoration control	Controls parameters in TMU_HDMI_IN	N/A
0x0031	[7:0]	HDMI Out Frequency restoration control 0	Controls parameters in TMU_HDMI_OUT	N/A
0x0032	[7:0]	HDMI Out Frequency restoration control 1	Controls parameters in TMU_HDMI_OUT	N/A
0x0033	[7:0]	DP pre-emphasis initial values	[1:0] – initial pre-emphasis to request from GPU at speed of 1.62GHz [3:2] – initial pre-emphasis to request from GPU at speed of 2.7GHz [5:4] – initial pre-emphasis to request from GPU at speed of 5.4GHz [7:6] – reserved	Reg in DP IN 8051 subsystem space. Address 0xc828,c829,c82a,c82b[1:0]
0x0034	[7:0]	DP swing initial values	[1:0] – initial swing to request from GPU at speed of 1.62GHz [3:2] – initial swing to request from GPU at speed of 2.7GHz [5:4] – initial swing to request from GPU at speed of 5.4GHz [7:6] – reserved	Reg in DP IN 8051 subsystem space. Address 0xc828,c829,c82a,c82b[3:2]
0x0035	[7:0]	ee_clc_spare_pa	refer to register description	DEV.SEC6.CHICKEN_BITS[7:0] of PA
0x0036	[7:0]	ee_clc_spare_pb	refer to register description	DEV.SEC6.CHICKEN_BITS[7:0] of PB
0x0037	[6:0]	I2C_Slave ID	7-bit address for slave ID	N/A
0x0037	7	CIO SW Extended bus mode	When 1 cause TLs and cio switch working in extended buss mode	
0x0038	to 0x39	part of port micro uuid register	value is read in port micro register 6	DEV.SEC6.UUID3 [7:0]
0x0039	to 0x39	part of port micro uuid register	value is read in port micro register 6	DEV.SEC6.UUID3 [15:8]
0x003A	[6:0]	port micro HVReq[6:0] register	value is read in port micro register 15	DEV.SEC6.HVREQ [6:0]
0x003A	7	Reserve	Reserve	N/A
0x003B	[7:0]	ee_clc_spare_pa/pb	refer to register description	DEV.SEC6.CHICKEN_BITS[23:16] of PA/PB
0x003C	[7:0]	ee_arc_config	Configuration bits for ARC subsystem	ARC Memory mapped register (EE_ARC_CONFIG[7:0])
0x003D	[7:0]	ee_arc_config	Configuration bits for ARC subsystem	ARC Memory mapped register (EE_ARC_CONFIG[15:8])

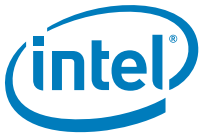


Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x003E	[7:0]	ee_arc_config	Configuration bits for ARC subsystem	ARC Memory mapped register (EE_ARC_CONFIG[23:16])
0x003F	[7:0]	ee_arc_config	Configuration bits for ARC subsystem	ARC Memory mapped register (EE_ARC_CONFIG[31:24])
0x0040	0	TMU Disable 1G Sync	0: Sampling on 1g frequency is enabled 1: Sampling on 125M is enabled	N/A
0x0040	1	TMU Serial Mode is Slave	0: TMU serial interface acts as master 1: TMU serial interface acts as slave	N/A
0x0040	2	TMU Disable All Traffic	0: TMU will work normally 1: TMU will not send any traffic	N/A
0x0040	3	TMU Disable DP Ssc	0: Enable support of SCC in DP 1: Disable support of SCC in DP	N/A
0x0040	4	TMU Disable Port 1	0: TMU port # will work normally 1: TMU port # will not send sync packets	N/A
0x0040	5	TMU Disable Port 2	0: TMU port # will work normally 1: TMU port # will not send sync packets	N/A
0x0040	6	TMU Disable Port 3	0: TMU port # will work normally 1: TMU port # will not send sync packets	N/A
0x0040	7	TMU Disable Port 4	0: TMU port # will work normally 1: TMU port # will not send sync packets	N/A
0x0041	[2:0]	Reserve	Reserve	N/A
0x0041	[5:3]	Reserve	Reserve	N/A
0x0041	6	Disable Freq offset adjustment in GTC	0: Do the frequency offset adjustment in GTC 1: Don't do the frequency offset adjustment in GTC	N/A
0x0041	7	Disable any modification of GTC. Will be passed as is	0: Do the GTC compensation calc 1: Don't change the GTC. Pass it as is	N/A
0x0042	[2:0]	Reserve	Reserve	N/A
0x0042	[5:3]	Reserve	Reserve	N/A
0x0042	[7:6]	Reserved	Reserved	N/A
0x0043	[2:0]	HDP RWM	RAM tuning parameter (Read Write Margin)	N/A
0x0043	[5:3]	HDP TL RWM	RAM tuning parameter (Read Write Margin)	N/A
0x0043	[7:6]	ee_usb_pcie_rst_ctrl	USB source reset control 0: PCIE Reset + HotReset + LinkDown + D3 to D0 1: PCIE Reset + HotReset + LinkDown 2:PCIE Reset + D3 to D0 3:PCIE Reset	N/A
0x0044	[2:0]	Reserve	Reserve	N/A
0x0044	[5:3]	Reserve	Reserve	N/A

Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x0045	[2:0]	flash_size	Defines FLASH size: 0x0 1M bit 0x1 2M bit 0x2 4M bit 0x3 8M bit 0x4 16M bit 0x5 32Mbit 0x6 64Mbit 0x7 128Mbit	N/A
0x0045	[5:3]	Reserved	Reserved	N/A
0x0045	6	ee_cio_phy_halt_on_reset_pa	cause the cio controller wake on halt state allowing control from debugger	N/A
0x0045	7	ee_cio_phy_halt_on_reset_pb	cause the cio controller wake on halt state allowing control from debugger	
0x0046	[7:0]	Reserved	Reserved	N/A
0x0047	[7:0]	Reserved	Reserved	N/A
0x0048	[7:0]	ee_clc_spare_pa/pb	refer to register description	DEV.SEC6.CHICKEN_BITS[31:24] of PA/PB
0x0049	0	Stand Alone (under Router)	1'b1 - Stand Alone	N/A
0x0049	1	USB Only (no PCIE Switch)	1'b0 - USB Only	
0x0049	[3:2]	Limit lane width of Physical Up/ Dn	2'b0 - x1 2'b1 - x2 2'b2 - x4	
0x0049	[5:4]	Rate Capability (Switch / CIO)	2'b0 - Gen1 2'b1 - Gen2 2'b2 - Gen3	
0x0049	[7:6]	Rate Capability (Endpoints)	2'b0 - Gen1 2'b1 - Gen2 2'b2 - Gen3	
0x004A	0	HDP OUT type select	0: DP, 1: HDMI	HDP vendor specific register in adapter. Port#10 Offset 0x6e, bit 0
0x004A	1	HDP IN #0 type select	0: DP, 1: HDMI	HDP vendor specific register in adapter. Port#11 Offset 0x6e, bit 0
0x004A	2	HDP OUT HDMI capability	0: HDMI not supported, 1: supported	HDP vendor specific register in adapter. Port#10 Offset 0x6e, bit 2

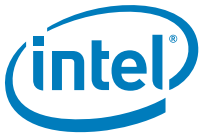


Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x004A	3	HDP OUT DP capability	0: DP not supported, 1: supported	HDP vendor specific register in adapter. Port#10 Offset 0x6e, bit 1
0x004A	4	HDP IN #0 HDMI capability	0: HDMI not supported, 1: supported	HDP vendor specific register in adapter. Port#11 Offset 0x6e, bit 2
0x004A	5	HDP IN #0 DP capability	0: DP not supported, 1: supported	HDP vendor specific register in adapter. Port#11 Offset 0x6e, bit 1
0x004A	6	ee_dont_discard_control_packet	this bit is XOR'ed with dont_discard_control_packet DMA MISC bit (which defaults to 1). This FLASH bit should be set to 1 if Swless is enabled	N/A
0x004A	7	Reserved	Reserved	N/A
0x004B	0	HDP IN #1 type select	0: DP, 1: HDMI	HDP vendor specific register in adapter. Port#12 Offset 0x6e, bit 0
0x004B	1	HDP IN #1 HDMI capability	0: HDMI not supported, 1: supported0: DP, 1: HDMI	HDP vendor specific register in adapter. Port#12 Offset 0x6e, bit 2
0x004B	2	HDP IN #1 DP capability	0: DP not supported, 1: supported0: DP, 1: HDMI	HDP vendor specific register in adapter. Port#12 Offset 0x6e, bit 1
0x004B	[7:3]	Reserved	Reserved	
0x004C	to 0x004F	GPIO Ownership configuration	2 bits per GPIO pin 00 : Control Port 01 : HardwareControlled (custom) 10 : Link Controller Port A 11 : Link Controller Port B	DEV.SEC6.GPIO_OWN_CTRL_LOW [7:0]
0x004D	to 0x004F	GPIO Ownership configuration	2 bits per GPIO pin 00 : Control Port 01 : HardwareControlled (custom) 10 : Link Controller Port A 11 : Link Controller Port B	DEV.SEC6.GPIO_OWN_CTRL_LOW [15:8]
0x004E	to 0x004F	GPIO Ownership configuration	2 bits per GPIO pin 00 : Control Port 01 : HardwareControlled (custom) 10 : Link Controller Port A 11 : Link Controller Port B	DEV.SEC6.GPIO_OWN_CTRL_HIGH[7:0]

Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x004F	to 0x004F	GPIO Ownership configuration	2 bits per GPIO pin 00 : Control Port 01 : HardwareControlled (custom) 10 : Link Controller Port A 11 : Link Controller Port B	DEV.SEC6.GPIO_OWN_CTRL_HIGH[15:8]
0x0050	[5:0]	MAX CIO Link Width	carry the max link width of cio link	N/A
0x0050	6	EE Read Arbiter Mode	Controls arbitration mode of ee_read_arbiter 0:round-robin (default), 1:strict;	N/A
0x0050	7	Target Bus Arbiter Mode	Controls arbitration mode of target_bus_arbiter 0:round-robin(default), 1:strict;	N/A
0x0051	[7:0]	ee_clc_spare_pa	refer to register description	DEV.SEC6.CHICKEN_BITS[15:8] of PA
0x0052	[7:0]	ee_clc_spare_pb	refer to register description	DEV.SEC6.CHICKEN_BITS[15:8] of PB
0x0053	0	Reserved	Reserved	N/A
0x0053	1	Reserved	Reserved	N/A
0x0053	2	Connector type optical / electrical	When 1 indicates that the connector type of port A is optical, when 0 indicate that the connector type is electrical	DEV.SEC6.GENERAL[1]
0x0053	3	Connector type optical / electrical	When 1 indicates that the connector type of port B is optical, when 0 indicate that the connector type is electrical	DEV.SEC6.GENERAL[1]
0x0053	[5:4]	board power source	1=BPD (bus powered device) 2=SPD (self powered device) 3=DPD (dual powered device)	DEV.SEC6.GENERAL[9:8]
0x0053	6	Reserved	Reserved	N/A
0x0053	7	Force TAP legacy mode	Forces TAP to work in legacy mode, mTAP and TAP network are disabled.	N/A
0x0054	0	Reserved	Reserved	N/A
0x0054	1	ee_pa_hdp_pwdn	1: HDP logic at portA is disabled 0: HDP logic at portA is enabled	N/A
0x0054	2	ee_pb_hdp_pwdn	1: HDP logic at portB is disabled 0: HDP logic at portB is enabled	N/A
0x0054	3	ee_cio_null_use_single_seed	Cause all lanes of multi-lane link to use the same scrambler initial seed	N/A
0x0054	4	ee_clc_tethered_cable_pa	indicate that the device is in tethered cable When 1 disable controller FW driving the external MUXes GPIO	DEV.SEC6.GENERAL[5]
0x0054	5	Enable port A	When 1 enable port A	DEV.SEC6.GENERAL[4]
0x0054	6	ee_clc_tethered_cable_pb	indicate that the device is in tethered cable When 1 disable controller FW driving the external MUXes GPIO	DEV.SEC6.GENERAL[5]
0x0054	7	Enable port B	When 1 enable port B	DEV.SEC6.GENERAL[4]
0x0055	[7:0]	snk1_dp_swap	Lanes swap for snk1 in dp mode No swapping means, swap = {3,2,1,0} = 0b11_10_01_00 = 0xe4	N/A

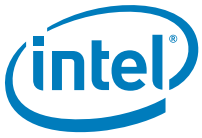


Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x0056	[7:0]	snk1_hdmi_swap	Lanes swap for snk1 in hdmi mode No swapping means, swap = {3,2,1,0} = 0b11_10_01_00 = 0xe40: DP, 1: HDMI	N/A
0x0057	[7:0]	snk2_dp_swap	Lanes swap for snk2 in dp mode No swapping means, swap = {3,2,1,0} = 0b11_10_01_00 = 0xe4	N/A
0x0058	[7:0]	snk2_hdmi_swap	Lanes swap for snk2 in hdmi mode No swapping means, swap = {3,2,1,0} = 0b11_10_01_00 = 0xe40: DP, 1: HDMI	N/A
0x0059	[7:0]	pa_dp_swap	Lanes swap for pa in dp mode No swapping means, swap = {3,2,1,0} = 0b11_10_01_00 = 0xe4	N/A
0x005A	[7:0]	pa_hdmi_swap	Lanes swap for pa in hdmi mode No swapping means, swap = {3,2,1,0} = 0b11_10_01_00 = 0xe40: DP, 1: HDMI	N/A
0x005B	[7:0]	pb_dp_swap	Lanes swap for pb in dp mode No swapping means, swap = {3,2,1,0} = 0b11_10_01_00 = 0xe4	N/A
0x005C	[7:0]	pb_hdmi_swap	Lanes swap for pb in hdmi mode No swapping means, swap = {3,2,1,0} = 0b11_10_01_00 = 0xe40: DP, 1: HDMI	N/A
0x005D	[7:0]	src_dp_swap	Lanes swap for src in dp mode No swapping means, swap = {3,2,1,0} = 0b11_10_01_00 = 0xe4	N/A
0x005E	0	snk1_ee_dp_aux_np_swap	causes the inversion of N and P pins of the DP AUX	N/A
0x005E	1	snk2_ee_dp_aux_np_swap	causes the inversion of N and P pins of the DP AUX	N/A
0x005E	2	src0_ee_dp_aux_np_swap	causes the inversion of N and P pins of the DP AUX	N/A
0x005E	3	src_pa_ee_dp_aux_np_swap	causes the inversion of N and P pins of the DP AUX	N/A
0x005E	4	src_pb_ee_dp_aux_np_swap	causes the inversion of N and P pins of the DP AUX	N/A
0x005E	5	HDP OUT type select	0: DP, 1: HDMI0: DP, 1: HDMI	N/A
0x005E	6	HDP OUT HDMI capability	0: HDMI not supported, 1: supported0: DP, 1: HDMI	N/A
0x005E	7	HDP OUT DP capability	0: DP not supported, 1: supported	N/A
0x005F	[1:0]	snk1_hdp_clk_select	1..0 – clock select for snk1 (debug)	Reg in DP IN 8051 subsystem space. Address 0xcc06[1:0]

Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x005F	[3:2]	snk2_hdp_clk_select	3..2 – clock select for snk2 (debug)	Reg in DP IN 8051 subsystem space. Address 0xcc06[1:0]
0x005F	[5:4]	cio null LS duration	When 00 - normal speed (long duration) When 01 - set LS speed level 1 - for simulating mDP mode When 10 - set LS speed level 2 - for simulating legacy mode with optic device When 11 - set LS speed level 3 - for simulating legacy mode w/o optic device	N/A
0x005F	6	Reserved	Reserved	N/A
0x005F	7	force waking cio domain on first power on	When 1 force waking cio domain on first power on	DEV.SEC6.GENERAL[12]
0x0060	[4:0]	ee_scratch_gen_poll_timer[4:0]	this timer used to configure the polling time need when using generic_fsm for status bit (BUSY) of flash. The resolaution is 100us multplay by this setting.	N/A
0x0060	5	force cio power on force power wake	Controls whether LC will power on the cio domain upon assertion of gpio3_force_pwr. 0 – will not power on 1 – will power on	DEV.SEC6.GENERAL[13]
0x0060	6	ee_cio_null_1x10_cb	cancel physical layer 2x10 changes	N/A
0x0060	7	ee_tmu_pll_calibration_disable	option to disbale tmu_pll calibration - "1" - disable, "0" enable	N/A
0x0061	to 0x0063	ee_clc_vendor_id	This 24-bit IEEE OUI for the vendor. For IECS reg0	DEV.SEC6.VENDOR_ID[7:0]
0x0062	to 0x0063	ee_clc_vendor_id	This 24-bit IEEE OUI for the vendor. For IECS reg0	DEV.SEC6.VENDOR_ID[15:8]
0x0063	to 0x0063	ee_clc_vendor_id	This 24-bit IEEE OUI for the vendor. For IECS reg0	DEV.SEC6.VENDOR_ID[23:16]
0x0064	to 0x0067	ee_clc_device_id	Vendor specific but it is recommended that it be unique between different classes of devices (ie 1m cable vs 2m cable). For IECS reg1	DEV.SEC6.DEVICE_ID[7:0]
0x0065	to 0x0067	ee_clc_device_id	Vendor specific but it is recommended that it be unique between different classes of devices (ie 1m cable vs 2m cable). For IECS reg1	DEV.SEC6.DEVICE_ID[15:8]
0x0066	to 0x0067	ee_clc_device_id	Vendor specific but it is recommended that it be unique between different classes of devices (ie 1m cable vs 2m cable). For IECS reg1	DEV.SEC6.DEVICE_ID[23:16]
0x0067	to 0x0067	ee_clc_device_id	Vendor specific but it is recommended that it be unique between different classes of devices (ie 1m cable vs 2m cable). For IECS reg1	DEV.SEC6.DEVICE_ID[31:24]

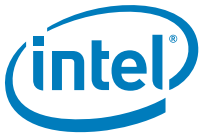


Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x0068	to 0x006B	ee_clc_protocol_version	IECS Protocol Version. Required to be 1. For IECS reg2	DEV.SEC6.PROTOCOL_VERSION[7:0]
0x0069	to 0x006B	ee_clc_protocol_version	IECS Protocol Version. Required to be 1. For IECS reg2	DEV.SEC6.PROTOCOL_VERSION[15:8]
0x006A	to 0x006B	ee_clc_protocol_version	IECS Protocol Version. Required to be 1. For IECS reg2	DEV.SEC6.PROTOCOL_VERSION[23:16]
0x006B	to 0x006B	ee_clc_protocol_version	IECS Protocol Version. Required to be 1. For IECS reg2	DEV.SEC6.PROTOCOL_VERSION[31:24]
0x006C	to 0x006F	ee_clc_mode	This field is a 4CC and used to indicate if the device is operating properly. 'APP ' – Indicates the device is fully functioning and will implement all the features advertised by the type field. Any other value indicates the device is functioning in a limited capacity and any action required is vendor specific. For IECS reg3	DEV.SEC6.MODE[7:0]
0x006D	to 0x006F	ee_clc_mode	This field is a 4CC and used to indicate if the device is operating properly. 'APP ' – Indicates the device is fully functioning and will implement all the features advertised by the type field. Any other value indicates the device is functioning in a limited capacity and any action required is vendor specific For IECS reg3	DEV.SEC6.MODE[15:8]
0x006E	to 0x006F	ee_clc_mode	This field is a 4CC and used to indicate if the device is operating properly. 'APP ' – Indicates the device is fully functioning and will implement all the features advertised by the type field. Any other value indicates the device is functioning in a limited capacity and any action required is vendor specific. For IECS reg3	DEV.SEC6.MODE[23:16]
0x006F	to 0x006F	ee_clc_mode	This field is a 4CC and used to indicate if the device is operating properly. 'APP ' – Indicates the device is fully functioning and will implement all the features advertised by the type field. Any other value indicates the device is functioning in a limited capacity and any action required is vendor specific. For IECS reg3	DEV.SEC6.MODE[31:24]
0x0070	to 0x0073	ee_clc_type	A 4CC either 'EM ', 'CM ', or 'ECM '. For IECS reg4	DEV.SEC6.TYPE[7:0]
0x0071	to 0x0073	ee_clc_type	A 4CC either 'EM ', 'CM ', or 'ECM '. For IECS reg4	DEV.SEC6.TYPE[15:8]
0x0072	to 0x0073	ee_clc_type	A 4CC either 'EM ', 'CM ', or 'ECM '. For IECS reg4	DEV.SEC6.TYPE[23:16]

Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x0073	to 0x0073	ee_clc_type	A 4CC either `EM `, `CM `, or `ECM `. For IECS reg4	DEV.SEC6.TYPE[31:24]
0x00074	[7:0]	src0_ee_hdmi_swap	Lanes swap for src in dp mode No swapping means, swap = {3,2,1,0} = 0b11_10_01_00 = 0xe40: DP, 1: HDMI	N/A
0x00075	to 0x00078	ee_arc_ee_base	ARC : Loaded into EEBASE - ARC EE Region base	ARC Memory mapped register (EEBASE[7:0])
0x00076	to 0x00078	ee_arc_ee_base	ARC : Loaded into EEBASE - ARC EE Region base	ARC Memory mapped register (EEBASE[15:8])
0x00077	to 0x00078	ee_arc_ee_base	ARC : Loaded into EEBASE - ARC EE Region base	ARC Memory mapped register (EEBASE[23:16])
0x00078	to 0x00078	ee_arc_ee_base	ARC : Loaded into EEBASE - ARC EE Region base	ARC Memory mapped register (EEBASE[31:24])
0x00079	to 0x0007C	ee_arc_ee_straps	Loaded into EESTRAPS – Config bits from FLASH	ARC Memory mapped register (EESTAPS[7:0])
0x0007A	to 0x0007C	ee_arc_ee_straps	Loaded into EESTRAPS – Config bits from FLASH	ARC Memory mapped register (EESTAPS[15:8])
0x0007B	to 0x0007C	ee_arc_ee_straps	Loaded into EESTRAPS – Config bits from FLASH	ARC Memory mapped register (EESTAPS[23:16])
0x0007C	to 0x0007C	ee_arc_ee_straps	Loaded into EESTRAPS – Config bits from FLASH	ARC Memory mapped register (EESTAPS[31:24])
0x0007D	to 0x00080	ee_arc_dpin_ssc	loaded into DPIN0CFG – DPIN0 parameters	N/A
0x0007E	to 0x00080	ee_arc_dpin_ssc	loaded into DPIN0CFG – DPIN0 parameters	N/A
0x0007F	to 0x00080	ee_arc_dpin_ssc	loaded into DPIN0CFG – DPIN0 parameters	N/A
0x00080	to 0x00080	ee_arc_dpin_ssc	loaded into DPIN0CFG – DPIN0 parameters	N/A
0x00081	[3:0]	ee_arc_plugevent_gpio	Loaded into PLUGEVENTCFG – plug event configuration (default GPIO_5__CIO_PLUG_EVENT_N)	ARC Memory mapped register (PLUGEVENTCFG[3:0])
0x00081	4	ee_arc_plugevent_on_cio	Loaded into PLUGEVENTCFG – plug event configuration	ARC Memory mapped register (PLUGEVENTCFG[30])
0x00081	5	ee_arc_plugevent_on_pcie	Loaded into PLUGEVENTCFG – plug event configuration	ARC Memory mapped register (PLUGEVENTCFG[31])
0x00081	6	ee_clc_cp_pcie_hide_emep	Controls whether DMA (embedded endpoint) will be enabled or disabled. 0 – dma is enabled 1 – dma is disabled	DEV.SEC6.EE_COMMON[8]

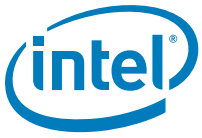


Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x00081	7	ee_arc_enable	1: ARC is enabled; 0: ARC is kept in reset	ARC Memory mapped register (ARC_DEBUG[0])
0x00082	to 0x00083	ee_arc_plugevent_delay	Loaded into PLUGEVENTCFG – plug event configuration	ARC Memory mapped register (PLUGEVENTCFG[11:4])
0x00083	[3:0]	ee_arc_plugevent_delay	Loaded into PLUGEVENTCFG – plug event configuration	ARC Memory mapped register (PLUGEVENTCFG[15:12])
0x00083	4	Reserved	Reserved	N/A
0x00083	5	Reserved	Reserved	N/A
0x00083	6	Reserved	Reserved	N/A
0x00083	7	Reserved	Reserved	N/A
0x00084	[3:0]	Disable CIO lanes	When a lane is in CIO mode, value of 1 disable the internal controller communicate the appropriate lane LS messages	DEV.SEC6.GENERAL[11:10]
0x00084	4	Bypass internal controller port A	When crux mode is selected by GPIO	DEV.SEC6.GENERAL[7]
0x00084	5	Bypass internal controller port B	When crux mode is selected by GPIO	DEV.SEC6.GENERAL[7] GENERAL
0x00084	6	disable SNK1 aux_n	When 1 disables internal controller controlling the SNK1 aux_n input	DEV.SEC6.AUX_N_CTRL[0]
0x00084	7	disable SNK2 aux_n	When 1 disables internal controller controlling the SNK2 aux_n input	DEV.SEC6.AUX_N_CTRL[2]
0x00085	0	disable UART messages on LS pins	When 1 the LS pins will carry the original LSEO/OE signals (for port A - CIO[1], for port B - CIO[3])	DEV.SEC6.GENERAL[6]
0x00085	[7:1]	Reserved	Reserved bits for CIO Switch	N/A
0x00086	[7:0]	Reserved	Reserved	N/A
0x00087	[7:0]	Reserved	Reserved	N/A
0x00088	[7:0]	GTC config bits	Chicken bits for GTC	N/A
0x00089	0	Reserved	Reserved	N/A
0x00089	2	ee_i2c_master_disable	this bit is used to enable or disable i2c_master module, if "0" i2c master will be enable, if"1" it will disable i2c master functionality	N/A
0x00089	3	XHC EMEP clock dynamic in Host	0 - XHC EMEP clocks are active in Host 1 - XHC EMEP clocks depends on XHC connect in Host	N/A
0x00089	4	ee_scracth_security_en	if "1" - scratch erase/prog is done by HW, if "0" - erase/prog is done by FW.	N/A
0x00089	5	ee_scratch_section_load_enable	descide if to enable scracth secion load on power_on "1" - enable, "0"disable	N/A
0x00089	6	Reserved	Reserved	N/A

Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x00089	7	ee_i2c_slave_disable	this bit is used to enable or disable i2c_slave module, if "0" i2c slave will be enable, if"1" it will disable i2c slave functionality	N/A
0x008a	to 0x008d	port micro version register	value is read in port micro register 7	DEV.SEC6.VERSION[7:0]
0x008b	to 0x008d	port micro version register	value is read in port micro register 7	DEV.SEC6.VERSION[15:8]
0x008c	to 0x008d	port micro version register	value is read in port micro register 7	DEV.SEC6.VERSION[23:16]
0x008d	to 0x008d	port micro version register	value is read in port micro register 7	DEV.SEC6.VERSION[31:24]
0x008e	[7:0]	General purpose configuration	HPD_Unplug on start. For DFT mode in which an HPD is generated when HPD_PLUG is detected. In DP mode: when set to value X[7:0], other than zero, will force the HPD signal to low for 64*40*X nsec. When 0xc850 is set (both in DP and HDMI mode) will force HPD low for a period of 16*40*X nsec.	Reg in DP IN 8051 subsystem space. Address 0xc848
0x008f	[7:0]	hdp_in_chicken0	When set, FW will disregard hdmi unstable indication from Analog.0: DP, 1: HDMI	Reg in DP IN 8051 subsystem space. Address 0xc849
0x0090	[7:0]	hdp_in_chicken1	Bit 0: when set, prevents requesting a new ADJUST_REQUEST from the GPU if already achieved alignment.	Reg in DP IN 8051 subsystem space. Address 0xc84a
0x0091	[7:0]	General purpose configuration	ee_hdp_in_gp_cfg3[0] (bit zero of FLASH reg 0x91) should now be: forces DP_IN FW to an eternal loop before waiting for HPD. Can be released by writing register 0xCC92 to value > 3 ([3:1] cause eternal loop in other places)	Reg in DP IN 8051 subsystem space. Address 0xc84b
0x0092	[7:0]	General purpose configuration	For future usage	Reg in DP OUT 8051 subsystem space. Address 0xc848
0x0093	[7:0]	General purpose configuration	For future usage	Reg in DP OUT 8051 subsystem space. Address 0xc849
0x0094	[7:0]	General purpose configuration	For future usage	Reg in DP OUT 8051 subsystem space. Address 0xc84a

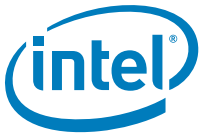


Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x0095	[7:0]	General purpose configuration	For future usage	Reg in DP OUT 8051 subsystem space. Address 0xc84b
0x0096	[7:0]	Low 8b of HDP_IN region	HDP_IN region accessed by HDP_IN (as a master)	Reg in DP IN 8051 subsystem space. Address 0xc84c
0x0097	[7:0]	Medium 8b of HDP_IN region	HDP_IN region accessed by HDP_IN (as a master)	Reg in DP IN 8051 subsystem space. Address 0xc84d
0x0098	[7:0]	High 8b of HDP_IN region	HDP_IN region accessed by HDP_IN (as a master)	Reg in DP IN 8051 subsystem space. Address 0xc84e
0x0099	[7:0]	Low 8b of HDP_OUT region	HDP_OUT region accessed by HDP_OUT (as a master)	Reg in DP OUT 8051 subsystem space. Address 0xc84c
0x009a	[7:0]	Medium 8b of HDP_OUT region	HDP_OUT region accessed by HDP_OUT (as a master)	Reg in DP OUT 8051 subsystem space. Address 0xc84d
0x009b	[7:0]	High 8b of HDP_OUT region	HDP_OUT region accessed by HDP_OUT (as a master)	Reg in DP OUT 8051 subsystem space. Address 0xc84e
0x009c	to 0x009d	Descriptor head bytes for IECS reg 11	Descriptor Head is the first node in a linked list of registers containing descriptors Byte 0: Register number of next descriptor or 0 to terminate the list Byte 1: Descriptor ID or Descriptor ID Continuation code	DEV.SEC6.DESCR_HEAD[7:0]
0x009d	to 0x009d	Descriptor head bytes for IECS reg 11	Descriptor Head is the first node in a linked list of registers containing descriptors Byte 0: Register number of next descriptor or 0 to terminate the list Byte 1: Descriptor ID or Descriptor ID Continuation code	DEV.SEC6.DESCR_HEAD[15:8]
0x009e	[7:0]	ee_cio_mng_sel_timeout	Select different value for different periods to wait before considering timeout	N/A
0x009f	to 0x00A0	ee_clc_direct_acc_base[7:0]	Select the DW offset (from start of the RAM) of memory mapped register area for SW	N/A
0x00A0	[4:0]	ee_clc_direct_acc_base[12:8]	Select the DW offset (from start of the RAM) of memory mapped register area for SW	N/A
0x00A0	[7:5]	ee_cio_null_cb	general chicken bits	N/A
0x00A1	0	Dn0 Gen1 force	Force Gen1 in Dn0 Port	N/A
0x00A1	1	Dn1 Gen1 force	Force Gen1 in Dn1 Port	N/A
0x00A1	2	Dn2 Gen1 force	Force Gen1 in Dn2 Port	N/A
0x00A1	3	Dn2 Gen1 force	Force Gen1 in Dn3 Port	N/A
0x00A1	4	EMEP no soft reset	Disables D3 --> D0 Reset	N/A

Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x00A1	5	PCIE to CIO Target disable	Disables PCIE to CIO Target access	N/A
0x00A1	6	CIO to PCIE RO Target disable	Disables CIO to PCIE Target access to Read Only registers	N/A
0x00A1	7	CIO to PCIE Target disable	Disables CIO to PCIE Target access	N/A
0x00A2	[7:0]	DDCGPIO ownership	2 bits per GPIO pin 00 : Control Port 01 : HardwareControlled (custom) 10 : Link Controller Port A 11 : Link Controller Port B	DEV.SEC6.GPIO_OWN_CTRL_HIGH [7:0]
0x00A3	[3:0]	DP_IN Capability ID	DP_IN Capability ID	N/A
0x00A3	[7:4]	DP_OUT Capability ID	DP_OUT Capability ID	N/A
0x00A4	[3:0]	DP_IN Maximal DPCD Rev	DP_IN Maximal DPCD Rev 0: 1.1 1: 1.2	N/A
0x00A4	[7:4]	DP_OUT Maximal DPCD Rev	DP_OUT Maximal DPCD Rev 0: 1.1 1: 1.2	N/A
0x00A5	[3:0]	DP_IN Maximal link rate	DP_IN Maximal link rate 0: 1.62 1: 2.7	N/A
0x00A5	[7:4]	DP_OUT Maximal link rate	DP_OUT Maximal link rate 0: 1.62 1: 2.7	N/A
0x00A6	[2:0]	DP_IN Maximal lane count	DP_IN Maximal lane count 0: 1 1: 2 2: 4	N/A
0x00A6	[5:3]	DP_OUT Maximal lane count	DP_OUT Maximal lane count 0: 1 1: 2 2: 4	N/A
0x00A6	6	DP_IN MST capability	DP_IN MST capability 0: not supported 1: supported	N/A
0x00A6	7	DP_OUT MST capability	DP_OUT MST capability 0: not supported 1: supported	N/A
0x00A7	0	DP_IN Legacy Adapters Only	DP_IN Legacy Adapters Only 0: Enable new/dp1.2 adapters 1: Enable legacy DP adapters only	N/A
0x00A7	1	DP_OUT Legacy Adapters Only	DP_OUT Legacy Adapters Only 0: Enable new/dp1.2 adapters 1: Enable legacy DP adapters only	N/A
0x00A7	2	DP_IN AUX adapter for MIN_DP_CAP_ID(0)	DP_IN AUX adapter for MIN_DP_CAP_ID(0) 0: legacy 1: dp1.2	N/A
0x00A7	3	DP_OUT AUX adapter for MIN_DP_CAP_ID(0)	DP_OUT AUX adapter for MIN_DP_CAP_ID(0) 0: legacy 1: dp1.2	N/A

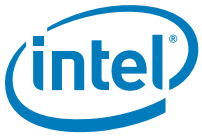


Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x00A7	4	DP_IN SST adapter for MIN_DP_CAP_ID(0)	DP_IN SST adapter for MIN_DP_CAP_ID(0) 0: legacy 1: dp1.2	N/A
0x00A7	5	DP_OUT SST adapter for MIN_DP_CAP_ID(0)	DP_OUT SST adapter for MIN_DP_CAP_ID(0) 0: legacy 1: dp1.2	N/A
0x00A7	6	Reserved	Reserved	N/A
0x00A7	7	DP_OUT AUX adapter for MIN_DP_CAP_ID(1)	DP_OUT AUX adapter for MIN_DP_CAP_ID(1) 0: legacy 1: dp1.2	N/A
0x00A8	0	DP_IN SST adapter for MIN_DP_CAP_ID(1)	DP_IN SST adapter for MIN_DP_CAP_ID(1) 0: legacy 1: dp1.2	N/A
0x00A8	1	DP_OUT SST adapter for MIN_DP_CAP_ID(1)	DP_OUT SST adapter for MIN_DP_CAP_ID(1) 0: legacy 1: dp1.2	N/A
0x00A8	2	DP_IN Prefer SST legacy	Whenever possible, use legacy DP_IN SST adapter 0: DP_IN SST adapter is selected only according to MIN_DP_CAP_ID(x)/ ee_sst_in_adp_dx 1: Legacy DP_IN SST adapter should be used whenever the link is SST 1.62G or 2.7G	N/A
0x00A8	3	DP_OUT Prefer SST legacy	Whenever possible, use legacy DP_OUT SST adapter 0: DP_IN SST adapter is selected only according to MIN_DP_CAP_ID(x)/ ee_sst_in_adp_dx 1: Legacy DP_IN SST adapter should be used whenever the link is SST 1.62G or 2.7G	N/A
0x00A8	4	DP_IN Wide Tx TL mode	Work in wide Tx mode in DP_IN from TL to the adapter 0: work in legacy mode 1: work in wide mode	N/A
0x00A8	5	DP_OUT Wide Tx TL mode	Work in wide Tx mode in DP_OUT from TL to the adapter 0: work in legacy mode 1: work in wide mode	N/A
0x00A8	6	ee_cio_car_pcie_clk_delay_cb	pcie tx clocks are active only after power good reset deassertion 0: disabled (legacy) 1: enabled	N/A
0x00A8	7	ee_cdr_mode_en	ee_cdr_mode_en - "0" disable "1" enable CDRmode	N/A
0x00A9	[7:0]	ee_master_lock_timeout	Timeout for target bus master “lock” hold without use, in [ms]; 0 disables locking mechanism; 0xFF means infinite i.e. timeout disabled	N/A
0x00AA	[7:0]	ee_pcie_dn_hide	Disable Downstream Bridges	N/A
0x00AB	0	ee_force_ana_comm_power_on	When 1 force the ON domain powerred up	N/A

Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x00AB	1	ee_force_dp_hdmi_power_on	When 1 force the ON domain powerred up0: DP, 1: HDMI	N/A
0x00AB	2	ee_force_usb_xhci_power_on	When 1 force the ON domain powerred up	N/A
0x00AB	3	ee_force_pcie_power_on	When 1 force the ON domain powerred up	N/A
0x00AB	4	ee_force_cio_power_on	When 1 force the ON domain powerred up	N/A
0x00AB	5	ee_force_lc_power_on	When 1 force the ON domain powerred up	N/A
0x00AB	6	Reserved	Reserved	N/A
0x00AB	7	ee_cio_phy_dis_rs	disable reed salomon mode in cio null phy	N/A
0x00AC	[7:0]	pa_ee_dp_swap2	swap in case the cable was connected upside down	N/A
0x00AD	[7:0]	pa_ee_hdmi_swap2	swap in case the cable was connected upside down0: DP, 1: HDMI	N/A
0x00AE	[7:0]	pb_ee_dp_swap2	swap in case the cable was connected upside down	N/A
0x00AF	0	ee_clc_debug_disable_uart_2	disable the second uart	N/A
0x00AF	1	ee_plug_event_source	0 - GPIO is set with ee_arc_config 1 - GPIO Only	N/A
0x00AF	2	Enable 64 bit BAR in DMA	1'b0 - DMA 64 bit BAR dis 1'b1 - DMA 64 bit BAR en	N/A
0x00AF	3	Enable 64 bit BAR in USB	1'b0 - USB 64 bit BAR dis 1'b1 - USB 64 bit BAR en	N/A
0x00AF	4	Disable MSIIX in USB EMEPs	0: MSI-X supported 1: MSI-X is disabled	N/A
0x00AF	5	Enable real link between USB and PCIE Switch	1'b0 - no real rate 1'b1 - real rate	N/A
0x00AF	6	ee_usb_swap_dis	CB to enable/disble swap in USB mode -"1" disable swap, "0" swap is supported	N/A
0x00AF	7	Enable DMA in Endpoint mode	1'b0 - no DMA 1'b1 - DMA exsists	N/A
0x00B0	[7:0]	ee_fr_pcie_sw_ctrl	Reserved	N/A
0x00B1	[7:0]	ee_ar_pcie_sw_ctrl	[0] - Delay Upstream / EMEP Link Up till NVM load is doen [1] - Delay Downstream idle indication [2] - XHC L1 entry control (USB Idle) [4] - Dn0 - XHC EMEP enable more NFTS [5] - Dn0 - XHC EMEP enable more NFTS [6] - Dn2 - DMA EMEP enable scrambling [7] - Dn0 - DMA EMEP enable scrambling	N/A

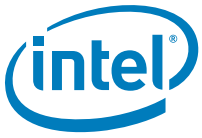


Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x00B2	[7:0]	ee_pcie_phy_ctrl1	[1:0] - gen1 NFTS value ctrl [3:2] - gen1 NFTS value ctrl [5:4] - gen1 NFTS value ctrl [6] - Rx EI exit type [7] - Delay pipe rate ctrl	N/A
0x00B3	[7:0]	ee_pcie_phy_ctrl2	[0] - Skip AHB Init [1] - Gen1 EI inferring method [2] - Gen2 EI Inferring method [3] - PCIE PHY Clk stable sel [4] - Single CMU/PLL mode enable [5] - CMU0 is always on [6] - Don’t power down CMU0 [7] - Don’t power down CMU1	N/A
0x00B4	[7:0]	ee_pcie_phy_ctrl3	[0] - Rx EI Spread ctrl [1] - Drop Rx Valid on RX EI [4:2] - Rx EI delay count ctrl [5] - Gen3 EI Inferring method [7:6] - Reserved	N/A
0x00B5	[7:0]	ee_pcie_phy_ctrl4	Reserved	N/A
0x00B6	[1:0]	Clock Rate of DMA	2'h0 - Gen1 2'h1 - Gen2 2'h2 - Gen3	N/A
0x00B6	[3:2]	Clock Rate of USB	2'h0 - Gen1 2'h1 - Gen2 2'h2 - Gen3	N/A
0x00B6	4	Enable fast PCIE Switch clock	1'b0 - disable fast 1'b1 - enable fast	N/A
0x00B6	5	ee_usb_aux_xtal_ck_en	select if to move to xtal clk when stable for usb_aux clk in car_poc_usb. "1" move to xtal else stay w/ lc_osc	N/A
0x00B6	6	pa_ee_usb2_polarity	polarity of USB2 D+/D- pins	N/A
0x00B6	7	pb_ee_usb2_polarity	polarity of USB2 D+/D- pins	N/A
0x00B7	[7:0]	USB SBRN Register	USB SBRN Register	N/A
0x00B8	[2:0]	Reserved	Reserved	N/A
0x00B8	3	DMA EMEP Prefetchable BAR	0: MSI-X supported 1: MSI-X is disabled	N/A
0x00B8	4	DMA EMEP No Soft Reset	0: Internal reset upon D3 --> D0 1: No internal reset upon D3 --> D0	N/A
0x00B8	5	DMA source reset control	0: Reset doesn't include D3 --> D0 1: Reset includes D3 --> D0	N/A
0x00B8	6	Immediate DMA init done after reset	1: Init done immediately after Reset	N/A
0x00B8	7	ee_xtal_pcie_sw_clksel_dis	0: sw_clk works w/ both xtal/pcie 1: new feature disabled, sw_clk works only w/ PCIE clks	N/A
0x00B9	[7:0]	pb_ee_hdmi_swap2	swap in case the cable was connected upside down0: DP, 1: HDMI	N/A

Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x00BA	[7:0]	Control Tx Deempasis	Tx Coefficients	N/A
0x00BB	[7:0]	Control Tx Deempasis	Tx Coefficients	N/A
0x00BC	[7:0]	Control Tx Deempasis	Tx Coefficients	N/A
0x00BD	[7:0]	ee_ee2tar_ctrl[7:0]	enables HW ee2tar, bit per client	N/A
0x00BE	[1:0]	ee_ee2tar_ctrl[9:8]	enables HW ee2tar, bit per client	N/A
0x00BE	2	Clock assign for rate change disable	0: XHC/DMA/adapter clocks are assigned from PCIE Switch Ports 1: Each clock use its own pipe rate control	N/A
0x00BE	3	Immediate PCIE init done after reset	1: Init done immediately after Reset	N/A
0x00BE	4	USB EMEP Prefetchable BAR	0: MSI-X supported 1: MSI-X is disabled	N/A
0x00BE	5	USB EMEP No Soft Reset	0: Internal reset upon D3 --> D0 1: No internal reset upon D3 --> D0	N/A
0x00BE	6	Phy Status value for not connected lanes	0: PhyStatus = 0 for not connected lanes 1: PhyStatus = 1 for not connected lanes	N/A
0x00BE	7	Immediate USB init done after reset	1: Init done immediately after Reset	N/A
0x00BF	To 0x00C1	ee_to_tar_cio_base[23:0]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00C2	[7:0]	ee_to_tar_cio_size[7:0]	Size of EE_TO_TAR section, in amount of tuples; 0 = nothing to do.	N/A
0x00C3	To 0x00C5	ee_to_tar_pcie_base[23:0]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00C6	[7:0]	ee_to_tar_pcie_size[7:0]	Size of EE_TO_TAR section, in amount of tuples; 0 = nothing to do.	N/A
0x00C7	To 0x00C9	ee_to_tar_dma_base[23:0]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00CA	[7:0]	ee_to_tar_dma_size[7:0]	Size of EE_TO_TAR section, in amount of tuples; 0 = nothing to do.	N/A
0x00CB	To 0x00CD	ee_to_tar_usb_pa_base[23:0]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00CE	[7:0]	ee_to_tar_ usb_pa_size[7:0]	Size of EE_TO_TAR section, in amount of tuples; 0 = nothing to do.	N/A
0x00CF	To 0x00D1	ee_to_tar_usb_pb_base[23:0]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00D2	[7:0]	ee_to_tar_ usb_pb_size[7:0]	Size of EE_TO_TAR section, in amount of tuples; 0 = nothing to do.	N/A
0x00D3	To 0x00D5	ee_to_tar_p2c_pa_base[23:0]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00D6	[7:0]	ee_to_tar_ p2c_pa_size[7:0]	Size of EE_TO_TAR section, in amount of tuples; 0 = nothing to do.	N/A
0x00D7	To 0x00D9	ee_to_tar_p2c_pb_base[23:0]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A

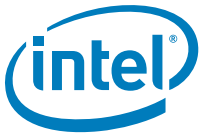


Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x00DA	[7:0]	ee_to_tar_ pcie_phy _size[7:0]	Size of EE_TO_TAR section, in amount of tuples; 0 = nothing to do.	N/A
0x00DB	To 0x00DD	ee_to_tar_p2c_pb_base[23:0]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00DE	[7:0]	ee_to_tar_ pcie_phy _size[7:0]	Size of EE_TO_TAR section, in amount of tuples; 0 = nothing to do.	N/A
0x00DF	To 0x00E1	ee_to_tar_ana_comm _base[23:0]	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00E2	[7:0]	ee_to_tar_ ana_comm _size[7:0]	Size of EE_TO_TAR section, in amount of tuples; 0 = nothing to do.	N/A
0x00E3	To 0x00E5	ee_to_tar_dp_domain _base[23:0	Base address from which the address/data tuples are read by Control Port and written to target bus	N/A
0x00E6	[7:0]	ee_to_tar_ dp_domain _size[7:0]	Size of EE_TO_TAR section, in amount of tuples; 0 = nothing to do.	N/A
0x00E7	To 0x00E8	ee_clc_spare_plus_pa [15:0]	LC FW use	N/A
0x00E9	To 0x00EA	ee_clc_spare_plus_pb [15:0]	LC FW use	N/A
0x00EB	To 0x00EC	ee_clc_spare_plus_pb /pb[15:0]	LC FW use	N/A
0x00ED	[7:0]	hw_gpio_ownership	hw ownership configuration for gpio_0[4:0] hw ownership configuration for gpio_1[7:5]	N/A
0x00EE	[7:0]	hw_gpio_ownership	hw ownership configuration for gpio_1[1:0] hw ownership configuration for gpio_2[6:2] hw_ownership configuration for gpio_3[7]	N/A
0x00EF	[7:0]	hw_gpio_ownership	hw ownership configuration for gpio_3[3:0] hw ownership configuration for gpio_4[7:4]	N/A
0x00F0	[7:0]	hw_gpio_ownership	hw ownership configuration for gpio_4[0] hw ownership configuration for gpio_5[5:1] hw_ownership configuration for gpio_6[7:6]	N/A
0x00F1	[7:0]	hw_gpio_ownership	hw ownership configuration for gpio_6[2:0] hw ownership configuration for gpio_7[7:3]	N/A
0x00F2	[7:0]	hw_gpio_ownership	hw ownership configuration for gpio_8[4:0] hw ownership configuration for poc_gpio_0[7:5]	N/A
0x00F3	[7:0]	hw_gpio_ownership	hw ownership configuration for poc_gpio_0[1:0] hw ownership configuration for poc_gpio_1[6:2] hw_ownership configuration for poc_gpio_2[7]	N/A
0x00F4	[7:0]	hw_gpio_ownership	hw ownership configuration for poc_gpio_2[3:0] hw ownership configuration for poc_gpio_3[7:4]	N/A

Table 16. Flash Byte Description

Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x00F5	[7:0]	hw_gpio_ownership	hw ownership configuration for poc_gpio_3[0] hw ownership configuration for poc_gpio_4[5:1] hw_ownership configuration for poc_gpio_5[7:6]	N/A
0x00F6	[7:0]	hw_gpio_ownership	hw ownership configuration for poc_gpio_5[2:0] hw ownership configuration for poc_gpio_6[7:3]	N/A
0x00F7	[7:0]	hw_gpio_ownership	hw ownership configuration for snk0_ddc_data[4:0] hw ownership configuration for snk0_ddc_clk[7:5]	N/A
0x00F8	[7:0]	hw_gpio_ownership	hw ownership configuration for snk0_ddc_clk[1:0] hw ownership configuration for snk1_ddc_data[6:2] hw_ownership configuration for snk1_ddc_clk[7]	N/A
0x00F9	[3:0]	hw_gpio_ownership	hw ownership configuration for snk1_ddc_clk[3:0]	N/A
0x00F9	[7:4]	Reserved	Reserved	N/A
0x00FA	[4:0]	ee_i2c_scl_master_ctrl	i2c_scl_master_ctrl	N/A
0x00FA	[7:5]	Reserved	Reserved	N/A
0x00FB	[4:0]	ee_i2c_sda_master_ctrl	i2c_sda_master_ctrl	N/A
0x00FB	[7:5]	Reserved	Reserved	N/A
0x00FC	[4:0]	ee_i2c_scl_slave_ctrl	i2c_scl_slave_ctrl	N/A
0x00FC	[7:5]	Reserved	Reserved	N/A
0x00FD	[4:0]	ee_i2c_sda_slave_ctrl	i2c_sda_slave_ctrl	N/A
0x00FD	[7:5]	Reserved	Reserved	N/A
0x00FE	[4:0]	ee_tmu_clk_in_ctrl	tmu_clk_in_ctrl	N/A
0x00FE	[7:5]	Reserved	Reserved	N/A
0x00FF	[4:0]	ee_src0_ddc_clk_ctrl	src0_ddc_clk_ctrl	N/A
0x00FF	[7:5]	Reserved	Reserved	N/A
0x0100	[4:0]	ee_src0_ddc_clk_ctrl	src0_ddc_clk_ctrl	N/A
0x0100	[7:5]	Reserved	Reserved	N/A
0x0101	[4:0]	ee_pa_overcur_ctrl	pa_overcur_ctrl	N/A
0x0101	[7:5]	Reserved	Reserved	N/A
0x0102	[7:0]	ee_pcie_clk_req_ctrl	ee_pcie_clk_req_ctrl	N/A
0x0103	[4:0]	ee_snk1_ddc_clk_ctrl	snk1_ddc_clk_ctrl	N/A
0x0103	[7:5]	Reserved	Reserved	N/A
0x0104	[4:0]	ee_snk1_ddc_data_ctrl	snk1_ddc_data_ctrl	N/A
0x0104	[7:5]	Reserved	Reserved	N/A
0x0105	[4:0]	ee_snk2_ddc_clk_ctrl	snk2_ddc_clk_ctrl	N/A
0x0105	[7:5]	Reserved	Reserved	N/A
0x0106	[4:0]	ee_snk2_ddc_data_ctr	snk2_ddc_data_ctrl	N/A
0x0106	[7:5]	Reserved	Reserved	N/A

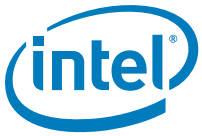


Table 16. Flash Byte Description

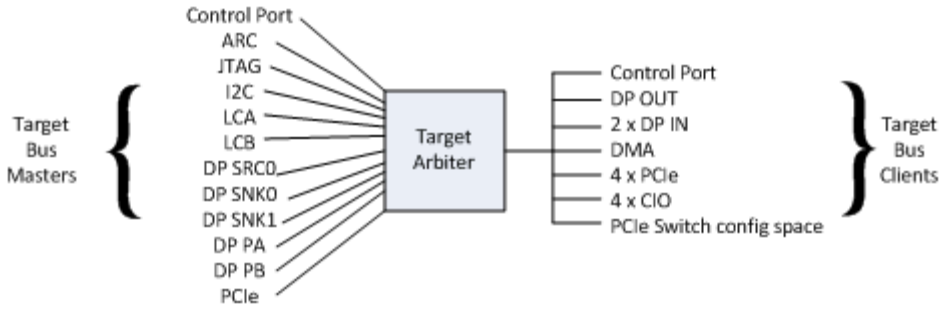
Address [Byte]	Bit[s] Offset	Field Name	Description / Purpose	Loaded to Register
0x0107	[7:0]	ee_cswf_control[7:0]	Configuration bits for CIO Switch	N/A
0x0108	[7:0]	Reserved	Reserved	N/A
0x0109	[7:0]	Reserved	Reserved	N/A
0x010A	[2:0]	ee_rm_lc_int	RM bits for ram shells in LC	N/A
0x010A	[5:3]	ee_rm_ana_int	RM bits for ram shells in ANA	N/A
0x010A	[7:6]	Reserved	Reserved	N/A
0x010B	[2:0]	ee_rm_usb_int	RM bits for ram shells in USB	N/A
0x010B	[5:3]	ee_rm_pcie_int	RM bits for ram shells in PCIE	N/A
0x010B	[7:6]	Reserved	Reserved	N/A
0x010C	[2:0]	ee_rm_dp_int	RM bits for ram shells in DP	N/A
0x010C	[5:3]	ee_rm_cio_int	RM bits for ram shells in CIO	N/A
0x010C	[7:6]	Reserved	Reserved	N/A
0x010D	[2:0]	ee_rm_rom_lc_int	RM bits for rom shells in LC	N/A
0x010D	[5:3]	ee_rm_rom_cio_int	RM bits for rom shells in CIO	N/A
0x010D	[7:6]	Reserved	Reserved	N/A
0x010E	To 0x0111	ee_drom_start_addr[31:0]	Base address (in Bytes) from which the DROM is being read (in bytes, points to the size field).	N/A
0x0115	[7:0]	Select Ports to force de-emphasis	bit 0 - Up, bit 1 - Dn0, … , bit 3 - Dn4	N/A
0x0116	[7:0]	Invert Port type (Up/Dn)	bit 0 - Up, bit 1 - Dn0, … , bit 3 - Dn4	N/A
0x0117	[4:0]	ee_pa_pwr_ctrl	gw_gpio_ownership config	N/A
0x0117	[7:5]	Reserved	Reserved	N/A
0x0118	[4:0]	ee_pb_pwr_ctrl	gw_gpio_ownership config	N/A
0x0118	[7:5]	Reserved	Reserved	N/A
0x0119	To 0x011C	ee_cdr_usb_ctrl [7:0]	cdr use	N/A
0x011D	To 0x0124	SNK1	DP-phy control bits	N/A
0x0125	To 0x012C	SNK2	DP-phy control bits	N/A
0x012D	To 0x0130	PA	DP-phy control bits	N/A
0x011	To 0x0134	PB	DP-phy control bits	N/A
0x011	To 0x0138	SRC0	DP-phy control bits	N/A
0x011	To 0x013C	Reserved	Reserved	N/A

4.0 Programming Interface

4.1 Register/Memory Access

A Target Bus and Target Arbiter are used to access the different register spaces. See Figure 8.

Figure 8. Register Access



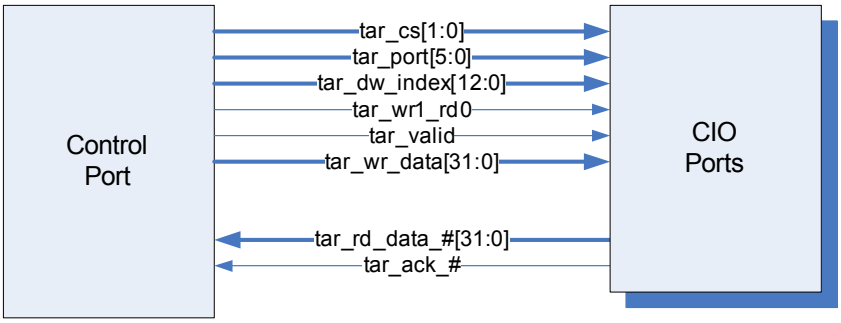
4.1.1 CIO Configuration Space Registers Access

These registers are accessed either through the Control Port µController, which receives the commands either from a CIO Packet or from FLASH Fields, or through the JTAG or I2C Slave mechanisms, which bypass the µController and access the Target Bus directly.

4.1.1.1 Target Bus Access via CIO Packet

Between the CIO Control Port and all the CIO Ports, there is an internal "target" interface used to access various configuration spaces in the ports. That interface is one-to-many / many-to-one, meaning all ports see all transactions and respond only when the destination port matches their own configuration (Figure 9).

Figure 9. Target Bus (# denotes CIO Port number)



The target bus can be driven by:

- Control Port µController
  - On reception of "CIO Config Layer Read/Write REQUEST" packets. This is the default method used by software.
  - As part of Control Port initialization sequence after CIO Reset, set of registers pre-configured in Flash Memory can be written.
- JTAG (for debug purposes).

4.1.1.2 Target Bus Access via Flash Memory

As part of the initialization sequence, a set of registers preconfigured in Flash Memory can be written. This can be done to fix default values or execute a custom workaround/configuration. See Section 3.3 for more details.

4.1.1.3 JTAG Access

There is an option to access any register mapped to the Target bus through JTAG commands. There are three registers accessed thru JTAG - command, write_data and read_data; all 32 bit wide.

Write flow

- Insert CTRL_PORT_DATA instruction (6'b111001) to IR.
- Insert 32 bits of data to write to JTAG DR. Push to TDI, start from MSB.
- Insert CTRL_PORT_CMD instruction (6'b111000) to IR.
- Insert 32 bits of command to JTAG DR. Push to TDI, start from MSB.
  - Structure: {Reserved[7'h00], Command[4'b0001], Configuration Space[1:0], Port[5:0], DWIndex[12:0]}. See Table 17.

Read flow

- Insert CTRL_PORT_CMD instruction (6'b111000) to IR.
- Insert 32 bits of command to JTAG DR. Push to TDI, start from MSB.
  - Structure: {Reserved [7'h00], Command [4'b0000], Configuration Space [1:0], Port [5:0], DWIndex[12:0]}. See Table 17.
- Insert CTRL_PORT_READ instruction (6'b111010) to IR.

- Wait 1ms.
- Push 32 bits to TDI and collect read data from TDO. MSB is read first.

The Command register parameters are decoded by Control Port according as follows:

Table 17. Command Register Parameters

31 25	24 21	20 19	18 13	12 0
Reserved	CMD	CS	Port#	DW Index

Field	Bit(s)	Description	
DW Index	12:0		Sets DW Index Target bus value
Port#	18:13		Sets Port# Target bus value
CS	20:19	Sets CS Target bus value, as follows:	
		CS Value	**Configuration space**
		00	Path Config. Space
		01	Port Config. Space
		10	Device Config. Space
		11	Counters Config. Space
CMD	21	0: Read command 1: Write command	
	22	0: Regular Target bus access 1: Access to CIO Switch registers	
	23	0: Regular Target bus access 1: Access to PCIe Switch registers	
Reserved	31:24	Reserved	

4.1.1.3.1 Assumptions / Notes:

- The write data is entered before the command. Otherwise, data in the write_data register will be written.
- There is no "cycle completion" mechanism - it is assumed that the cycle is completed properly.
- Since target bus is much faster than JTAG, no overrides of commands should occur. Yet, waiting ~1ms between accesses will ensure internal cycle completion.
- The cycle may complete with an internal timeout (if the targeted register does not respond with ack). If there is a write there is no indication. If there is a read, 0xDEADBEEF is returned.
- There is a round robin arbitration mechanism between Control Port and JTAG target accesses, thus they should not miss each other. Cycle completion is guaranteed by timeout (1ms).
- Access through JTAG does not involve the microcontroller at all.

4.1.1.4 I^2C Master

4.1.1.4.1 Description

Alpine-Ridge DP has an internal I^2C master in order to communicate with external controllers. Alpine-Ridge DP I^2C master supports clock stretching. Alpine-Ridge DP I^2C master does not support a multi-master environment.

4.1.1.5 I²C Slave

4.1.1.5.1 Description

I²C Slave module is used in Alpine-Ridge DP in order to provide additional access to the chip (similar to JTAG access) through external interface but using reduced pin count (two overall: clock & data). I²C has a serial Interface which internally transforms into parallel data. I²C main function is to act as slave and provide read/write access to chip target bus.

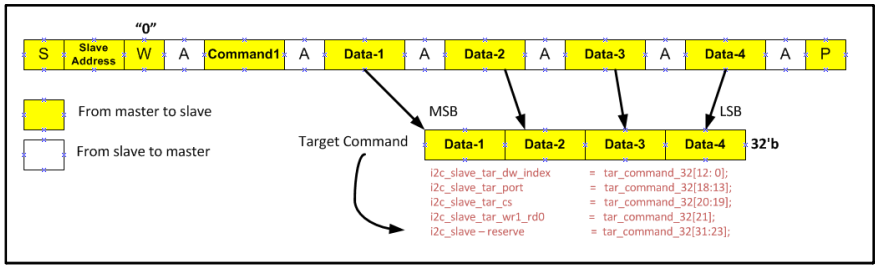
4.1.1.5.2 Write/Read transaction in I²C protocol

Write Command in I²C protocol

I²C Slave supports 4 unique commands:

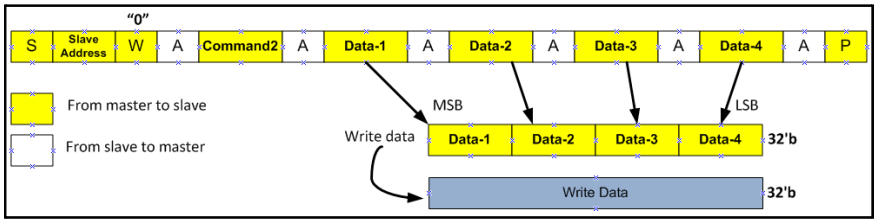
Command #1 (8'd1): Access Target Bus, see Figure 10.

Figure 10. I²C Command #1



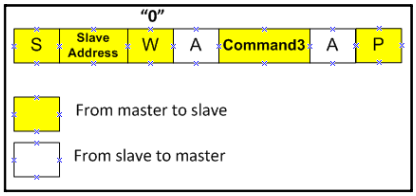
Command #2 (8'd2): Write into Target Bus, see Figure 11.

Figure 11. I²C Command #2



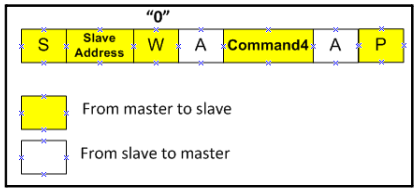
Command #3 (8'd3): Read previous target command data bus. See Figure 12.

Figure 12. I²C Command #3



Command #4 (8'd4): Read previous write data Bus. See Figure 13.

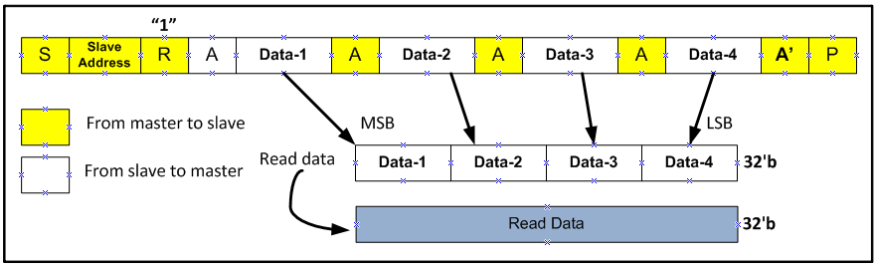
Figure 13. I²C Command #4



Read Command in I²C protocol

There are 3 sources of data for the read command: from Target Bus, from previous target command data bus or from previous write data bus. The source of data is selected using the write command and the data is then read using the read command. See Figure 14.

Figure 14. I²C Read Command



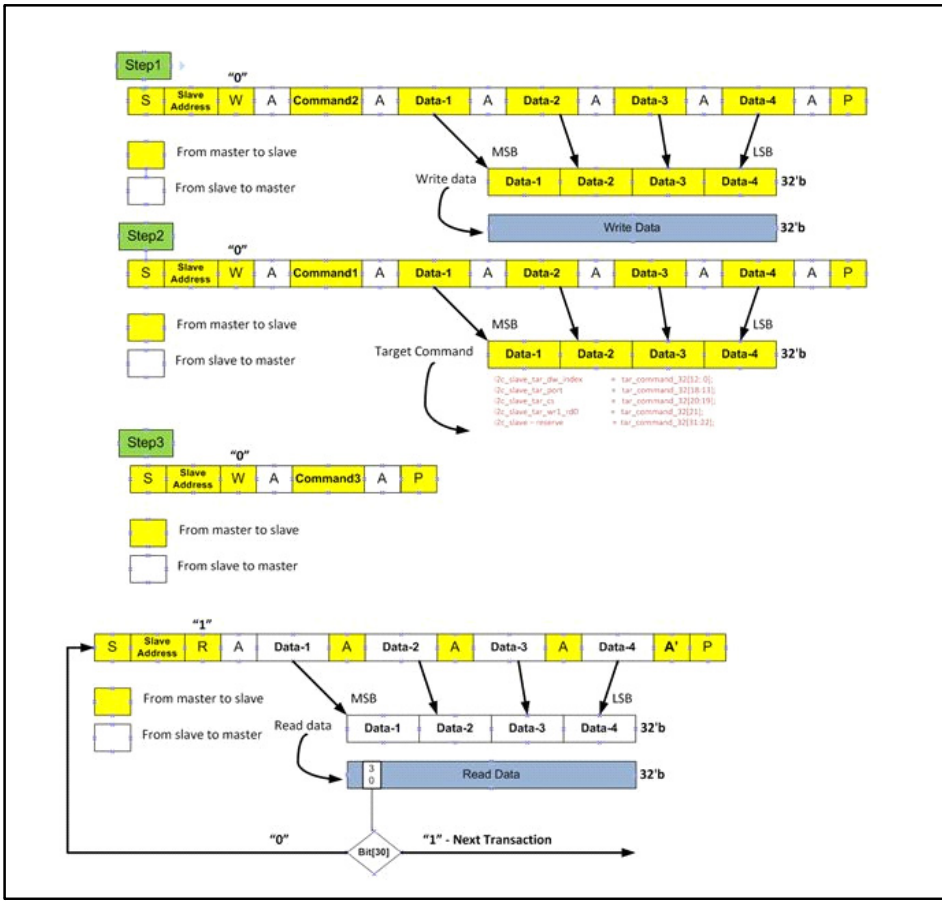
Write flow step-by-step

Master write into target bus

- Step1: master writes command #2 + write data - load data that will be written to target bus.
- Step2: master writes command #1 + target command - target access details, wr1_rd0 bit set to 1 for write mode.
- Step3: master reads data, poles acknowledge bit:
  - a. Write command #3
  - b. Read data using Read Command
  - c. Check bit 30, repeat reading (step b) until bit 30 is read 1 - acknowledge of write transaction

See also Figure 15.

Figure 15. I²C Write Flow Step-By-Step



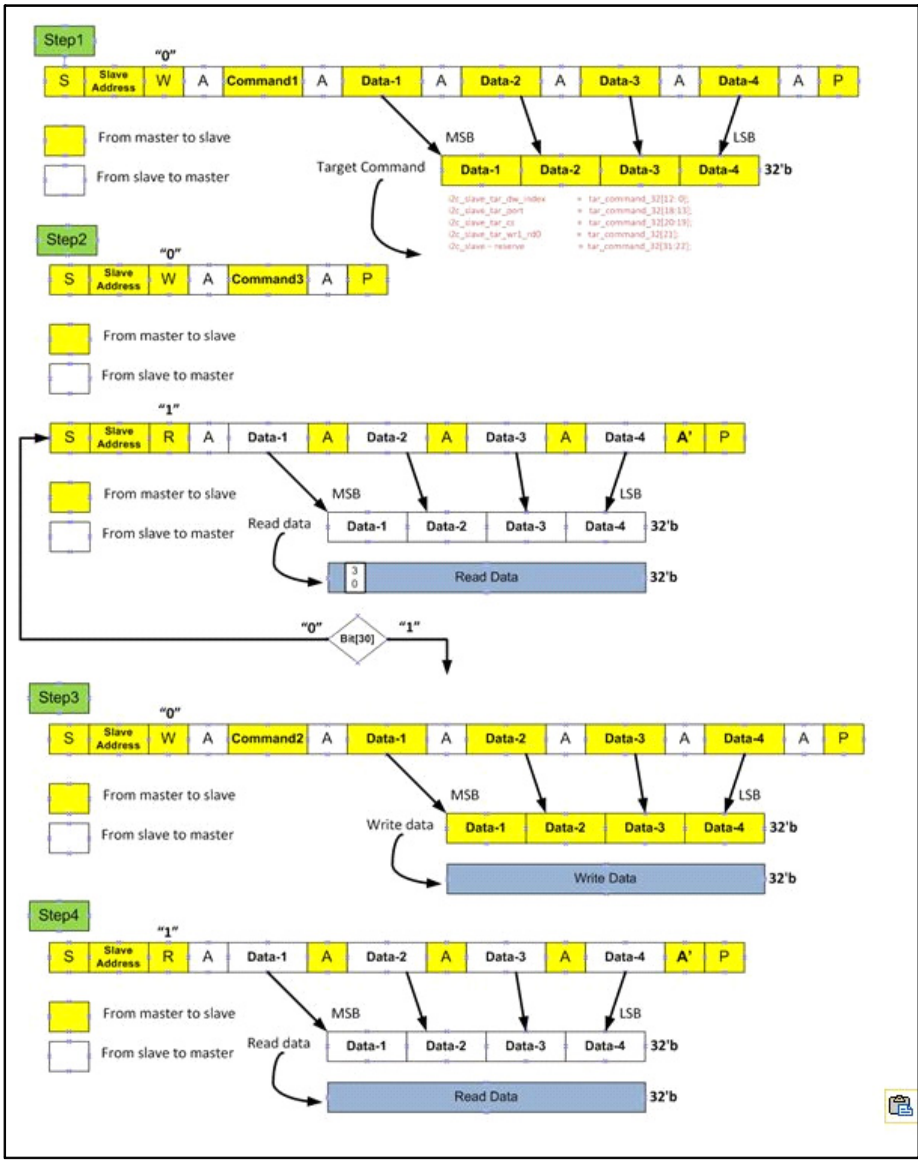
Read flow step-by-step

Master read from target bus

- Step1: Master writes command #1 + target command - target access details, wr1_rd0 bit set to 0 for read mode.
- Step2: Master reads data, poles acknowledge bit:
  - a. write command #3
  - b. Read data using Read Command
  - c. Check bit 30, repeat reading (step b) until bit 30 is read 1
- Step3: Master writes command #2 + dummy write data - dummy load data, data loaded will not be used.
- ..tep4: Master reads data using Read Command - data is received from target bus.

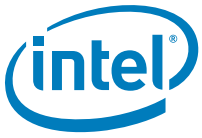
See also Figure 16.

Figure 16. I2C Read Flow Step-By-Step



4.1.2 Internal CIO Switch and PCIe Switch Registers

These are internal implementation registers, which result in "mirroring" other registers, some from CIO specification, others of other registers in the chip. These can be accessed either by a JTAG command or through the FLASH Target Bus access mechanism.



4.1.2.1 JTAG Access

Accomplished JTAG Access is accomplished in the same way as a regular JTAG Access to the Target Bus (like writing a Configuration Space Register), except that bit 22 of the command must be set.

4.1.2.2 Flash Memory Access

Flash Memory Access is accomplished in the same way as a regular Flash Access to the Target Bus (like writing a Configuration Space Register), except that bit 22 of the command must be set.

4.1.3 Configuration Through Flash Memory

The Flash Memory is used for setting initial values to specific registers in the chip.

Upon reset, the value from the Flash Memory field is read into the appropriate registered bit. Some of these registered bits cannot be written in any other way except Flash Memory access, others can be changed by a regular Target Access.

4.1.4 DP 8051

The dp_8051 module contains the 8051 controller (from Synopsys DesignWare) with its memories. It also contains an interface to the host as part of the memory space. The memory space is for three kinds of memories: External RAM, External ROM and Host Interface. In addition, it contains a Serial Port interface.

In order to enable patches to the ROM there is a mechanism that enables patches by Flash Memory write or by Target accesses. The number of dp_8051 instances is as the number of physical DP ports, 5 in Alpine-Ridge DP.

Data Flow

The dp_8051 contains a number of flows for data:

1 Data to the External memories and the host can be written in the following ways:
   - a.Target access: from CIO port (or external CPU) data can be written to the external memories, Host interface and the Patch registers.
   - b. DW8051 memory access: the 8051 core can access its internal and external memories including the host interface, as part of the firmware that is programmed in the ROM.

2 Data to patch registers and external RAM is written in 2 ways:
   - a. Flash Memory: During initialization of the Alpine-Ridge DP the Flash Memory automatically writes the patch registers and the relevant space in the External RAM for patches.
   - b. Target access: The user may override the Flash Memory settings of the patch registers and the external RAM by writing to the Target interface.

3 JTAG Access: The JTAG machine can access the host interface directly when DFT mode is enabled.

Register Access

Accessing the DP_8051 registers is done indirectly through the DP Vendor Specific Configuration Register Attributes register, as follows:

Write sequence for ROM, RAM and Host:

1 Write to Ip_addr register.

2 Write to Ip_wdata register.

3 Write to Ip_cmd register.

4 Poll ip_vld bit. If it is cleared, next write can proceed.

Read sequence for ROM, RAM and Host:

1 Write to Ip_addr register.

2 Write to Ip_cmd register.

3 Poll ip_vld bit. If it is cleared read Ip_rdata.

Write sequence for Patch Registers:

1 Write to Ip_patch Control register to assert SW reset for the 8051. Wait at least 500 ns for the reset to take effect.

2 Write to one of the ip_patch registers with valid bit asserted.

3 Write the corresponding space in the External RAM. Note that the data should contain 3 bytes, which is actually a 3 bytes command. The command should be a Long Jump command (0x2) which will point to another space in the RAM.

4 rite to Ip_patch Control register to release SW reset for the 8051 (reset needs to be asserted for at least 8 cycles of Host DP clock).

4.1.5 DP IP Registers

IP registers in the DP can be accessed through the 8051 either by Target Access through the Control Port or by the JTAG Mechanism.

4.1.5.1 Access to DP Registers via Control Port

This is accomplished in the same way as writing to the 8051 registers, but the Data field is only 8 bits wide.

Looking at the Address accessed, the 8051 will translate the command to the IP Host Interface.

4.1.5.2 Access to DP Registers via JTAG

The Memory in the DP (in and out) can be accessed via JTAG. Addresses can be accessed by bytes only. The RDV_DOMAIN must be powered on, CIO_DOMAIN may be powered off. The Write and Read flows are described below.

Write flow

1 Insert DP_ADDR_RX_REG instruction (6'b011101) to IR.

2 Insert 13 bits of the base address to write to JTAG DR and 3 bits to choose the port (000=DPout; 001=DP in 1; 010-DP in2; 011 - PA; 100 -PB).

3 Insert DP_WR_RX_REG instruction (6'b011110) to IR.

4 Insert 8 bits of the data that you want to write Insert DP_EXE_RX_REG instruction (6'b011111) to IR.

Read flow

1 Insert DP_ADDR_RX_REG instruction (6'b011101) to IR.

2 Insert 13 bits of the base address to write to JTAG DR and 3 bits to choose the port (000=DPout; 001=DP in 1; 010-DP in2; 011 - PA; 100 -PB).

3 Insert DP_EXE_RX_REG instruction (6'b011111) to IR.

4 Insert DP_READ_RX_REG instruction (6'b100111) to IR.

5 Shift data out to TDO by inserting 00000000 to Jtag (8 bits of data).

DP registers will be selected according to bit [13]:

0 = DP mode

4.1.5.3 Access to DP Registers via JTAG by Control Port

Write flow

First give the address of the register to be accessed.

- Write the address of DP register to be written to, to register IP_ADDR in DP Vendor Specific Registers (See "Display Port (DP)" on page 244), i.e. register 0x51 for SRC and 0x91 for SNK.
- Insert CTRL_PORT_DATA instruction (6'b111001) to IR.
- Insert 32 bits of register address to write to JTAG DR. Push to TDI, start from MSB. For example, if the data is to be read from register B48, insert to TDI 32'h0000CB48.
- Insert CTRL_PORT_CMD instruction (6'b111000) to IR.
- Insert 32 bits of command to JTAG DR. Push to TDI, start from MSB.

Structure: {Reserved[7'h0], Command[4'b1], Configuration Space[2'b01], Port[6'd10/6'd11/6'd12], DWIndex[13'h51/13'h91}.

Write the data to be written to register IP_RDATA in DP Vendor Specific Registers (See "Display Port (DP)" on page 244), i.e. register 0x52 for SRC and 0x92 for SNK.

- Insert CTRL_PORT_DATA instruction (6'b111001) to IR.
- Insert 32 bits of register address to write to JTAG DR. Push to TDI, start from MSB.
- Insert CTRL_PORT_CMD instruction (6'b111000) to IR.
- Insert 32 bits of command to JTAG DR. Push to TDI, start from MSB.

Structure: {Reserved[7'h00], Command[4'b1], Configuration Space[2'b01], Port[6'd10/6'd11/6'd12], DWIndex[13'h52/13'h92]}.

Write the command to be performed on the register (write in this case), to register IP_CMD in DP Vendor Specific Registers (See "Display Port (DP)" on page 244), i.e. register 0x50 for SRC and 0x90 for SNK:

- Insert CTRL_PORT_DATA instruction (6'b111001) to IR.
- Insert 32 bits of command to JTAG DR. Push to TDI, **start from MSB**.
- The write command is: 32'h00000003
- Insert CTRL_PORT_CMD instruction (6'b111000) to IR.
- Insert 32 bits of command to JTAG DR. Push to TDI, **start from MSB**.

Structure: {Reserved[7'h0], Command[4'b1], Configuration Space[2'b01], Port[6'd10/6'd11/6'd12], DWIndex[13'h50/13'h90]}.

Write will be executed by Control Port.

Read flow

First give the address of the register to be accessed.

Write the address of DP register to register IP_ADDR in DP Vendor Specific Registers (See "Display Port (DP)" on page 244), i.e. register 0x51 for SRC and 0x91 for SNK.

- Insert CTRL_PORT_DATA instruction (6'b111001) to IR.
- Insert 32 bits of register address to JTAG DR. Push to TDI, start from MSB. For example, if the data is to be read from register B48, insert to TDI 32'h0000CB48.
- Insert CTRL_PORT_CMD instruction (6'b111000) to IR.
- Insert 32 bits of command to JTAG DR. Push to TDI, start from MSB.

Structure: {Reserved[7'h0], Command[4'b1], Configuration Space[2'b01], Port[6'd10/6'd11/6'd12], DWIndex[13'h51/13'h91}.

Write the command to be performed on the register (read in this case) to register IP_CMD in DP Vendor Specific Registers (See "Display Port (DP)" on page 244), i.e. register 0x50 for SRC and 0x90 for SNK

- Insert CTRL_PORT_DATA instruction (6'b111001) to IR.
- Insert 32 bits of command to JTAG DR. Push to TDI, start from MSB.
- The read command is: 32'h00000001
- Insert CTRL_PORT_CMD instruction (6'b111000) to IR.
- Insert 32 bits of command to JTAG DR. Push to TDI, start from MSB.

Structure: {Reserved[7'h0], Command[4'b1], Configuration Space[2'b01], Port[6'd10/6'd11/6'd12], DWIndex[13'h50/13'h90]}.

- Writing will be executed by Control Port.

Read the data of DP register from register IP_RDATA in DP Vendor Specific Registers (See "Display Port (DP)" on page 244), i.e. register 0x53 for SRC and 0x93 for SNK

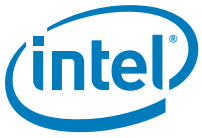
- Insert CTRL_PORT_CMD instruction (6'b111000) to IR.
- Insert 32 bits of command to JTAG DR. Push to TDI, start from MSB.

Structure: {Reserved [7'h0], Command [4'b0], Configuration Space [2'b01], Port [6'd10/6'd11/6'd12], DWIndex[13'h53/13'h93]}.

- Insert CTRL_PORT_READ instruction (6'b111010) to IR.
- Wait 1 ms.
- Push 32 bits to TDI and collect read data from TDO. MSB is read first.

4.1.6 DP OUT CPU

These registers can be accessed indirectly through the DP OUT TMU Configuration Register Attribute register (TMU_DP_CS_2, TMU_DP_CS_3 and TMU_DP_CS_4 - see "Display Port (DP) OUT" on page 241).



Command bits:

- 31: 1 = read, 0 = write.
- 12: 1 = Access to Compute Engine's Control Store, 0 = Access Compute Engine's Register Block.
- 6:0: Low order address field. Control Store address uses bits 6:0. Register Block uses bits 3:0.

On write requests, data should be written prior to issuing the command.

4.1.7 TMU uCTL

Access to the uCTL is through registers VSEC_TMU_CS_22-24 (see "TMU Vendor Specific Registers" on page 125).

uCTL command (in VSEC_TMU_CS_22) description:

imem_ready - bit 31 - Should be set to 1 only when the software has finished loading the iRAM and does not require to access it anymore, i.e., the software can read/write from/to the iRAM only while this bit is 0 - when the bit is set to 1, the software prevents the uCTL from accessing the iRAM.

go - bit 20 - This bit is set to 1 by the software to initiate an operation. It is cleared by hardware when the operation is complete.

op - bits 18:16 -

- 3'd0 - rd_imem: Read from addr[8:0] of iRAM - the data is returned through VSEC_TMU_CS_24[31:0] when the operation is complete.
- 3'd1 - wr_imem: Write VSEC_TMU_CS_23[31:0] to addr[8:0] of iRAM - the same data is returned on VSEC_TMU_CS_24 [31:0] when the operation is complete.
  - While writing to iRAM, keep the upper 4 bits of the data set to4'b0000, otherwise it will be considered as trapping info:
  - VSEC_TMU_CS_23 [31:28] represents the number of the trap, VSEC_TMU_CS_23 [9:0] is from-iROM-address, VSEC_TMU_CS_23 [23:16] is to-iRAM-address.
  - Any time the program counter goes through from-iROM-address it will jump to to-iRAM-address.
  - When such a write is performed, a corresponding bit in the trap_valid vector is set to indicate the validity of this trap.
- 3'd2 - rd_trap_valid: Read trap_valid vector - the vector is returned through VSEC_TMU_CS_24 [31:0] when the operation is complete.
- 3'd3 - wr_trap_valid: Write trap_valid vector. This is mainly for the debug option or to cancel some trapping by clearing its correspondent valid bit in the vector.
- The same data is returned on VSEC_TMU_CS_24 [31:0] when the operation is done.
- 3'd4 - rd_sfr: Read various registers like ISR, IMR, and some GPRs according to addr[3:0] - the data is returned on VSEC_TMU_CS_24 [31:0] when the operation is complete.
- 3'd5 - wr_sfr: Write various registers like ISR, IMR, and some GPR's according to addr[3:0] - the same data is returned on VSEC_TMU_CS_24 [31:0] when the operation is complete.
- 3'd6 - clear: Clear the history of the filters. In the next calculation no averaging is complete.
- 3'd7 - soft_reset: Soft reset of the uCTL.

addr - bits 8:0 - Address to access iRAM or various registers (in conjunction with op).

4.2 Register Terminology

See Table 18:

Table 18. Register Terminology

Shorthand	Description
R/W	Read/Write. A register with this attribute can be read and written. If written since reset, the value read reflects the value written.
R/W S	Read/Write Status. A register with this attribute can be read and written. This bit represents status of some sort, so the value read may not reflect the value written.
RO	Read Only. If a register is read only, writes to this register have no effect.
WO	Write Only. Reading this register may not return a meaningful value.
R/Clr	Read Clear. A register bit with this attribute is cleared after read. Writes have no effect on the bit value.
W/Clr	Write Clear. A register bit with this attribute is cleared after writing any value.
R/W SC	Read/Write Self Clearing. When written to a 1b the bit causes an action to be initiated. Once the action is complete, the bit returns to 0b. These fields are always read as zero.
R/W1C	Read/Write Clear. A register bit with this attribute can be read and written. However, a Write of a 1b clears (sets to 0b) the corresponding bit and a write of a 0b has no effect.
HwInit	For PCIe registers (from PCI Express Base 2.0 specification). Hardware Initialized – Register bits are initialized by firmware or hardware mechanisms such as pin strapping or serial FLASH. (System firmware hardware initialization is only allowed for system integrated devices). Bits are read only after initialization and can only be reset (for write-once by firmware) with Fundamental Reset. HwInit register bits are not modified by an FLR.
ROS	For PCIe registers (from PCI Express Base 2.0 specification). Sticky - Read-only – Register bits are read-only and cannot be altered by software. Bits are neither initialized nor modified by hot reset or FLR. Where noted, devices that consume AUX power must preserve sticky register values when AUX power consumption (via either AUX power or PME Enable) is enabled. In these cases, registers are neither initialized nor modified by hot, warm, or cold reset.
RsvdP	For PCIe registers (from PCI Express Base 2.0 specification). Reserved and Preserved – Reserved for future R/W implementations. Registers are read-only and must return zero when read. Software must preserve the value read for writes to bits.
RsvdZ	For PCIe registers (from PCI Express Base 2.0 specification). Reserved and Zero – Reserved for future RW1C implementations. Registers are read-only and must return zero when read. Software must use 0b for writes to bits.

4.3 CIO Configuration Space

The CIO control path protocol uses four configuration spaces. These are:

- Device configuration space: This must be implemented by all Switches in a CIO topology. This configuration space is implemented per-switch and represents the configuration space of the control port of the switch. This configuration space is used to query Switch capabilities, to assign an address for the switch and to set the default route.
- Port configuration space: This must be implemented by all switches in a CIO topology. This configuration space is implemented separately for each port of the switch. This configuration space is used to query port capabilities and to keep per-port error statistics.
- Path configuration space: This must be implemented by all switches in a CIO topology. This configuration space is implemented separately for each port of the switch. This configuration space is used to setup and tear down paths through the switch.

- Counters configuration space: This configuration space is optional and may be implemented by a CIO switch. This configuration space is implemented separately for each port of the switch. This configuration space is used to collect performance statistics for a set of selected paths.

The four configuration spaces are described in the following sections.

Note: The offset field in this chapter refers to the double word index of the register.

4.3.1 Device Configuration Space

Note: The offset field in this chapter refers to the double word index of the register.

Figure 17. Device Configuration Space

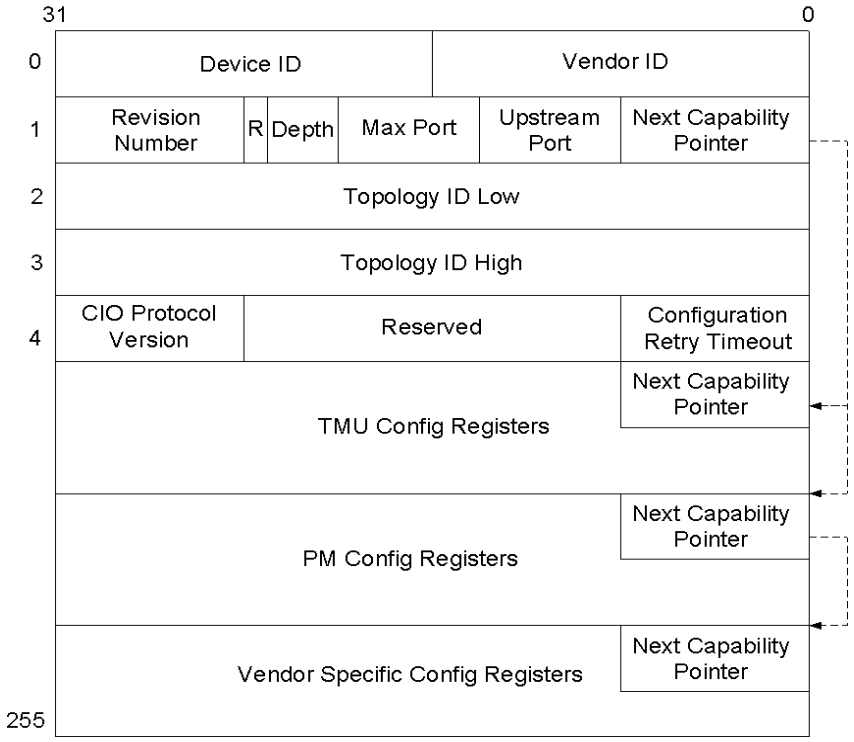


Figure 17 shows the device configuration space registers that must be implemented by every CIO Switch. The device configuration space has a total of 256 double-words. The first four double-words describe the basic attributes of a CIO Switch. The remaining 252 double-words are organized into a linked list of optional or required capability structures. The required capabilities include Time Management and Power Management configuration registers. Vendor specific capability structure is optional. Table 19 specifies the next capability pointers of the device configuration space.

Table 19. Next Capability Pointers for Device Configuration Space

Pointer Name	Pointer Value [decimal]	Comments
DEV_TMU_CFG_BASE	5	

Table 19. Next Capability Pointers for Device Configuration Space

Pointer Name	Pointer Value [decimal]	Comments
DEV_PM_CFG_BASE	N/A	None
DEV_VSEC_0_BASE	32	I^2C access registers
DEV_VSEC_1_BASE	40	custom DFT registers
DEV_VSEC_2_BASE	99	ANA registers
DEV_VSEC_3_BASE	121	TMU DFT registers, device specific, common to all ports
DEV_VSEC_4_BASE	172	GPIO
DEV_VSEC_5_BASE	207	SWless
DEV_VSEC_6_BASE	255	Link controller
DEV_VSEC_7_BASE	1024	Flash controller
DEV_VSEC_8_BASE	NA	Reserved
DEV_VSEC_9_BASE	1728	TBT Phy
DEV_VSEC_10_BASE	4087	USB

4.3.1.1 Basic Configuration

The basic attributes of the device configuration space registers are described in Table 20.

Table 20. Device Configuration Register Basic Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	DEVICE_CS_0	15:0	Vendor ID This field identifies the manufacturer of the device.	RO	0x8086
0	DEVICE_CS_0	31:16	Device ID This field is assigned by the manufacturer and identifies the type of the device.	R/W	0x1578
1	DEVICE_CS_1	7:0	Next Capability Pointer This filed defines the double word index of the first capability register set in the device configuration space.	RO	See Pointer in Table 19

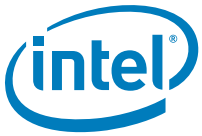


Table 20. Device Configuration Register Basic Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
1	DEVICE_CS_1	13:8	Upstream Port This field specifies the port that connects the Switch to its parent Switch in the Domain's tree topology. On the Root Switch, this port specifies the interface to the Connection Manager. On reset, this field may be loaded with a default value through hardware strapping or other mechanism. This field may be overridden by a subsequent configuration message. A value of 0 for an un-initialized device means that there is no default value for the Upstream port. If enabled, loaded from FLASH (see FLASH map, byte 0x18).	R/W	0
1	DEVICE_CS_1	19:14	Max Port This field specifies the highest numbered port of the CIO Switch. All the ports of a Switch must be numbered sequentially. Therefore, the number of ports in the Switch is given by (Max Port + 1). This includes the control port (port 0).	RO	12
1	DEVICE_CS_1	22:20	Depth This field specifies the depth of the Switch in the CIO tree topology. It is set by the Connection Manager. On reset, this field must be initialized to 0. The Root Switch has a Depth of 0.	R/W	0
1	DEVICE_CS_1	23	Reserved Must be set to 0.	RO	0
1	DEVICE_CS_1	31:24	Revision Number This value is assigned by the manufacturer and identifies the revision number of the device.	RO	0
2	DEVICE_CS_2	31:0	TopologyID Low This field contains the topological address assigned to the device by the Connection Manager. This field must be set to 0 on reset.	R/W	0
3	DEVICE_CS_3	30:0	TopologyID High This field contains the topological address assigned to the device by the Connection Manager. This field must be set to 0 on reset.	R/W	0
3	DEVICE_CS_3	31	TopologyID Valid The MSB bit of the TopologyID configuration register is a valid flag. The valid flag is set to 0 on reset and is set to 1 by the Connection Manager when the TopologyID is initialized. All the reserved bits of the TopologyID field must be set to 0. See CIO Spec for usage details.	R/W	0
4	DEVICE_CS_4	7:0	Configuration Retry Timeout This field specifies the timeout value in milliseconds that is used by the Control Port to retry ERROR notification and PLUG_EVENT packets.	R/W	0xA

Table 20. Device Configuration Register Basic Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
4	DEVICE_CS_4	23:8	Reserved Must be set to 0.	RO	0
4	DEVICE_CS_4	31:24	CIO Version This field specifies the version of the CIO Transport layer protocol that is supported by the Switch implementation.	R/W	2

4.3.1.2 TMU Configuration

Figure 18 shows the configuration registers in the device configuration space for the Time Sync capability register set. The register attributes are described in Table 19 Implementations must support atomic read and write of all multi-double word configuration registers.

Note: The register offset is relative to DEV_TMU_CFG_BASE in Table 19.

Figure 18. Time Sync Device Configuration Space Registers

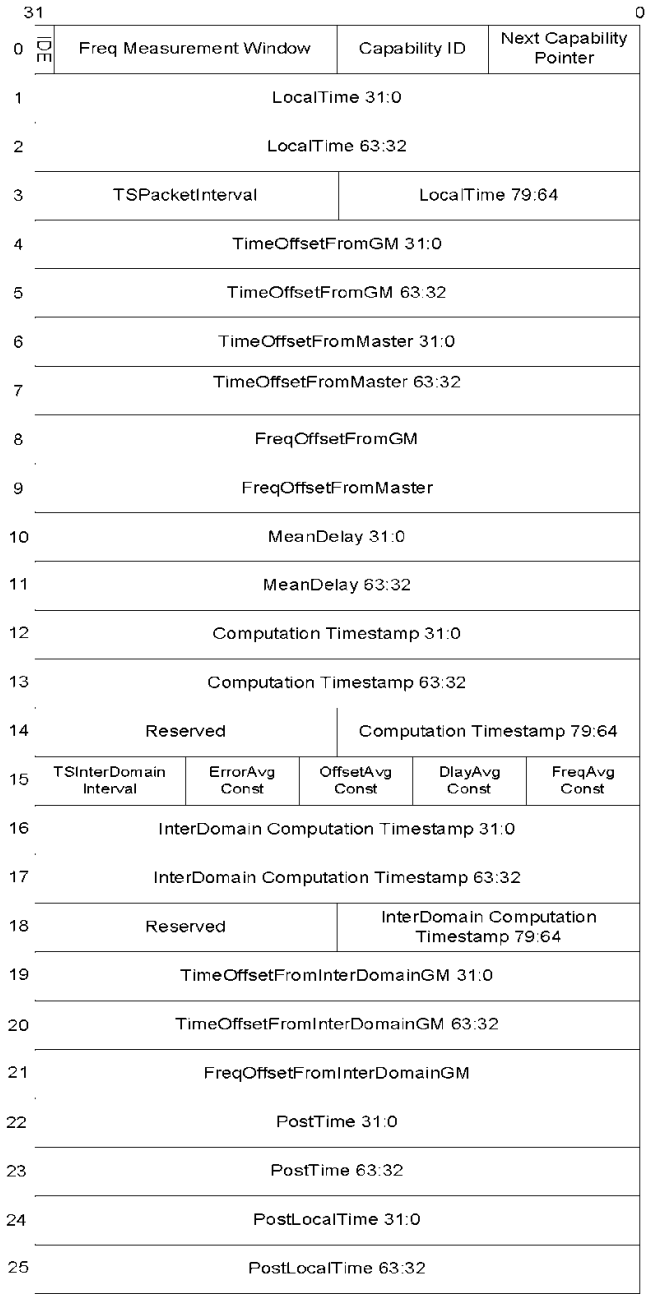


Table 21. Time Sync Device Configuration Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	TMU_DEV_CS_0	7:0	Next Capability Pointer This field defines the doubleword index of the next capability register set in the device configuration space. It is set to 00h if this is the last set in the device configuration space.	RO	See Pointer in Table 19
0	TMU_DEV_CS_0	15:8	Capability ID This field must contain the value 03h indicating this is the start of the Time Sync capability register set.	RO	3
0	TMU_DEV_CS_0	30:16	Freq Measurement Window This register specifies the number of Time Sync packet exchanges that must occur before the frequency ratio and frequency offset are computed.	R/W	800
0	TMU_DEV_CS_0	31	Inter-Domain Enable (IDE) This flag must be set to 1 to enable the Root Switch of a domain to start receiving Inter-Domain Timestamp packets. When set to 0, the Inter-Domain Timestamp packets are discarded by the Root Switch. This flag has no effect on other Switches in the domain.	R/W	0
1	TMU_DEV_CS_1	31:0	LocalTime 31:0 This register contains the least significant 32 bits of the 80-bit LocalTime counterOn reset, this register must default to 0.	RO	0
2	TMU_DEV_CS_2	31:0	LocalTime 63:32 This register contains the next higher 32 bits of the 80-bit LocalTime counter. On reset, this register must default to 0.	RO	0
3	TMU_DEV_CS_3	15:0	LocalTime 79:64 This register contains the most significant 16 bits of the 80-bit LocalTime counterUpon reset, this register must default to 0.	RO	0
3	TMU_DEV_CS_3	31:16	TSPacketInterval This register field encodes the time interval between successive transmissions of the Delay Request TSNOS on a link. The time interval is specified in 1024 nanoseconds. Setting this register to 0 disables the Time Sync packet exchange on the port. The default value of this register is 16.	R/W	16

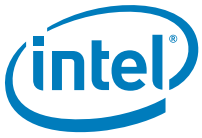


Table 21. Time Sync Device Configuration Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
4	TMU_DEV_CS_4	31:0	TimeOffsetFromGM 31:0 This register contains the least significant 32 bits of the computed time offset between LocalClock entity and the Root Switch's LocalClock entity Upon reset this register must default to 0. The value of this register is the result obtained from Equation (10).	RO	0
5	TMU_DEV_CS_5	31:0	TimeOffsetFromGM 63:32 This register contains the most significant 32 bits of the computed time offset between LocalClock entity and the Root Switch's LocalClock entity Upon reset this register must default to 0. The value of this register is the result obtained from Equation (10).	RO	0
6	TMU_DEV_CS_6	31:0	TimeOffsetFromMaster 31:0 This register contains the least significant 32 bits of the computed time offset between LocalClock entity and the master's LocalClock entityUpon reset this register must default to 0. The value of this register is the result obtained from Equation (8).	R0	0
7	TMU_DEV_CS_7	31:0	TimeOffsetFromMaster 63:32 This register contains the most significant 32 bits of the computed time offset between LocalClock entity and the master's LocalClock entityUpon reset this register must default to 0. The value of this register is the result obtained from Equation (8).	RO	0
8	TMU_DEV_CS_8	31:0	FreqOffsetFromGM This register contains the computed frequency offset between the LocalClock entity and the Root Switch's LocalClock entity represented using 2's complement format. On reset this register must default to 0. The value of this register is the result obtained from Equation (4).	RO	0
9	TMU_DEV_CS_9	31:0	FreqOffsetFromMaster This register contains the computed frequency offset between the LocalClock entity and the master's LocalClock entity represented using 2's complement format. On reset this register must default to 0. The value of this register is the result obtained from Equation (2).	RO	0

Table 21. Time Sync Device Configuration Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
10	TMU_DEV_CS_10	31:0	MeanDelay 31:0 This register contains the least significant 32 bits of the computed time delay between the slave and the master Switches. This register has the same format as the TimeOffsetFromGM register shown in On reset this register must default to 0. The value of this register is the result obtained from Equation (5).	RO	0
11	TMU_DEV_CS_11	31:0	MeanDelay 63:32 This register contains the most significant 32 bits of the computed time delay between the slave and the master Switches. This register has the same format as the TimeOffsetFromGM register. On reset this register must default to 0. The value of this register is the result obtained from Equation (5).	RO	0
12	TMU_DEV_CS_12	31:0	Computation Timestamp 31:0 This register contains the least significant 32 bits of the most recent value of the t4[n] obtained at the conclusion of a Time Sync packet exchange between the Switch and it's master in the same domain. On reset this register must be set to 0.	RO	0
13	TMU_DEV_CS_13	31:0	Computation Timestamp 63:32 This register contains the next higher 32 bits of the most recent value of the t4[n] obtained at the conclusion of a Time Sync packet exchange between the Switch and it's master in the same domain. On reset this register must be set to 0.	RO	0
14	TMU_DEV_CS_14	15:0	Computation Timestamp 79:64 This register contains the most significant 16 bits of the most recent value of the t4[n] obtained at the conclusion of a Time Sync packet exchange between the Switch and it's master in the same domain. On reset this register must be set to 0.	RO	0
14	TMU_DEV_CS_14	31:16	Reserved Must be set to 0.	RO	0
15	TMU_DEV_CS_15	5:0	FreqAvgConst This register specifies the IIR filter co-efficient used to average the frequency ratio. The IIR filter co-efficient is given by (1/2^FreqAvgConst). On reset this register must be set to 4.	R/W	8

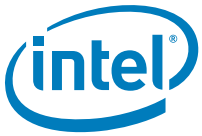


Table 21. Time Sync Device Configuration Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
15	TMU_DEV_CS_15	11:6	DelayAvgConst This register specifies the IIR filter co-efficient used to average the propagation delay. The IIR filter co-efficient is given by (1/2^DelayAvgConst). On reset this register must be set to 4.	R/W	8
15	TMU_DEV_CS_15	17:12	OffsetAvgConst This register specifies the IIR filter co-efficient used to average the time offset. The IIR filter co-efficient is given by (1/2^OffsetAvgConst). On reset this register must be set to 4.	R/W	8
15	TMU_DEV_CS_15	23:18	ErrorAvgConst This register specifies the IIR filter co-efficient used to average the time offset averaging error. The IIR filter co-efficient is given by (1/2^ErrorAvgConst). On reset this register must be set to 4.	R/W	8
15	TMU_DEV_CS_15	31:24	TSInterDomainInterval This register field encodes the time interval between the transmissions of Inter-domain Timestamp packets. The time interval in microseconds is specified by (TSInterDomainInterval + 1) * TSPacketInterval. If this register is set to 0, Inter-domain Timestamp packets are transmitted once per TimeSync packet exchange. The default value of this register is 0.	R/W	0
16	TMU_DEV_CS_16	31:0	InterDomain Computation Timestamp 31:0 On an inter-domain slave Switch, this register contains the least significant 32 bits of the computed value of the inter-domain timestamp. The value of this register is obtained from (11). On all other Switches, this register contains the least significant 32 bits of the most recent value of the Interdomain Timestamp value contained in the Follow Up packet received from Switch x's master. On reset this register must be set to 0.	RO	0

Table 21. Time Sync Device Configuration Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
17	TMU_DEV_CS_17	31:0	InterDomain Computation Timestamp 63:32 On an inter-domain slave Switch, this register contains the next higher 32 bits of the computed value of the inter-domain timestamp. The value of this register is obtained from (11). On all other Switches, this register contains the next higher 32 bits of the most recent value of the Interdomain Timestamp value contained in the Follow Up packet received from Switch x's master. On reset this register must be set to 0.	RO	0
18	TMU_DEV_CS_18	15:0	InterDomain Computation Timestamp 79:64 On an inter-domain slave Switch, this register contains the most significant 32 bits of the computed value of the inter-domain timestamp. The value of this register is obtained from (11). On all other Switches, this register contains the most significant 32 bits of the most recent value of the Interdomain Timestamp value contained in the Follow Up packet received from Switch x's master. On reset this register must be set to 0.	RO	0
18	TMU_DEV_CS_18	31:16	Reserved Must be set to 0.	RO	0
19	TMU_DEV_CS_19	31:0	TimeOffsetFromInterDomainGM 31:0 On an inter-domain slave Switch, this register contains the least significant 32 bits of the computed time offset between the local domain Root Switch's LocalClock entity and the grandmaster domain Root Switch's LocalClock entityThe value of this register is the result obtained from Equation (22). On all other Switches, this register contains the most recent value of the TimeOffsetFromInterDomainGM contained in the Follow Up packet received from Switch x's master. On reset this register must be set to 0.	RO	0

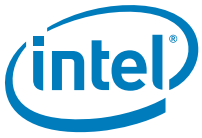


Table 21. Time Sync Device Configuration Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
20	TMU_DEV_CS_20	31:0	TimeOffsetFromInterDomainGM 63:32 On an inter-domain slave Switch, this register contains the most significant 32 bits of the computed time offset between the local domain Root Switch's LocalClock entity and the grandmaster domain Root Switch's LocalClock entity. The format of this register is shown in. The value of this register is the result obtained from Equation (22). On all other Switches, this register contains the most recent value of the TimeOffsetFromInterDomainGM contained in the Follow Up packet received from Switch x's master. On reset this register must be set to 0.	RO	0
21	TMU_DEV_CS_21	31:0	FreqOffsetFromInterDomainGM On an inter-domain slave Switch, this register contains the computed frequency offset between the local domain Root Switch's LocalClock entity and the grandmaster domain Root Switch's LocalClock entity represented using 2's complement format. The value of this register is the result obtained from Equation (15). On all other Switches, this register contains the most recent value of the FrequencyOffsetFromInterDomainGM contained in the Follow Up packet received from Switch x's master. On reset this register must default to 0.	RO	0
22	TMU_DEV_CS_22	31:0	Post Local Time 31:0 This register specifies the value that is used to update the least significant 32 bits of the nanoseconds field of the Local Time register when the PostTime matches the CIO Time. On reset, this register must default to 0.	R/W	0
23	TMU_DEV_CS_23	31:0	Post Local Time 63:32 This register specifies the value that is used to update the most significant 32 bits of the nanoseconds field of the Local Time register when the PostTime matches the CIO Time. On reset, this register must default to 0.	R/W	0
24	TMU_DEV_CS_24	31:0	Post Time 31:0 This register specifies the least significant 32 bits of the nanoseconds field of the CIO Time register at which the software updates to the LocalTime register must be applied. On reset, this register must default to 0.	R/W	0

Table 21. Time Sync Device Configuration Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
25	TMU_DEV_CS_25	31:0	Post Time 63:32 This register specifies the most significant 32 bits of the nanoseconds field of the CIO Time register at which the software updates to the LocalTime register must be applied. On reset, this register must default to 0.	R/W	0

4.3.1.3 PM Configuration

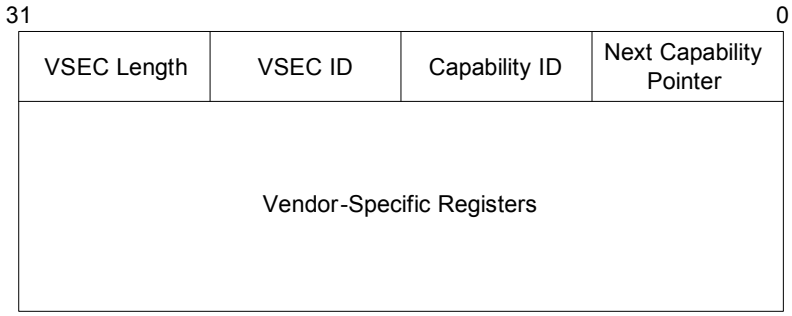
No PM device registers are implemented in the Alpine-Ridge DP.

Note: The register offset is relative to DEV_PM_CFG_BASE in Table 19.

4.3.1.4 Vendor Specific Configuration

The Vendor-Specific capability structure is an optional capability that is permitted to be implemented by any CIO Switch. This allows the CIO Switch vendors to use the device configuration space to expose vendor-specific registers. Multiple Vendor-Specific capability structures are permitted to exist in the device configuration space. Table 18 details the format of the Vendor-Specific capability structure.

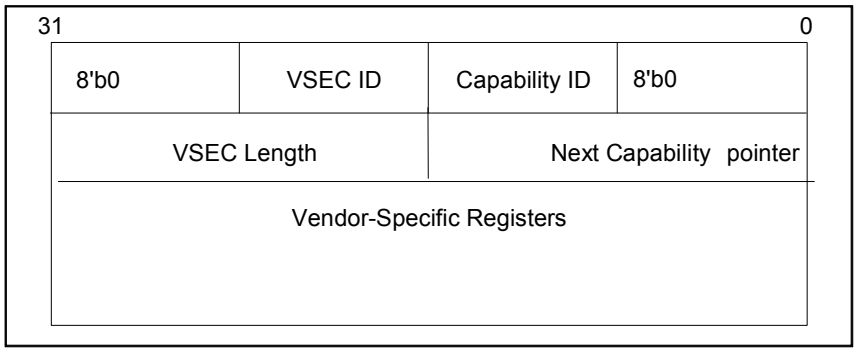
Figure 19. Vendor-Specific Capability Structure



In order to support more than 256 registers defined by a basic CIO - (e.g. for Link Controller registers that reside in VSEC6, which starts at offset 0xFF) - an extension was added.

VSEC that points to a VSEC which is mapped above offset 0xFF, or has a length of more than 0xFF, should have the structure defined in Table 19.

Figure 20. Extended Vendor-Specific Capability Structure



First Double word:

- [31:24] Length =0 // indicates this type of larger VSEC
- [23:16] VSEC ID // legacy
- [15: 8] Cap ID // legacy
- [7: 0] next pointer=0

Second Double word:

- [31:16] Length
- [15: 0] next pointer

Note: Length should be +2, as the header is two double words.

In Alpine-Ridge DP there are seven Vendor Specific capability structures for DFT, I2C, Analog registers, TMU, GPIO, SWless and Link Controller.

4.3.1.4.1 I²C Vendor Specific Registers

The attributes of the I²C vendor-specific capability registers are described in Table 22. These registers reside in the LC power-domain.

Note: The register offset is relative to DEV_VSEC_0_BASE in Table 19.

Table 22. I²C Vendor-Specific Capability Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	VSEC_I2C_CS_0	7:0	Next Capability Pointer This field defines the double word index of the next capability register set in the device configuration space. It is set to 00h if the Vendor-Specific capability register set is the final register set in the linked list of capability register sets in the device configuration space.	RO	See Pointer in Table 19
0	VSEC_I2C_CS_0	15:8	Capability ID This field must contain the value 05h indicating this is the start of the Vendor-Specific capability register set.	RO	5

Table 22. I²C Vendor-Specific Capability Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	VSEC_I2C_CS_0	23:16	VSEC ID This field is a vendor-defined ID number that indicates the nature and format of the VSEC structure.	RO	0
0	VSEC_I2C_CS_0	31:24	VSEC Length This field indicates the number of double words in the entire VSEC structure including the header and the Vendor-Specific registers.	RO	7
1	I2C_PRER	15:0	Clock Prescale This field is used to prescale the SCL clock line. Due to the structure of the I²C interface, the core uses a 5*SCL clock internally. The prescale field must be programmed to this 5*SCL frequency (minus 1). The Prescale value required to set the desired SCL is determined by the following formula: Prescale = 25*10^6/(5*Desired_SCL_Freq[Hz])-1 Change the value of the prescale field only when the I2C Core Enable bit is cleared.	R/W	0xC
1	I2C_PRER	31:16	Reserved Must be set to 0.	RO	0
2	I2C_CTR	2:0	Reserved Must be set to 0.	R0	0
2	I2C_CTR	3	Soft bit to enable 9 stops	R/W	0
2	I2C_CTR	4	Target Lock When the software wants to generate an I²C transaction it must set this bit, make sure that the Controller Lock bit is reset, and only then start the access. When the software completes the access it must clear this bit.	R/W	0
2	I2C_CTR	5	I²C Reset I²C logic soft reset.	R/W	1
2	I2C_CTR	6	Reserved Must be set to 0.	R0	0
2	I2C_CTR	7	I²C Core Enable When set to '1', the I²C core is enabled.	R/W	1
2	I2C_CTR	31:8	Reserved Must be set to 0.	R0	0
3	I2C_TXR	0	Transmit Data LSB In case of a data transfer this bit represents the data's LSB. In case of a slave address transfer this bit represents the RW bit: '1' = reading from slave. '0' = writing to slave.	R/W	0
3	I2C_TXR	7:1	Transmit Data Next byte to transmit via I²C.	R/W	0
3	I2C_TXR	31:8	Reserved Must be set to 0.	R0	0

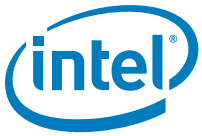


Table 22. I²C Vendor-Specific Capability Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
4	I2C_RXR	7:0	Receive Data Last byte received via I2C.	R0	0
4	I2C_RXR	31:8	Reserved Must be set to 0.	R0	0
5	I2C_CR	2:0	Reserved Must be set to 0.	R/W SC	0
5	I2C_CR	3	Ack When acting as a receiver (reading register), sent ACK (ACK = '0') or NACK (ACK = '1')	R/W	0
5	I2C_CR	4	Write Write to slave.	R/W SC	0
5	I2C_CR	5	Read Read from slave.	R/W SC	0
5	I2C_CR	6	Stop Generate stop condition.	R/W SC	0
5	I2C_CR	7	Start Generate (repeated) start condition.	R/W SC	0
5	I2C_CR	31:8	Reserved Must be set to 0.	R0	0
6	I2C_SR	0	Reserved	R0	0
6	I2C_SR	1	Transfer In Progress '1' when transferring data. '0' when transfer complete.	R0	0
6	I2C_SR	2	Controller Lock When the hardware wants to generate an I²C transaction it must set this bit, make sure that the Target Lock bit is reset, and only then start the access. When the hardware completes the access it must clear this bit.	R0	0
6	I2C_SR	3	Request Failed Indicates that hardware rd/wr request failed due to NACK.	R0	0
6	I2C_SR	4	Reserved Must be set to 0.	R0	0
6	I2C_SR	5	Arbitration Lost This bit is set when the core lost arbitration. Arbitration is lost when: A STOP signal is detected, but not requested. The master drives SDA high, but SDA is low.	R0	0
6	I2C_SR	6	I²C Bus Busy '1' after START signal detected. '0' after STOP signal detected.	R0	0
6	I2C_SR	7	Received Acknowledge This flag represents acknowledge from the addressed slave. '1' = No acknowledge received. '0' = Acknowledge received.	R0	0

Table 22. I²C Vendor-Specific Capability Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
6	I2C_SR	31:8	Reserved Must be set to 0.	R0	0

4.3.1.4.2 DFT Vendor Specific Registers

The attributes of the DFT vendor-specific capability registers are described in Table 23.

Note: The register offset is relative to DEV_VSEC_1_BASE in Table 19.

Table 23. DFT Vendor-Specific Capability Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	VSEC_DFT_CS_0	7:0	**Next Capability Pointer** This field defines the doubleword index of the next capability register set in the device configuration space. It is set to 00h if this is the last register set in the device configuration space.	RO	See Pointer in Table 19
0	VSEC_DFT_CS_0	15:8	**Capability ID** This field must contain the value 05h indicating this is the start of the Vendor-Specific capability register set.	RO	5
0	VSEC_DFT_CS_0	23:16	**VSEC ID** This field is a vendor-defined ID number that indicates the nature and format of the VSEC structure.	RO	1
0	VSEC_DFT_CS_0	31:24	**VSEC Length** This field indicates the number of double words in the entire VSEC structure including the header and the Vendor-Specific registers.	RO	53
1	DFT1	0	**Credit Sync TX Enable** Controls SYNC packets generation by the CIO Switch: 0: disabled. 1: (default) enabled. Loaded from FLASH (if exists) (see FLASH map, byte 0x19 – Section 3.2. Retained throughout CIO reset.	R/W	1
1	DFT1	1	**Disable Target Timeout** Controls Target Bus timeout in case of no response 1ms after Target transaction valid was issued: 0: (default) timeout enabled. 1: timeout disabled. Loaded from FLASH (if exists) (see FLASH map, byte 0x19 – Section Section 3.2).	R/W	0
1	DFT1	2	Disable USB plug event, default loaded from flash - ee_plug_event_control[0]	R/W	0
1	DFT1	3	**Disable plug event of CIO ports** default loaded from flash - ee_plug_event_control[1]	R/W	0

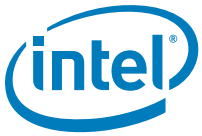


Table 23. DFT Vendor-Specific Capability Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
1	DFT1	4	**Disable plug event of DP OUT0 port** default loaded from flash - ee_plug_event_control[2]	R/W	0
1	DFT1	5	**Disable plug event of DP IN0 port** default loaded from flash - ee_plug_event_control[3]	R/W	0
1	DFT1	6	**Disable plug event of DP IN1 port** default loaded from flash - ee_plug_event_control[4]	R/W	0
1	DFT1	7	**Router/Switch** Reflects Router/Switch configuration from FLASH: 0: Switch. 1: Router.	RO	1
1	DFT1	11:8	**CIO Plug State** Reflects current ports [UN]PLUG state: 0: Plugged. 1: Unplugged.	RO	0xF
1	DFT1	12	**CIO Plug Event Pending** Reflects the state of the Plug Events (from CP perspective) 0: there are events that were not ACK'ed by CM 1: idle (no un-ACK'ed events)	RO	0x1
1	DFT1	15:13	**Max Iterations** Sets the number of iterations performed by the CIO Switch Scheduler.	R/W	2
1	DFT1	31:16	**CRC Error Count** Statistical counter of CRC errors on Control Packets; cleared on CIO reset	R/Clr	0
2	RSVD	31:0	Reserved	RO	0
3	PORT_ERR	0	**CIO1 Link Error** CIO Port#1 reports Link Error; cleared by setting to 1 or thru native CIO Error Ack mechanism.	R/WC	0
3	PORT_ERR	1	**CIO1 HEC Error** CIO Port#1 reports HEC Error; cleared by setting to 1 or thru native CIO Error Ack mechanism.	R/WC	0
3	PORT_ERR	2	**CIO1 FC Error** CIO Port#1 reports FC Error; cleared by setting to 1 or thru native CIO Error Ack mechanism.	R/WC	0
3	PORT_ERR	3	Reserved	RO	0
3	PORT_ERR	4	**CIO2 Link Error** CIO Port#1 reports Link Error; cleared by setting to 1 or thru native CIO Error Ack mechanism.	R/WC	0
3	PORT_ERR	5	**CIO2 HEC Error** CIO Port#1 reports HEC Error; cleared by setting to 1 or thru native CIO Error Ack mechanism.	R/WC	0

Table 23. DFT Vendor-Specific Capability Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
3	PORT_ERR	6	**CIO2 FC Error** CIO Port#1 reports FC Error; cleared by setting to 1 or thru native CIO Error Ack mechanism.	R/WC	0
3	PORT_ERR	7	Reserved	RO	0
3	PORT_ERR	8	**CIO3 Link Error** CIO Port#1 reports Link Error; cleared by setting to 1 or thru native CIO Error Ack mechanism.	R/WC	0
3	PORT_ERR	9	**CIO3 HEC Error** CIO Port#1 reports HEC Error; cleared by setting to 1 or thru native CIO Error Ack mechanism.	R/WC	0
3	PORT_ERR	10	**CIO3 FC Error** CIO Port#1 reports FC Error; cleared by setting to 1 or thru native CIO Error Ack mechanism.	R/WC	0
3	PORT_ERR	11	Reserved	RO	0
3	PORT_ERR	12	**CIO4 Link Error** CIO Port#1 reports Link Error; cleared by setting to 1 or thru native CIO Error Ack mechanism.	R/WC	0
3	PORT_ERR	13	**CIO4 HEC Error** CIO Port#1 reports HEC Error; cleared by setting to 1 or thru native CIO Error Ack mechanism.	R/WC	0
3	PORT_ERR	14	**CIO4 FC Error** CIO Port#1 reports FC Error; cleared by setting to 1 or thru native CIO Error Ack mechanism.	R/WC	0
3	PORT_ERR	15	Reserved	RO	0
3	PORT_ERR	31:16	**CIO Errors Enable** Enable bit per error above - when cleared, CP will not send respective error to CM, but it will be reflected in the status bits above.	R/W	0xFFFF
4	EEC	0	**EE_SK** Clock input to the FLASH. When BitBang is 1, the EE_SK output signal is mapped to this bit and provides the serial clock input to the FLASH. Software clocks the FLASH via toggling this bit with successive writes.	R/W	0
4	EEC	1	**EE_CS** Chip select input to the FLASH. When BitBang is 1, EE_CS output signal is mapped to the FLASH device's chip select. S/W enables the FLASH by writing '1' to this bit.	R/W	0
4	EEC	2	**EE_DI** Data input to the FLASH. When BitBang is 1, the EE_DI output signal is mapped directly to this bit. Software provides data input to the FLASH via writes to this bit.	R/W	0

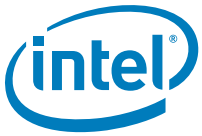


Table 23. DFT Vendor-Specific Capability Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
4	EEC	3	**EE_DO** Data output bit from the FLASH. The EE_DO input signal is mapped directly to this bit in the register and contains FLASH data output. It is read-only from the software perspective – writes to this bit have no effect.	RO	NA
4	EEC	4	**BitBang** Enable Bit Banging by SW. Software must write a 1 to this bit to get direct FLASH access. When the software completes the access it must write a 0.	R/W	0
4	EEC	5	**No FLASH** If set, there is no valid FLASH image or the FLASH chip is missing.	R/W	0
4	EEC	6	reserved	RO	0
4	EEC	7	**FLASH Done** FLASH read done status bit.	RO	0
4	EEC	8	**EE DMA En** Reflects ee_dma_en FLASH bit value.	RO	Expected to be 1 in HR image
4	EEC	9	**CM OVERRIDE EN** enables CM_OVERRIDE request processing in CP, in secure_en=0. if 0, CM_OVERRIDE will be silently ignored	R/W	0
4	EEC	16:10	**EE cp control** Loaded from FLASH (ee_cp_control[7:1]).	RO	0x0
4	EEC	17	**EEP done off** FLASH read done status bit for _off domain.	RO	0
4	EEC	29:18	Reserved	RO	0
4	EEC	30	**bitbang_ready** confirms that HW accesses to NVM are stalled (ee_read_arbiter). Should be polled for 1 after setting [31].	RO	0
4	EEC	31	**bitbang_request** request stall HW accesses to NVM (ee_read_arbiter). Should be set prior to NVM write/erase or bitbanging; cleared when done.	R/W	0
5	DFT_MIRROR	3:0	**MRR1** Chooses which Egress port data is mirrored to Port#1. Reset value of 1 chooses itself, which is regular functionality.	R/W	1
5	DFT_MIRROR	7:4	**MRR2** Same as above, for Port#2.	R/W	2
5	DFT_MIRROR	11:8	**MRR3** Same as above, for Port#3.	R/W	3
5	DFT_MIRROR	15:12	**MRR4** Same as above, for Port#4.	R/W	4
5	DFT_MIRROR	19:16	**MRR5** Same as above, for Port#5.	R/W	5

Table 23. DFT Vendor-Specific Capability Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
5	DFT_MIRROR	23:20	**MRR6** Same as above, for Port#6.	R/W	6
5	DFT_MIRROR	25:24	**REP1** Port#1 Replicates CIO Port# REP1 data.	R/W	0
5	DFT_MIRROR	27:26	**REP2** Port#2 Replicates CIO Port# REP2 data.	R/W	1
5	DFT_MIRROR	29:28	**REP3** Port#3 Replicates CIO Port# REP3 data.	R/W	2
5	DFT_MIRROR	31:30	**REP4** Port#4 Replicates CIO Port# REP4 data.	R/W	3
6	DFT_SNOOP	0	**SNOOP1** When set, enables "snooping" (passing through) of all packet types by the CIO Port#1 to CIO Switch. Used for snooping TMU and FC traffic.	R/W	0
6	DFT_SNOOP	1	**SNOOP2** Same as above, for Port#2.	R/W	0
6	DFT_SNOOP	2	**SNOOP3** Same as above, for Port#3.	R/W	0
6	DFT_SNOOP	3	**SNOOP4** Same as above, for Port#4.	R/W	0
6	DFT_SNOOP	4	Reserved	R/W	0
6	DFT_SNOOP	5	Reserved	R/W	0
6	DFT_SNOOP	6	Reserved	R/W	0
6	DFT_SNOOP	7	Reserved	R/W	0
6	DFT_SNOOP	8	**LPBK1** When set, enables external loopback (master loopback) on CIO Port#1.	R/W	0
6	DFT_SNOOP	9	**LPBK2** Same as above, for Port#2.	R/W	0
6	DFT_SNOOP	10	**LPBK3** Same as above, for Port#3.	R/W	0
6	DFT_SNOOP	11	**LPBK4** Same as above, for Port#4.	R/W	0
6	DFT_SNOOP	12	**Adapter Loopback 1** Loopback of Tx->Rx on CIO null adapter level Port#1.	R/W	0
6	DFT_SNOOP	13	**Adapter Loopback 2** Same as above, for Port#2.	R/W	0
6	DFT_SNOOP	14	**Adapter Loopback 3** Same as above, for Port#3.	R/W	0
6	DFT_SNOOP	15	**Adapter Loopback 4** Same as above, for Port#4.	R/W	0
6	DFT_SNOOP	16	**TL Loopback 1** Loopback of Tx->Rx on CIO null TL level Port#1.	R/W	0
6	DFT_SNOOP	17	**TL Loopback 2** Same as above, for Port#2.	R/W	0

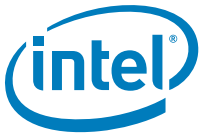


Table 23. DFT Vendor-Specific Capability Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
6	DFT_SNOOP	18	**TL Loopback 3** Same as above, for Port#3.	R/W	0
6	DFT_SNOOP	19	**TL Loopback 4** Same as above, for Port#4.	R/W	0
6	DFT_SNOOP	29:20	Reserved	RO	0
6	DFT_SNOOP	30	**Master Lock** master_lock bit - when set, CP target accesses will assert master_lock target interface signal	RW	0
6	DFT_SNOOP	31	**HDP In/Out bypass mode** HDP IN -> OUT HDMI bypass enable	R/W	0
7	DFT7	0	cio_data_rst_n_null_1	R/W	1
7	DFT7	1	cio_data_rst_n_null_2	R/W	1
7	DFT7	2	cio_data_rst_n_null_3	R/W	1
7	DFT7	3	cio_data_rst_n_null_4	R/W	1
7	DFT7	15:4	Reserved	RO	0
7	DFT7	31:16	**Probe Mode Data** Probe Mode data output	RO	0
8	UCTL	0	**uCTL soft reset** When written to 1, causes soft reset to Control Port uCTL.	R/W SC	0
8	UCTL	1	**Lock patch ram** Locks CP Patch RAM for writes after initial FLASH load. Can be cleared by SW and following FLASH reload will load the patch again, after which that bit will lock again. Applies to TRAP registers as well.	R/W	0
8	UCTL	2	**SW REQ** SW Semaphore request. SW can write to 1 and poll sem_state==0. Clear to release	R/W	0
8	UCTL	3	**Semaphore State** 0: SW, 1: CP ownership	RO	0
8	UCTL	14:4	**Goto Address** when any_trap==1, indicates next PC addr, otherwise equal to current PC	RO	
8	UCTL	15	**CP_REQ** CP Semaphore request. CP can write to 1 and poll sem_state==1.	RO	0
8	UCTL	26:16	**IMem Addr** Program Counter of uCTL	RO	
8	UCTL	27	**Any_trap** Internal indication of a trap on current uCTL PC	RO	0
8	UCTL	31:28	**Dbg Func.** Current uCTL execution function (encoded).	RO	
9	TRAP	0	**Break Continue** When set to 1, pulses uCTL C17 bit.	R/W SC	0
9	TRAP	15:1	**Trap Valid Lo** Trap valid indications per uCTL ROM patch traps (Lo)	R/W	0

Table 23. DFT Vendor-Specific Capability Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
9	TRAP	30:16	**Trap Valid Hi** Trap valid indications per uCTL ROM patch traps (Hi)	R/W	0
9	TRAP	31	Reserved	RO	0
10	MAILBOX	15:0	**SFR4 Low** uCTL's SFR4 lo mapped to DEV CFG space, reset on CIO reset.	R/W	0
10	MAILBOX	31:16	**SFR4 High** uCTL's SFR4 hi mapped to DEV CFG space, reset on Power Good reset.	R/W	0
11	PM_SEL_TRIG	13:0	Reserved	R/W	0
11	PM_SEL_TRIG	14	**PM Interrupt on Fall** Interrupt uCTL on negedge of visa_lanes_out bit.	R/W	0
11	PM_SEL_TRIG	15	**PM Interrupt on Rise** Interrupt uCTL on posedge of visa_lanes_out bit.	R/W	0
11	PM_SEL_TRIG	16	Reserved	R/W	0
11	PM_SEL_TRIG	20:17	**PM Data Bit Select** Select 1 out of 16 visa_lanes_out bits to act as trigger.	R/W	0
11	PM_SEL_TRIG	30:21	Reserved	RO	0
11	PM_SEL_TRIG	31	**PM Trig Occurred** latch trigger to uCTL (interrupt). To clear, write 0.	R/W	0
12	SERIAL_NUMBER	31:0	**Serial Number** Read/Write register, which can be loaded through EE->Tar with a unique per chip value. After EEPROM is loaded gets the value of **ee_drom_start_addr.**	R/W	0
13	IORING_GLUE_REG	26:0	**DFT settings** Resides in the LC power-domain.	R/W	0x57E
		31:27		RO	
14	DFT14	31:0	**Port Plug State** CP INTERNAL indication, bit per port: 1-unplugged, 0-plugged	RO	NA
15	DFT15	31:0	**Port Plug Event Pending** CP INTERNAL indication, bit per port: 1-pending, 0-idle	RO	NA
16	DFT16	31:0	**Last Port Plug Event** CP INTERNAL indication, last plug event packet data DW	RO	NA
17	DFT17	31:0	**HDP ports plug state** CP INTERNAL indication, HDP ports status debug register	RO	NA

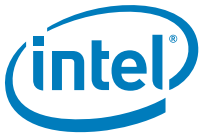


Table 23. DFT Vendor-Specific Capability Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
18	DFT18	31:0	**CIO Multi-Lane link control** [0] - cio_sw_extended_mode, loaded from FLASH; rest reserved. [15:0] on power-good reset, [31:16] on cio-reset	R/W	0
19	DFT19	7:0	Reserved	R/W	0
19	DFT19	15:8	**CIO SW Long Packet Thresh**	R/W	0x5C
19	DFT19	19:16	reserved	R/W	0
19	DFT19	23:20	**cio_tx_bp_free_space_thresh** Threshold used by TL to rise back pressure towards CIO switch	R/W	4
19	DFT19	24:24	**cio_sw_mid_length_pkts_performance_impr_dis** Chicken bit - Set this bit to disable CIO Switch performance improvement for medium length packets	R/W	0
19	DFT19	28:25	**cio_tx_bp_free_space_thresh_for_slow_adapters** Threshold used by TL to rise back pressure towards CIO switch. Used by DMA/CP as they can be slow response adapters.	R/W	0
19	DFT19	31:29	reserved	R/W	0
20	Sx Control	31	go_to_sx_request	R/W	0
20	Sx Control	30	cp_clc_ok_to_go_to_sx override	R/W	0
20	Sx Control	29	cp_clc_ok_to_go_to_sx	RO	0
20	Sx Control	28	clc_power_down_req	RO	0
20	Sx Control	27	cp_power_down_ack	RO	0
20	Sx Control	26	cp_power_down_ack override	R/W	0
20	Sx Control	25:17	Reserved	R/W	0
20	Sx Control	16	always wake CIO domain		0
20	Sx Control	15:8	wake_enables (portB)		0
20	Sx Control	7:0	wake_enables (portA)		0
21	IO CTRL REG	31:30	i_pb_config1__cio_2_lseo bit[30] - sust enable bit[31] - value	R/W	0
21	IO CTRL REG	29:28	i_pb_config2__cio_2_lsoe bit[28] - sust enable bit[29] - value	R/W	0
21	IO CTRL REG	27:26	i_pa_config1__cio_0_lseo bit[26] - sust enable bit[27] - value	R/W	0
21	IO CTRL REG	25:24	i_pa_config2__cio_0_lsoe bit[24] - sust enable bit[25] - value	R/W	0

Table 23. DFT Vendor-Specific Capability Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
21	IO CTRL REG	23:22	src_pb_hdp_from_pin_hpd bit[22] - sust enable bit[23] - value	R/W	0
21	IO CTRL REG	21:20	src_pa_hdp_from_pin_hpd bit[20] - sust enable bit[21] - value	R/W	0
21	IO CTRL REG	19:18	poc_i_gpio_pins_to_core_bus9 bit[18] - sust enable bit[19] - value	R/W	0
21	IO CTRL REG	17:16	poc_i_gpio_pins_to_core_bus3 bit[16] - sust enable bit[17] - value	R/W	0
21	IO CTRL REG	15:0	pm_data control	R/W	0
22	VISA DFT 1	31:0		R/W	0
23	VISA DFT 2	31:0		R/W	0
24	VISA DFT 3	31:0		R/W 0, 2 SC	0
25	VISA DFT 4	31:0		RO	0
26	VISA DFT 5	31:0		RO	0
27	PCIe Wr DATA	31:0	PCIe Write Data	R/W	0
28	PCIe Command	5:0	**Register Number** PCIe Switch Register offset	R/W	0
28	PCIe Command	9:6	**Extended Register Number** Extended PCIe Switch Register offset	R/W	0
28	PCIe Command	18:10	**Choose Bridge** EMEP_cnfg = Choose_bridge[8] Dn6_cnfg = Choose_bridge[7] . . . Dn0_cnfg = Choose_bridge[1] Up0_cnfg = Choose_bridge[0]	R/W	0
28	PCIe Command	20:19	reserved		
28	PCIe Command	21	**Read_Write** 0: Read command 1: Write command	R/W	0
28	PCIe Command	24:22	**Command** 010: Access to PCIe Switch registers	R/W	0
28	PCIe Command	29:25	reserved		
28	PCIe Command	30	**Request_Ack** Set to 1 to execute. Clears on completion	R/W SC	0
28	PCIe Command	31	**Timeout** This bit is set to 1 if last access completed with timeout	RW	0
29	PCIe Rd DATA	31:0	**PCIe Read Data** Valid when Resquest_Ack bit is cleared and Timeout bit is zero	RW	0

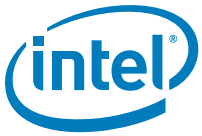


Table 23. DFT Vendor-Specific Capability Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
30	DFT30	31:0	**LSM_Stat** Resets on power good. Used by CP for LSM reset statistic. Each byte represents how many link resets done by the LSM feature for each port (4ports-4bytes)	R/W	0
31	DFT31	7:0	Number of permitted consecutive errors (Each 100ms), when link state is CLD->CL0. Resets on power good. Loaded from EE2TAR. Recommended value – 19	R/W	0
31	DFT31	15:8	Number of consecutive errors (Each 100ms), when link state is CL0. Resets on power good. Loaded from EE2TAR. Recommended value - 2	R/W	0
31	DFT31	16	**LSM init enable** Resets on power good. Loaded from EE2TAR. Recommended value - 1	R/W	0
31	DFT31	17	**LSM runtime enable** To switch to single step DFT mode, set this bit to 0. Resets on power good. Loaded from EE2TAR. Recommended value - 1	R/W	0
31	DFT31	18	**Trigger one single step** Resets on power good.	R/W	0
31	DFT31	19	Use DFT HEC counters instead of real (0x6->0x0 port_cs)**.** Resets on power good.	R/W	0
31	DFT31	20	Do not reset upstream port Resets on power good.	R/W	0
31	DFT31	21	**use_plug_state_history, not in use, do not set this bit**	R/W	0
31	DFT31	22	**cp_dma_en_xor**	R/W	0
31	DFT31	31:23	reserved	R/W	0
32	DFT32	31:0		R/W	0xFFFFFFFF
40	CAR_DFT1_DYNAMIC	31:0	Writing 1 to bits in this register causes temporal reset events in the device, at the moment of write event Reading value of *_dynamic_* has no meaning, but change from prev read indicates odd amount of resets at respective bit (allows some sanity check that prev write succeeded)	R/W S	0
41	CAR_DFT1_STATIC_SET	31:0	Writing 1 to bits in this register causes level reset assertion in the device; Reading value of *_static_* represents current reset request state	R/W S	0
42	CAR_DFT1_STATIC_CLR	31:0	Writing 1 to bits in this register causes level reset DE-assertion in the device; Reading value of *_static_* represents current reset request state	R/W S	0

Table 23. DFT Vendor-Specific Capability Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
43	CAR_DFT2_DYNAMIC	31:0	Writing 1 to bits in this register causes temporal reset events in the device, at the moment of write event Reading value of *_dynamic_* has no meaning, but change from prev read indicates odd amount of resets at respective bit (allows some sanity check that prev write succeeded)	R/W S	0
44	CAR_DFT2_STATIC_SET	31:0	Writing 1 to bits in this register causes level reset assertion in the device; Reading value of *_static_* represents current reset request state	R/W S	0
45	CAR_DFT2_STATIC_CLR	31:0	Writing 1 to bits in this register causes level reset DE-assertion in the device; Reading value of *_static_* represents current reset request state	R/W S	0
46	CAR_DFT3_DYNAMIC	31:0	Writing 1 to bits in this register causes temporal reset events in the device, at the moment of write event Reading value of *_dynamic_* has no meaning, but change from prev read indicates odd amount of resets at respective bit (allows some sanity check that prev write succeeded)	R/W S	0
47	CAR_DFT3_STATIC_SET	31:0	Writing 1 to bits in this register causes level reset assertion in the device; Reading value of *_static_* represents current reset request state	R/W S	0
48	CAR_DFT3_STATIC_CLR	31:0	Writing 1 to bits in this register causes level reset DE-assertion in the device; Reading value of *_static_* represents current reset request state	R/W S	0
49	CAR_DFT4_DYNAMIC	31:0	Writing 1 to bits in this register causes temporal reset events in the device, at the moment of write event Reading value of *_dynamic_* has no meaning, but change from prev read indicates odd amount of resets at respective bit (allows some sanity check that prev write succeeded)	R/W S	0
50	CAR_DFT4_STATIC_SET	31:0	Writing 1 to bits in this register causes level reset assertion in the device; Reading value of *_static_* represents current reset request state	R/W S	0
51	CAR_DFT4_STATIC_CLR	31:0	Writing 1 to bits in this register causes level reset DE-assertion in the device; Reading value of *_static_* represents current reset request state	R/W S	0
52	CP_DISABLE_PLUG_EVENT	12:0	Disable plug event, bit per port. Bits [4:1] can be set by ee_cp_plug_event_control[1] or DFT1[3], bits[10:8] can be set by ee_cp_plug_event_control[4:2] or DFT1[6:4]	R/W S	0

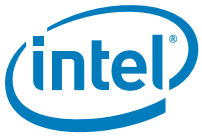


Table 24. CAR_DFT1_DYNAMIC/STATIC_SET/STATIC_CLR

Register Name	Bit(s)	Field Name and Description	Type	Default Value
CAR_DFT1_*	0	pa_car_cio_port_rst_n	R/W	0
CAR_DFT1_*	1	pa_car_cio_rx_rst_n_c0	R/W	0
CAR_DFT1_*	2	pa_car_cio_rx_rst_n_c1	R/W	0
CAR_DFT1_*	3	pa_car_usb_phy_rst_n	R/W	0
CAR_DFT1_*	4	pa_car_usb_rx_rst_n_u0	R/W	0
CAR_DFT1_*	5	pa_car_usb_rx_rst_n_u1	R/W	0
CAR_DFT1_*	6	pa_car_cio_usb_xtal_ref_rst_n	R/W	0
CAR_DFT1_*	7	pa_cio_pg_car_cio_port	R/W	0
CAR_DFT1_*	8	cio_rstn_src	R/W	0
CAR_DFT1_*	31:9	Reserved(*)	R/W	0

(*) = {dynamic, static_set, static_clr}

Table 25. CAR_DFT2_DYNAMIC/STATIC_SET/STATIC_CLR

Register Name	Bit(s)	Field Name and Description	Type	Default Value
CAR_DFT2_*	0	pb_car_cio_port_rst_n	R/W	0
CAR_DFT2_*	1	pb_car_cio_rx_rst_n_c0	R/W	0
CAR_DFT2_*	2	pb_car_cio_rx_rst_n_c1	R/W	0
CAR_DFT2_*	3	pb_car_usb_phy_rst_n	R/W	0
CAR_DFT2_*	4	pb_car_usb_rx_rst_n_u0	R/W	0
CAR_DFT2_*	5	pb_car_usb_rx_rst_n_u1	R/W	0
CAR_DFT2_*	6	pb_car_cio_usb_xtal_ref_rst_n	R/W	0
CAR_DFT2_*	7	pb_cio_pg_car_cio_port	R/W	0
CAR_DFT2_*	19:8	Reserved(*)	R/W	0
CAR_DFT2_*	20	car_tmu_dp_reset_n	R/W	0
CAR_DFT2_*	21	cio_pg	R/W	0
CAR_DFT2_*	22	cio_pg_car_cio_0	R/W	0
CAR_DFT2_*	23	cio_pg_car_cio_1	R/W	0
CAR_DFT2_*	24	cio_pg_car_cio_sw	R/W	0

Table 25. CAR_DFT2_DYNAMIC/STATIC_SET/STATIC_CLR

Register Name	Bit(s)	Field Name and Description	Type	Default Value
CAR_DFT2_*	25	dp_pg_hdp_csr	R/W	0
CAR_DFT2_*	26	car_tmu_fast_reset_n	R/W	0
CAR_DFT2_*	27	car_tmu_reset_n	R/W	0
CAR_DFT2_*	28	car_cio_rst_n	R/W	0
CAR_DFT2_*	29	car_cio_sw_rst_n	R/W	0
CAR_DFT2_*	30	pa_car_tmu_phy_dig_ctrl_rst_n	R/W	0
CAR_DFT2_*	31	pb_car_tmu_phy_dig_ctrl_rst_n	R/W	0

(*) = {dynamic, static_set, static_clr}

Table 26. CAR_DFT3_DYNAMIC/STATIC_SET/STATIC_CLR

Register Name	Bit(s)	Field Name and Description	Type	Default Value
CAR_DFT3_*	0	car_clc_pa_patch_load_rst_n	R/W	0
CAR_DFT3_*	1	car_clc_pb_patch_load_rst_n	R/W	0
CAR_DFT3_*	2	ana_lc_csr_rst_n	R/W	0
CAR_DFT3_*	3	svr_cal_csr_rst_n	R/W	0
CAR_DFT3_*	4	car_comm_xtal_rst_n	R/W	0
CAR_DFT3_*	5	car_power_good_e	R/W	0
CAR_DFT3_*	6	cio_pg_car_comm_pcie_xtal	R/W	0
CAR_DFT3_*	7	pcie_pg_car_comm_pcie_xtal	R/W	0
CAR_DFT3_*	8	xhc_pg_car_comm_pcie_xtal	R/W	0
CAR_DFT3_*	9	cio_pg_car_eep	R/W	0
CAR_DFT3_*	10	car_comm_perst_and_pwgd	R/W	0
CAR_DFT3_*	11	usb_pg_car_comm_lc_osc_25	R/W	0
CAR_DFT3_*	31:12	Reserved(*)	R/W	0

(*) = {dynamic, static_set, static_clr}

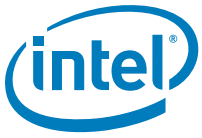


Table 27. CAR_DFT4_DYNAMIC/STATIC_SET/STATIC_CLR

Register Name	Bit(s)	Field Name and Description	Type	Default Value
CAR_DFT4_*	0	car_pcie_rst_n_sw	R/W	0
CAR_DFT4_*	1	car_pcie_rst_n_ds0	R/W	0
CAR_DFT4_*	2	car_pcie_rst_n_ds1	R/W	0
CAR_DFT4_*	3	car_pcie_rst_n_ds2	R/W	0
CAR_DFT4_*	4	car_pcie_rst_n_ds3	R/W	0
CAR_DFT4_*	5	car_pcie_rst_n_ds4	R/W	0
CAR_DFT4_*	6	ux_side_rst_b	R/W	0
CAR_DFT4_*	7	ux_prim_rst_b	R/W	0
CAR_DFT4_*	8	car_pcie_rst_n_ad_p0	R/W	0
CAR_DFT4_*	9	xhc_car_pcie_pclk_xhc_rst_n	R/W	0
CAR_DFT4_*	10	car_pcie_tl_dma_rst_n	R/W	0
CAR_DFT4_*	11	car_pcie_pclk_dma_rst_n	R/W	0
CAR_DFT4_*	12	car_pcie_rst_n_us	R/W	0
CAR_DFT4_*	13	car_pcie_rst_n_ad_p1	R/W	0
CAR_DFT4_*	14	car_pcie_dma_rst_n	R/W	0
CAR_DFT4_*	15	car_pcie_perst_dma_rst_n	R/W	0
CAR_DFT4_*	16	pcie_rst_3_n	R/W	0
CAR_DFT4_*	17	pcie_rst_2_n	R/W	0
CAR_DFT4_*	18	pcie_rst_1_n	R/W	0
CAR_DFT4_*	19	pcie_rst_0_n	R/W	0
CAR_DFT4_*	20	rstn_sw	R/W	0
CAR_DFT4_*	21	cio_pg_car_pcie_sw	R/W	0
CAR_DFT4_*	22	cio_pg_car_pcie_tl_dma	R/W	0
CAR_DFT4_*	23	cio_pg_car_pcie_user_dma	R/W	0
CAR_DFT4_*	24	pcie_pg_car_pcie_phy_500	R/W	0
CAR_DFT4_*	25	pcie_pg_car_pcie_sw	R/W	0
CAR_DFT4_*	26	xhc_pg_car_pcie_user_xhc	R/W	0
CAR_DFT4_*	31:27	Reserved(*)	R/W	0

(*) = {dynamic, static_set, static_clr}

4.3.1.4.3 Analog Vendor Specific Registers

The attributes of the Analog vendor-specific capability registers are described in Table 28. This register resides in the RDV power-domain.

Note: The register offset is relative to DEV_VSEC_2_BASE in Table 19.

Table 28. Analog Vendor-Specific Capability Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	VSEC_ANA_CS_0	7:0	Next Capability Pointer This field defines the doubleword index of the next capability register set in the device configuration space. It is set to 00h if the Vendor-Specific capability register set is the final register set in the linked list of capability register sets in the device configuration space.	RO	See Pointer in Table 19
0	VSEC_ANA_CS_0	15:8	Capability ID This field must contain the value 05h indicating this is the start of the Vendor-Specific capability register set.	RO	5
0	VSEC_ANA_CS_0	23:16	VSEC ID This field is a vendor-defined ID number that indicates the nature and format of the VSEC structure.	RO	2
0	VSEC_ANA_CS_0	31:24	VSEC Length This field indicates the number of double words in the entire VSEC structure including the header and the Vendor-Specific registers.	RO	8

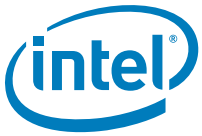


Table 28. Analog Vendor-Specific Capability Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
1	PCIE_PHY_IP_AHB_COMMAND	31:0	Used to access PCIe PHY registers. Bit mapping is the following: [7:0] - ahb_wdata_i [15:8] - ahb_wmask_i (active low) [28:16] - ahb_addr_i [29] - ahb_write_i [30] - Reserved [31] - req1_done0 SW should set the fields and req1_done0, then poll req1_done0==0 for completion. ahb_addr_i has the following encoding: The upper 4 bits of the AHB address is used for device selection: 0x0 - CMU0 0x1 - Lane0 0x2 - Lane1 0x3 - Lane2 0x4 - Lane4 0x5 - Common Lane Block 0x6 - CMU1 0x7 - Broadcast to all lanes 0x8 - Broadcast to Lane0 and Lane1 0x9 - Broadcase to Lane2 and Lane3	R/W	
2	PCIE_PHY_IP_AHB_DATA	7:0	PCIe PHY register data (read/write)	R/W	
2	PCIE_PHY_IP_AHB_DATA	31:8	PCIe PHY DFT bits: ln0_rxelecidle_o ln1_rxelecidle_o ln2_rxelecidle_o ln3_rxelecidle_o pcie_phy_rst_n_l0 pcie_phy_rst_n_l1 pcie_phy_rst_n_l2 pcie_phy_rst_n_l3 ee_pcie_pll_powerdown cmu0_ok_o cmu1_ok_o pcie_phy_clk_stable tbus_data_o (12bit)	RO	
3	SVR_CORE_ADD	15:0	Register address for SVR	R/W	
3	SVR_CORE_ADD	31:16	reserved		
4	SVR_CORE_DATA	31:0	Register data for SVR	R/W	
5	PCIE_PHY_DFT0	31:0	DFT bits	R/W	
6	PCIE_PHY_DFT1	31:0	DFT bits	R/W	
7	PCIE_PHY_DFT2	31:0	DFT bits	RO	

4.3.1.4.4 TMU Vendor Specific Registers

The attributes of the TMU vendor-specific capability registers are described in Table 29.

Note: The register offset is relative to DEV_VSEC_3_BASE in Table 19.

Table 29. TMU Vendor-Specific Capability Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	VSEC_TMU_CS_0	7:0	Next Capability Pointer This field defines the doubleword index of the next capability register set in the device configuration space. It is set to 00h if the Vendor-Specific capability register set is the final register set in the linked list of capability register sets in the device configuration space.	RO	See Pointer in Table 19
0	VSEC_TMU_CS_0	15:8	Capability ID This field must contain the value 05h indicating this is the start of the Vendor-Specific capability register set.	RO	5
0	VSEC_TMU_CS_0	23:16	VSEC ID This field is a vendor-defined ID number that indicates the nature and format of the VSEC structure.	RO	3
0	VSEC_TMU_CS_0	31:24	VSEC Length This field indicates the number of double words in the entire VSEC structure including the header and the Vendor-Specific registers.	RO	50
1	VSEC_TMU_CS_1	15:0	Serial Calc Interval Interval of sending serial computation. Units in usec.	R/W	16
1	VSEC_TMU_CS_1	31:16	Serial Event Interval Interval of sending serial packet after serial comp request. Units in nsec.	R/W	750
2	VSEC_TMU_CS_2	14:0	PLL Param PLL frequency can be changed by SW. Writing to this register will cause PLL frequency to change. Param Default=10,000 (1GHz). Param Min=0 (99.0464Mhz), Param Max=20,000(1.009536Ghz). 1 step is 0.9536ppm of the main frequency	R/W	0
2	VSEC_TMU_CS_2	15	PLL Direction PLL SW change can be relative to current value. This bit states the direction: 1 - step up, 0 - step down. Relevant only if bit16 of this register is 1.	R/W	0
2	VSEC_TMU_CS_2	16	PLL Change Relative/Absolute PLL SW change relative or absolute: 0 - PLL Param taken as is, 1 - PLL Param is taken relative to previous value depending on PLL change direction.	R/W	0
2	VSEC_TMU_CS_2	31:17	Reserved	RO	0

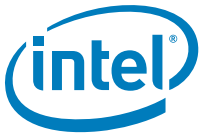


Table 29. TMU Vendor-Specific Capability Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
3	VSEC_TMU_CS_3	31:0	Reserved	RO	0
4	VSEC_TMU_CS_4	31:0	Post Local Time 31:0 This register specifies the value that is used to update the least significant 32 bits of the nanoseconds field of the Local Time register when the PostTime matches the CIO Time. On reset, this register must default to 0.	R/W	0
5	VSEC_TMU_CS_5	31:0	Post Local Time 63:32 This register specifies the value that is used to update the most significant 32 bits of the nanoseconds field of the Local Time register when the PostTime matches the CIO Time. On reset, this register must default to 0.	R/W	0
6	VSEC_TMU_CS_6	31:0	Post Time 31:0 This register specifies the least significant 32 bits of the nanoseconds field of the CIO Time register at which the software updates to the LocalTime register must be applied. On reset, this register must default to 0.	R/W	0
7	VSEC_TMU_CS_7	31:0	Post Time 63:32 This register specifies the most significant 32 bits of the nanoseconds field of the CIO Time register at which the software updates to the LocalTime register must be applied. On reset, this register must default to 0.	R/W	0
8	VSEC_TMU_CS_8	15:0	Reserved	R0	0
8	VSEC_TMU_CS_8	23:16	Disruption Threshold Disruption threshold value.	R/W	10
8	VSEC_TMU_CS_8	31:24	Lock Threshold Lock threshold value (obsolete).	R/W	10
9	VSEC_TMU_CS_9	3:0	Reserved	RO	0
9	VSEC_TMU_CS_9	5:4	Lock State Current state of TIME Lock.	RO	0
9	VSEC_TMU_CS_9	6	Disruption State Current state of TIME Disruption.	RO	1
9	VSEC_TMU_CS_9	7	Disruption Value Disruption polarity for DP events generation.	R/W	0
9	VSEC_TMU_CS_9	31:8	Reserved	RO	0
10	VSEC_TMU_CS_10	2:0	TMU Rep 1 Replicate from port # for snoop mode.	WO	0
10	VSEC_TMU_CS_10	5:3	TMU Rep 2 Replicate from port # for snoop mode.	WO	0
10	VSEC_TMU_CS_10	8:6	TMU Rep 3 Replicate from port # for snoop mode.	WO	0
10	VSEC_TMU_CS_10	11:9	TMU Rep 4 Replicate from port # for snoop mode.	WO	0

Table 29. TMU Vendor-Specific Capability Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
10	VSEC_TMU_CS_10	31:12	Reserved	RO	0
11-18	VSEC_TMU_CS_11 - VSEC_TMU_CS_18	31:0	General purpose rd/wr registers	R/W	0
19	VSEC_TMU_CS_19	7:0	Serial Interface Bit Error Counter Counts the number of occurrences when violation of serial bit interface occurred. Sticky counter stays on 255 until read. When read, clears itself.	R/Clr	0
19	VSEC_TMU_CS_19	15:8	Serial Interface Bad Packet Counter Counts the number packets with bad CRC. Sticky counter stays on 255 until read. When read, clears itself.	R/Clr	0
19	VSEC_TMU_CS_19	23:16	Serial In Disruption counter Count the number of received serial in packets with disruption bit set.	RO	0
19	VSEC_TMU_CS_19	31:24	Reserved	RO	0
20	VSEC_TMU_CS_20	31:0	Reserved	RO	0
21	VSEC_TMU_CS_21	0	DP LS Window Interval DP clock restoration window - choose between 2/4 msec.	R/W	1
21	VSEC_TMU_CS_21	15:1	DP Wait Before Calc Interval DP calc delay after 2/4msec window. Units in usec.	R/W	500
21	VSEC_TMU_CS_21	23:16	DP PLL Change Interval PLL change interval for DP_OUT. 0 – 1 usec 1 – 2 usec 2 – 4 usec 3 – 8 usec	R/W	0
21	VSEC_TMU_CS_21	27:24	DP Change Source Use adjusted or local counter: 0 - use adjusted, 15 - use local.	R/W	0
21	VSEC_TMU_CS_21	29:28	Reserved	RO	0
21	VSEC_TMU_CS_21	30	Disable Symbol Shift Disable rx-time-to-wire fix from PHY.	R/W	1
21	VSEC_TMU_CS_21	31	Symbol Shift Polarity Change polarity of rx-time-to-wire from PHY.	R/W	1
22	VSEC_TMU_CS_22	31:0	uCTL Command Command to ALU. Bit 31 - imem_ready Bit 20 - go Bits 18:16 - operation: 7 / 6 / 5 / 4 / 3 / 2 / 1 / 0 – soft_reset / clear / wr_sfr / rd_sfr / wr_trap_valid / rd_trap_valid / wr_imem / rd_imem Bits 8:0 - addr	R/W	0
23	VSEC_TMU_CS_23	31:0	uCTL Data Data to ALU.	R/W	0

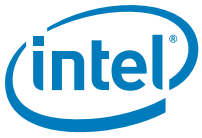


Table 29. TMU Vendor-Specific Capability Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
24	VSEC_TMU_CS_24	31:0	uCTL Read Data Data from ALU.	RO	0
25	VSEC_TMU_CS_25	5:0	Upstream Port States the upstream port for TMU master/slave relation. Valid when TMU Upstream Port Valid bit is set to 1.	R/W	0
25	VSEC_TMU_CS_25	7:6	Reserved	RO	0
25	VSEC_TMU_CS_25	8	Upstream Port Valid If set to 0 (default) TMU chooses master/slave by CIO Upstream configuration. If set to 1, TMU will use TMU Upstream Port parameter to choose master/slave.	R/W	0
25	VSEC_TMU_CS_25	31:9	Reserved	RO	0
26	VSEC_TMU_CS_26	7:0	Serial Time to Wire Time to Wire on serial interface.	R/W	14
26	VSEC_TMU_CS_26	15:8	Serial Time to Calc Time to from Send Serial command to first bit on the wire.	R/W	66
26	VSEC_TMU_CS_26	21:16	Serial Time to Fix Time adjustment for t_local_g parameter in CIO time calculation by ALU.	R/W	8
26	VSEC_TMU_CS_26	26:22	Disruption Force Bit [0] - when 1 - SW force disruption on Serial interface, and also stop 2msec event to DP, when 0 - enable the event. Bit[1] - when 1 SW stop IIR sampling in DP IN, when 0 – enable. Bit[2] - when 1 - SW stop IIR sampling in DP_OUT, when 0 – enable. Bit[3] - when 1 - SW stop calc event in DP_OUT, when 0 – enable. Bit[4] - when 1 SW stop PLL change event in DP_OUT, when 0 – enable.	R/W	0
26	VSEC_TMU_CS_26	31:27	Disruption Mask Bit [0] - when 0 - SW mask disruption blocking of 2msec event to DP, when 1 - disruption will block this event. Bit[1] - when 0 SW mask disruption blocking of IIR sampling in DP_IN, when 1 - disruption will block this event. Bit[2] - when 0 - SW mask disruption blocking of IIR sampling in DP_OUT, when 1 - disruption will block this event. Bit[3] - when 0 - SW mask disruption blocking of calc event in DP_OUT, when 1 - disruption will block this event. Bit[4] - when 0 SW mask disruption blocking of PLL change event in DP_OUT, when 1 - disruption will block this event.	R/W	31
27-34	VSEC_TMU_CS_27 - VSEC_TMU_CS_34	31:0	General purpose rd/wr registers	R/W	0

Table 29. TMU Vendor-Specific Capability Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
35	VSEC_TMU_CS_35	4:0	Serial First Half Max Null Max time in 2nsec units to detect first half of NULL bit.	R/W	12
35	VSEC_TMU_CS_35	9:5	Serial First Half Max One Max time in 2nsec units to detect first half of ONE bit.	R/W	20
35	VSEC_TMU_CS_35	14:10	Serial First Half Max Zero Max time in 2nsec units to detect first half of ZERO bit.	R/W	7
35	VSEC_TMU_CS_35	19:15	Serial First Half Min Null Min time in 2nsec units to detect first half of NULL bit.	R/W	8
35	VSEC_TMU_CS_35	24:20	Serial First Half Min One Min time in 2nsec units to detect first half of ONE bit.	R/W	13
35	VSEC_TMU_CS_35	29:25	Serial First Half Min Zero Min time in 2nsec units to detect first half of ZERO bit.	R/W	1
35	VSEC_TMU_CS_35	30	Serial Ignore No Lock When 0 - Serial in packet will be accepted regardless lock state field, when 1 - Only packet that don't have Lock state=1 will be accepted.	R/W	1
35	VSEC_TMU_CS_35	31	Serial Ignore Disruption When 0 - Serial in packet will be accepted regardless disruption field, when 1 - Only packet that don't have disruption=1 will be accepted.	R/W	0
36	VSEC_TMU_CS_36	4:0	Serial First Half Max Null Max time in 2nsec units to detect first half of NULL bit.	R/W	12
36	VSEC_TMU_CS_36	9:5	Serial Second Half Max One Max time in 2nsec units to detect second half of ONE bit.	R/W	8
36	VSEC_TMU_CS_36	14:10	Serial Second Half Max Zero Max time in 2nsec units to detect second half of ZERO bit.	R/W	20
36	VSEC_TMU_CS_36	19:15	Serial Second Half Min Null Min time in 2nsec units to detect second half of NULL bit.	R/W	8
36	VSEC_TMU_CS_36	24:20	Serial Second Half Min One Min time in 2nsec units to detect second half of ONE bit.	R/W	1
36	VSEC_TMU_CS_36	29:25	Serial Second Half Min Zero Min time in 2nsec units to detect second half of ZERO bit.	R/W	13
36	VSEC_TMU_CS_36	30	Reserved	RO	0
36	VSEC_TMU_CS_36	31	Serial Always Good 0 – Only accept serial with good CRC. 1 - Accept serial in packets regardless CRC error.	R/W	0

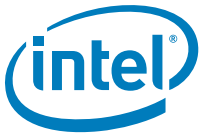


Table 29. TMU Vendor-Specific Capability Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
37	VSEC_TMU_CS_37	31:0	Timestamp of Serial packet Arrival 31:0 Time of last good serial packet arrival. When reading from this register a snapshot is taken of all the serial packet related parameters. Time format is as define in CIO spec for Local time.	RO	0
38	VSEC_TMU_CS_38	31:0	Timestamp of Serial packet Arrival 63:32 Snapshot of time of last good serial packet arrival. Bits [63:32]. Taken on the last read of register #37. Time format is as define in CIO spec for Local time.	RO	0
39	VSEC_TMU_CS_39	15:0	Timestamp of Serial packet Arrival 79:64 Snapshot of time of last good serial packet arrival. Bits [79:64]. Taken on the last read of register #37. Time format is as define in CIO spec for Local time.	RO	0
39	VSEC_TMU_CS_39	17:16	Serial Packet Lock State Snapshot of Lock state parameter extracted from last serial packet. Taken on the last read of register #37.	RO	0
39	VSEC_TMU_CS_39	18	Serial Packet Disruption State Snapshot of Disruption state parameter extracted from last serial packet. Taken on the last read of register #37.	RO	0
39	VSEC_TMU_CS_39	31:19	Reserved	RO	0
40	VSEC_TMU_CS_40	31:0	Serial Packet System Time 31:0 Snapshot of System time parameter extracted from last serial packet. Bits [31:0]. Taken on the last read of register #37. Time format is as define in CIO spec for Local time.	RO	0
41	VSEC_TMU_CS_41	31:0	Serial Packet System Time 63:32 Snapshot of System time parameter extracted from last serial packet. Bits [63:32]. Taken on the last read of register #37. Time format is as define in CIO spec for Local time.	RO	0
42	VSEC_TMU_CS_42	15:0	Serial Packet System Time 79:64 Snapshot of System time parameter extracted from last serial packet. Bits [79:64]. Taken on the last read of register #37 Time format is as define in CIO spec for Local time.	RO	0
42	VSEC_TMU_CS_42	28:16	Reserved	RO	0
42	VSEC_TMU_CS_42	29	Enable Serial Master Mode When 1 - TMU will send packets on serial out interface, when 0 - TMU will send Null stream on the serial out interface.	R/W	1
42	VSEC_TMU_CS_42	30	Enable Serial Slave Mode When 1 - Serial in packets will be accepted (overrides FLASH configuration), when 0 – dropped.	R/W	0

Table 29. TMU Vendor-Specific Capability Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
42	VSEC_TMU_CS_42	31	Disable Serial Slave Mode When 1 - Serial in packets will be dropped (overrides FLASH configuration), when 0 - will not be dropped.	R/W	0
43	VSEC_TMU_CS_43	31:0	Reserved	RO	0

4.3.1.4.5 GPIO Vendor Specific Registers

The attributes of the GPIO vendor-specific capability registers are described in Table 30.

Note: The register offset is relative to DEV_VSEC_4_BASE in Table 19.

Table 30. GPIO Vendor-Specific Capability Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	VSEC_GPIO_CS_0	7:0	Next Capability Pointer This field defines the double word index of the next capability register set in the device configuration space. It is set to 00h if the Vendor-Specific capability register set is the final register set in the linked list of capability register sets in the device configuration space.	RO	See Pointer in Table 19
0	VSEC_GPIO_CS_0	15:8	Capability ID This field must contain the value 05h indicating this is the start of the Vendor-Specific capability register set.	RO	5
0	VSEC_GPIO_CS_0	23:16	VSEC ID This field is a vendor-defined ID number that indicates the nature and format of the VSEC structure.	RO	4
0	VSEC_GPIO_CS_0	31:24	VSEC Length This field indicates the number of double words in the entire VSEC structure including the header and the Vendor-Specific registers.	RO	34
1	GPIO_CONTROL	0	Periodic Enable When set, enables periodic GPIO message transmission.	R/W	0
1	GPIO_CONTROL	2:1	Periodic Unit 0:1ms, 1:100ms, 2:1sec; 3:Reserved.	R/W	0
1	GPIO_CONTROL	3	Reserved	RO	0
1	GPIO_CONTROL	7:4	GPIO_PDF PDF value used in GPIO messages.	R/W	0xF
1	GPIO_CONTROL	15:8	Periodic Count Amount of Periodic Units between each periodic interrupt.	R/W	10
1	GPIO_CONTROL	31:16	GPIO Interrupt counter Amount of GPIO interrupts to CP uCTL (debug).	R/Clr	0

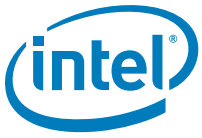
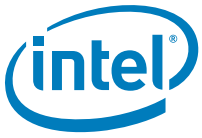


Table 30. GPIO Vendor-Specific Capability Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
2	GPIO_0	0	ENable When set enables this GPIO pin control by Hardware.	R/W	0
2	GPIO_0	1	Out/In Out/In - mode, 1:output, 0: input, regardless of ENable.	R/W	0
2	GPIO_0	2	Output Enable Drives the pin in output mode, regardless of ENable (active low).	R/W	1
2	GPIO_0	3	Data Sampled/driven data, depending on the mode.	R/W	0
2	GPIO_0	4	Changed Status bit. Indicates that the pin has changed since last SW read of the register, regardless of ENable. Useful for polling mode, in case pin is changing frequently (read-only, clear on read).	R/Clr	0
2	GPIO_0	5	INVert Inverts the value to/from the pin.	R/W	0
2	GPIO_0	6	OpenDrain This pin is used for open drain tunneling	R/W	0
2	GPIO_0	27:7	Reserved	RO	0
2	GPIO_0	31:28	InDeX GPIO index.	R/W	0
3	GPIO_1	31:0	Same as GPIO_0	NA	0x4
4	GPIO_2	31:0	Same as GPIO_0	NA	0x4
5	GPIO_3	31:0	Same as GPIO_0	NA	0x4
6	WAKE_N	31:0	Same as GPIO_0, but should only be used in open-drain mode. This is the GPIO recommended for WAKE_N tunneling.	NA	0x4
7	GPIO_5	31:0	Same as GPIO_0	NA	0x4
8	GPIO_6	31:0	Same as GPIO_0	NA	0x4
9	GPIO_7	31:0	Same as GPIO_0	NA	0x4
10	GPIO_8	31:0	Same as GPIO_0	NA	0x4
11	GPIO_9	31:0	Same as GPIO_0	NA	0x4
12	GPIO_10	31:0	Same as GPIO_0	NA	0x4
13	GPIO_11	31:0	Same as GPIO_0	NA	0x4
14	GPIO_12	31:0	Same as GPIO_0	NA	0x4

Table 30. GPIO Vendor-Specific Capability Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
15	GPIO_13	31:0	Same as GPIO_0	NA	0x4
16	GPIO_14	31:0	Same as GPIO_0	NA	0x4
17	GPIO_15	31:0	Same as GPIO_0	NA	0x4
18	Route_String_lo_0	31:0	Route String low DW	R/W	0
19	Route_String_hi_0	31:0	Route String hi DW	R/W	0
20	Route_String_lo_1	31:0	Route String low DW	R/W	0
21	Route_String_hi_1	31:0	Route String hi DW	R/W	0
22	Route_String_lo_2	31:0	Route String low DW	R/W	0
23	Route_String_hi_2	31:0	Route String hi DW	R/W	0
24	Route_String_lo_3	31:0	Route String low DW	R/W	0
25	Route_String_hi_3	31:0	Route String hi DW	R/W	0
26	Route_String_lo_4	31:0	Route String low DW	R/W	0
27	Route_String_hi_4	31:0	Route String hi DW	R/W	0
28	Route_String_lo_5	31:0	Route String low DW	R/W	0
29	Route_String_hi_5	31:0	Route String hi DW	R/W	0
30	Route_String_lo_6	31:0	Route String low DW	R/W	0
31	Route_String_hi_6	31:0	Route String hi DW	R/W	0
32	Route_String_lo_7	31:0	Route String low DW	R/W	0
33	Route_String_hi_7	31:0	Route String hi DW	R/W	0



4.3.1.4.6 SWLESS Vendor Specific Registers

The attributes of the SWLESS vendor-specific capability registers are described in Table 31.

Note: The register offset is relative to DEV_VSEC_5_BASE in Table 19.

Table 31. SWLESS Vendor-Specific Capability Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	VSEC_SWLESS_CS_0	7:0	Next Capability Pointer This field defines the doubleword index of the next capability register set in the device configuration space. It is set to 00h if the Vendor-Specific capability register set is the final register set in the linked list of capability register sets in the device configuration space.	RO	See Pointer in Table 19
0	VSEC_SWLESS_CS_0	15:8	Capability ID This field must contain the value 05h indicating this is the start of the Vendor-Specific capability register set.	RO	5
0	VSEC_SWLESS_CS_0	23:16	VSEC ID This field is a vendor-defined ID number that indicates the nature and format of the VSEC structure.	RO	5
0	VSEC_SWLESS_CS_0	31:24	VSEC Length This field indicates the number of double words in the entire VSEC structure including the header and the Vendor-Specific registers.	RO	17
1	SWLESS0	31:0	General Purpose R/W register for SWLESS feature.	R/W	0
2	SWLESS1	31:0	General Purpose R/W register for SWLESS feature.	R/W	0
3	SWLESS2	31:0	General Purpose R/W register for SWLESS feature.	R/W	0
4	SWLESS3	31:0	General Purpose R/W register for SWLESS feature.	R/W	0
5	SWLESS4	31:0	General Purpose R/W register for SWLESS feature.	R/W	0
6	SWLESS5	31:0	General Purpose R/W register for SWLESS feature.	R/W	0

Table 31. SWLESS Vendor-Specific Capability Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
7	SWLESS6	31:0	General Purpose R/W register for SWLESS feature.	R/W	0
8	SWLESS7	31:0	General Purpose R/W register for SWLESS feature.	R/W	0
9	SWLESS8	31:0	General Purpose R/W register for SWLESS feature.	R/W	0
10	SWLESS9	31:0	General Purpose R/W register for SWLESS feature.	R/W	0
11	SWLESS10	31:0	General Purpose R/W register for SWLESS feature.	R/W	0
12	SWLESS11	31:0	General Purpose R/W register for SWLESS feature.	R/W	0
13	SWLESS12	31:0	General Purpose R/W register for SWLESS feature.	R/W	0
14	SWLESS13	31:0	General Purpose R/W register for SWLESS feature.	R/W	0
15	SWLESS14	31:0	General Purpose R/W register for SWLESS feature.	R/W	0
16	SWLESS15	31:0	General Purpose R/W register for SWLESS feature.	R/W	0

4.3.1.4.7 Link Controller Vendor Specific Registers

The attributes of the Link Controller vendor-specific capability registers are described in Table 33, , Table 65.

Link Controller vendor-specific capability registers are implemented in 2 main sections:

- Common registers - Instanced once and can be indirectly accessed by both uControllers.
- Per uController registers - each uController has its own set of registers that it can directly access. It can also indirectly access the registers of the other controller.

LC_DESC register holds the values describing the registers spaces and addressing. See Figure 21 and Table 32.

Figure 21. LC Vendor-Specific Register Space

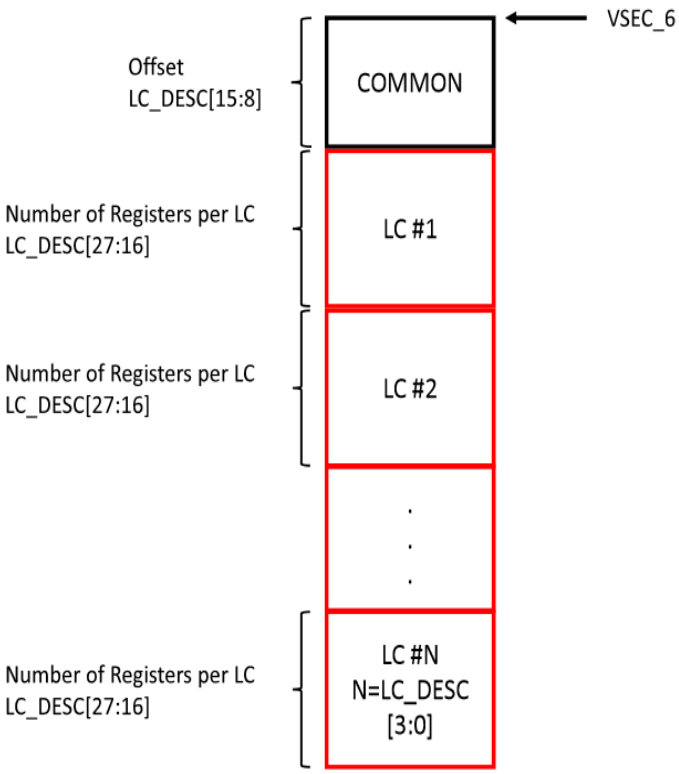


Table 32. LC Vendor-Specific Register Space

Section	Base	Size	Size in Alpine-Ridge DP
Common Registers	DEV_VSEC_6_BASE	LC_DESC[15:8]	20
LC_(N) (N=1,2…)	DEV_VSEC_6_BASE + LC_DESC[15:8] + (N-1)*LC_DESC[27:16]	LC_DESC[27:16]	256 (N=1 for PA, N=2 for PB)

Alpine-Ridge DP implements 2 Link controllers.

In Table 32, the offset indicated is relative to the base of each LC register space.

Link Controller vendor-specific capability registers reside in the LC power-domain.

Table 33. Link Controller Vendor-Specific Capability Common Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x0	VSEC6_HDR	7:0	Next Capability Pointer	RO	0
0x0	VSEC6_HDR	15:8	VSEC Capability	RO	5
0x0	VSEC6_HDR	23:16	VSEC ID	RO	6
0x0	VSEC6_HDR	31:24	VSEC Length	RO	0

Table 33. Link Controller Vendor-Specific Capability Common Register Attributes (Contin-

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x1	EXT_HEADER	15:0	Next Capability Pointer	RO	See Pointer in Table 19
0x1	EXT_HEADER	31:16	LENGTH indicates the length of this configuration space	RO	532
0x2	LC_DESC	3:0	Number of link controllers	RO	2
0x2	LC_DESC	7:4	Reserved	RO	0
0x2	LC_DESC	15:8	Offset of first link controller indicates the offset of first register of first uController	RO	20
0x2	LC_DESC	27:16	Number of registers per link controller	RO	256
0x2	LC_DESC	31:28	Reserved	RO	0
0x3	FUSE0	31:0	Fuse1 carry the 1st double word of fuse value	RO	N/A
0x4	FUSE1	31:0	Fuse2 carry the 2nd double word of fuse value	RO	N/A
0x5	FUSE2	31:0	Fuse3 carry the 3rd double word of fuse value	RO	N/A
0x6	FUSE3	31:0	Fuse4 carry the 4th double word of fuse value	RO	N/A
0x7	AUX_N_CTRL	0	Sel_sw_snk0_aux_n select the source for SNK0 aux_n: 0 - aux_n value is driven by FW from a uController register 1 - aux_n is driven from sw_snk0_aux_n field (by SW)	R/W	0
0x7	AUX_N_CTRL	1	sw_snk0_aux_n SW value of SNK1 aux_n - driven to aux_n signal when SW is selected as aux_n source	R/W	0
0x7	AUX_N_CTRL	2	Sel_sw_snk1_aux_n select the source for SNK1 aux_n: 0 - aux_n value is driven by FW from a uController register 1 - aux_n is driven from sw_snk1_aux_n field (by SW)	R/W	0
0x7	AUX_N_CTRL	3	sw_snk1_aux_n SW value of SNK1 aux_n - driven to aux_n signal when SW is selected as aux_n source	R/W	0
0x7	AUX_N_CTRL	31:4	reserved	RO	0
0x8	EE_COMMON	0	block_ee_reload (when 1 - Allow blocking setting register default value from EPROM auto load).	R/W	0
0x8	EE_COMMON	1	ee_force_dp_hdmi_power_on (When 1 - force dp domain power on regardless FW setting. the value is read from EPROM)**HDP In/Out bypass mode** HDP IN -> OUT HDMI bypass enable	R/W	0

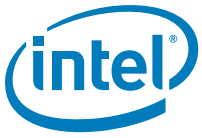


Table 33. Link Controller Vendor-Specific Capability Common Register Attributes (Contin-

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x8	EE_COMMON	2	ee_force_pcie_power_on (When 1 - force pcie domain power on regardless FW setting.the value is read from EPROM)	R/W	0
0x8	EE_COMMON	3	ee_force_usb_xhci_power_on (When 1 – force usb domain power on regardless FW setting.the value is read from EPROM)	R/W	0
0x8	EE_COMMON	4	ee_force_cio_power_on (When 1 – force cio domain power on regardless FW setting.the value is read from EPROM)	R/W	0
0x8	EE_COMMON	5	ee_force_ana_comm_power_on (When 1 – force ana_comm domain power on regardless FW setting.the value is read from EPROM)	R/W	0
0x8	EE_COMMON	6	ee_force_lc_power_on (When 1 – force lc domain power on regardless FW setting.the value is read from EPROM)	R/W	0
0x8	EE_COMMON	7	reserved	RO	0
0x8	EE_COMMON	8	ee_cp_pcie_hide_emep Reflects the value of signal.	R/W	0
0x8	EE_COMMON	9	tmu_pll_calibration_disable (read from EPROM)	R/W	0
0x8	EE_COMMON	31:10	reserved	RO	0
0x9	RESET_CTRL	31:0	clc_ctrl_rst_req_toggle when a bit in this field toggles it cause assertion of specific domain reset.	R/W	0
0xA	HDP_RESET_CTRL	31:0	clc_hdp_ctrl_rst_req_toggle when a bit in this field toggles it cause assertion of specific domain reset.	R/W	0
0xB	GPIO_OWN_CTRL_LOW	31:0	gpio_ownership_reg0 each pair of bits control a specific GPIO pin source according to this encoding: 00 - controlled by control port. 01 - controlled by hardware 10 - link controller A 11 - link controller B Loaded from Flash	R/W	32'h55555555
0xC	GPIO_OWN_CTRL_HIGH	7:0	gpio_ownership_reg1 Controls ownership of DDC_GPIO pins [3:0].Each pair of bits control a specific DDC_GPIO pin source accessing according to this encoding: 00 - controlled by control port. 01 - controlled by hardware 10 - link controller A 11 - link controller B Loaded from flash	R/W	8'h55

Table 33. Link Controller Vendor-Specific Capability Common Register Attributes (Contin-

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0xC	GPIO_OWN_CTRL_HIGH	31:8	reserved	R/W	0
0xD	SEMAPHORE	3:0	Requester encoding encoded requester id: 0 - Reserved 1 – CM 2 - LC_PA 3 - LC_PB 4 - SRC0 5 : 15 - reserved Writable only when semaphore bit was 0	R/W	0
0xD	SEMAPHORE	30:4	Reserved	R/W	0
0xD	SEMAPHORE	31	Semaphore Lock bit. Master should try writing this bit along with its ID. If successfully written, the master won the lock. Master should take care to clear the lock bit as soon as possible	R/W	0
0xE	TBT2PCIE	31:0	Handshake register see Table 38. value driven to PCIE vendor specific configuration space offset 0x548. See Table 123.	R/W	0
0xF	THERMAL_SENSOR	6:0	ts_result_code	RO	0
0xF	THERMAL_SENSOR	7	ts_valid	RO	0
0xF	THERMAL_SENSOR	15:8	thermal_sensor_reg (bit 8 - ts_bit_config bit 9 - ts_start (self_clear) bit 10 - ts_comp_polarity)	R/W	0
0xF	THERMAL_SENSOR	31:16	reserved	RO	0
0x10	DP_SINK_ALLOCATION	3:0	snk0 ownership (Encoding: 0x1-CM/SW. 0x2-PA. 0x3-PB. 0x4-SRC0)	R/W	0
0x10	DP_SINK_ALLOCATION	7:4	snk1 ownership (same encoding as above)	R/W	0
0x10	DP_SINK_ALLOCATION	11:8	I2C master owner	R/W	0
0x10	DP_SINK_ALLOCATION	14:12	reserved general-purpose lock bits	R/W	0
0x10	DP_SINK_ALLOCATION	15	snk0_release_request. Indicate to owner of snk0 that src0 has a connection and would like to connect to snk0	R/W	0
0x10	DP_SINK_ALLOCATION	31:16	reserved general-purpose lock bits	R/W	0
0x11	EE2TAR_FSM_STATUS	31:0	ee2tar_fsm_status	RO	0
0x12	reserved4	31:0	reserved	RO	0
0x13	reserved5	31:0	reserved	RO	0

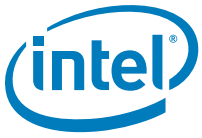


Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x0	VENDOR_ID	23:0	ee_clc_vendor_id IECS (addr 0) vendor ID register from EPROM	RO	0
0x0	VENDOR_ID	31:24	reserved	RO	0
0x1	DEVICE_ID	31:0	ee_clc_device_id IECS (addr 1) device ID register from EPROM	RO	0
0x2	PROTOCOL_VERSION	31:0	ee_clc_protocol_version IECS (addr 2) version register from EPROM	RO	0
0x3	MODE	31:0	ee_clc_mode IECS (addr 3) mode register from EPROM	RO	0
0x4	TYPE	31:0	ee_clc_type IECS (addr 4) type register from EPROM	RO	0
0x5	UUID0	31:0	UUID0 carry value of UUID [31:0] driven from fuse [31:0]	RO	0
0x6	UUID1	31:0	UUID1 carry value of UUID [63:32] driven from fuse [63:32]	RO	0
0x7	UUID2	31:0	UUID2 carry value of UUID [96:64]: driven value of 00000000.	RO	0
0x8	UUID3	31:0	UUID3carry value of UUID [96:64]: {device_id[15:0],14'0,controller instance number[1:0]}	RO	0
0x9	oUUID0	31:0	ouuid0 IECS (addr 6) oUUID register [31:0]	R/W	0
0xA	oUUID1	31:0	ouuid1 IECS (addr 6) oUUID register [63:32]	R/W	0
0xB	oUUID2	31:0	ouuid0 IECS (addr 6) oUUID register [95:64]	R/W	0
0xC	oUUID3	31:0	ouuid0 IECS (addr 6) oUUID register [127:96]	R/W	0
0xD	PCIE2TBT	31:0	Handshake register, see Table 34. value from PCIE vendor specific configuration register offset 0x54C. See Table 124	R/W	0
0xE	IECS_CMD	31:0	iecs_cmd IECS (addr 8) command register	R/W	0

Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0xF	reserved	31:0	reserved	R/W	0
0x10	HVREQ	6:0	ee_clc_port_reg_max_wats	RO	0
0x10	HVREQ	7	hvreq_reg_bpd	R/W	0
0x10	HVREQ	31:8	hvreq	RO	0
0x11	DESCR_HEAD	7:0	byte0 IECS (addr 11) DESCR_HEAD register [7:0]	RO	0
0x11	DESCR_HEAD	15:8	byte1 IECS (addr 11) DESCR_HEAD register [15:9]	RO	0
0x11	DESCR_HEAD	31:16	reserved	RO	0
0x12	LC_CP_STATUS	0	cp_out_of_reset	RO	0
0x12	LC_CP_STATUS	1	cp_upsteam_unplugged	RO	0
0x12	LC_CP_STATUS	2	got pdf=0xd	RO	0
0x12	LC_CP_STATUS	7:3	reserved	RO	0
0x12	LC_CP_STATUS	30:8	reserved	R/W	0
0x12	LC_CP_STATUS	31	lc_xhc_connect	R/W	1
0x13	LC_PHY_TXFFE	3:0	lc_to_phy_txffe_val_c0	R/W	0
0x13	LC_PHY_TXFFE	5:4	reserved	R/W	0
0x13	LC_PHY_TXFFE	6	phy_to_lc_txffe_done_c0	RO	0
0x13	LC_PHY_TXFFE	7	lc_to_phy_txffe_req_c0	R/W	0
0x13	LC_PHY_TXFFE	11:8	lc_to_phy_txffe_val_c1	R/W	0
0x13	LC_PHY_TXFFE	13:12	reserved	R/W	0
0x13	LC_PHY_TXFFE	14	phy_to_lc_txffe_done_c1	RO	0

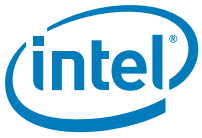


Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x13	LC_PHY_TXFFE	15	lc_to_phy_txffe_req_c1	R/W	0
0x13	LC_PHY_TXFFE	19:16	lc_to_phy_txffe_current_value_c0	R/W	0
0x13	LC_PHY_TXFFE	21:20	lc_to_phy_txffe_val_c0(reserved[5:4])	R/W	0
0x13	LC_PHY_TXFFE	22	reserved	R/W	0
0x13	LC_PHY_TXFFE	23	lc_to_phy_txffe_current_value_valid_c0	R/W	0
0x13	LC_PHY_TXFFE	27:24	lc_to_phy_txffe_current_value_c1	R/W	0
0x13	LC_PHY_TXFFE	29:28	lc_to_phy_txffe_val_c1(reserved[5:4])	R/W	0
0x13	LC_PHY_TXFFE	30	reserved	R/W	0
0x13	LC_PHY_TXFFE	31	lc_to_phy_txffe_current_value_valid_c1	R/W	0
0x14	PHY_LC_TXFFE	3:0	phy_to_lc_txffe_val_c0	RO	0
0x14	PHY_LC_TXFFE	4	phy_to_lc_rx_is_locked_c0	RO	0
0x14	PHY_LC_TXFFE	5	phy_to_lc_rx_is_active_c0	RO	0
0x14	PHY_LC_TXFFE	6	lc_to_phy_txffe_done_c0	R/W	0
0x14	PHY_LC_TXFFE	7	phy_to_lc_txffe_req_c0	RO	0
0x14	PHY_LC_TXFFE	11:8	phy_to_lc_txffe_val_c1	RO	0
0x14	PHY_LC_TXFFE	12	phy_to_lc_rx_is_locked_c1	RO	0
0x14	PHY_LC_TXFFE	13	phy_to_lc_rx_is_active_c1	RO	0
0x14	PHY_LC_TXFFE	14	lc_to_phy_txffe_done_c1	R/W	0
0x14	PHY_LC_TXFFE	15	phy_to_lc_txffe_req_c1	RO	0

Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x14	PHY_LC_TXFFE	19:16	phy_to_lc_txffe_current_value_c0	RO	0
0x14	PHY_LC_TXFFE	21:20	phy_to_lc_txffe_val_c0(reserved[5:4])	RO	0
0x14	PHY_LC_TXFFE	22	reserved	RO	0
0x14	PHY_LC_TXFFE	23	phy_to_lc_tx_is_active_c0	RO	0
0x14	PHY_LC_TXFFE	27:24	phy_to_lc_txffe_current_value_c1	RO	0
0x14	PHY_LC_TXFFE	29:28	phy_to_lc_txffe_val_c1(reserved[5:4])	RO	0
0x14	PHY_LC_TXFFE	30	reserved	RO	0
0x14	PHY_LC_TXFFE	31	phy_to_lc_tx_is_active_c1	RO	0
0x15	VERSION	31:0	version IECS (addr 15) VERSION register	RO	0
0x16	POC_MAILBOX_IN	31:0	poc_lc_mailbox carry mailbox content from power on controller to link controller	RO	0
0x17	POC_MAILBOX_OUT	31:0	lc_poc_mailbox carry mailbox content from link controller to power on controller	R/W	0
0x18	POC_CSR_IN_LOW	31:0	poc_lc_csr0 carry value from power on controller (POC) CSR register [31:0]. See Table 35.	RO	0
0x19	POC_CSR_IN_HIGH	31:0	poc_lc_csr1 carry value to be written to power on controller CSR register [63:32]. POC CSR is written when lc_poc_csr_latch is asserted. See Table 35.	RO	0
0x1A	POC_CSR_OUT_LOW	31:0	lc_poc_csr0 carry value to be written to POC CSR [31:0]. POC CSR is written when lc_poc_csr_latch is asserted. See Table 35.	R/W	0
0x1B	POC_CSR_OUT_HIGH	31:0	lc_poc_csr1 carry value to be written to POC CSR [63:32]. POC CSR is written when lc_poc_csr_latch is asserted. See Table 35.	R/W	0x0210_0000

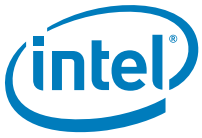


Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x1C	POC_CTRL	0	lc_poc_csr_latch when asserted latch the value from poc_lc_csr1 and poc_lc_csr0 into POC CSR. See Table 35.	R/W SC	0
0x1C	POC_CTRL	1	lc_poc_mailbox_latch when asserted latch the value from poc_lc_mailbox POC mailbox register.	R/W SC	0
0x1C	POC_CTRL	2	lc_power_off_req when asserted indicate that this link controller ask to shut of its power domain, the shut off request takes place only when all link controller have asserted this bit.	R/W	0
0x1C	POC_CTRL	3	lc_poc_csr_common_latch	R/W SC	0
0x1C	POC_CTRL	4	lc_poc_usb_osc_1m_calib_latch	R/W SC	0
0x1C	POC_CTRL	5	lc_poc_ramp_ctrl_latch	R/W SC	0
0x1C	POC_CTRL	6	lc_poc_osc_curr_tune_latch	R/W SC	0
0x1C	POC_CTRL	7	lc_poc_usb_sx_sw_ctrl_latch	R/W SC	0
0x1C	POC_CTRL	8	poc_csr_ready indicate that the POC CSR is ready for asserting the lc_poc_csr_latch. See Table 35	RO	0
0x1C	POC_CTRL	9	poc_mailbox_ready indicate that the POC CSR is ready for asserting the lc_poc_mailbox_latch.	RO	0
0x1C	POC_CTRL	10	lc_power_off_requested When asserted indicates to the link controller that all link controller have asserted their power shut off requests and the power off process has started. In a case where a link controller has changed his mind after requesting power off - it should deassert lc_power_off_req and should read this bit to verify that regression succeeded.	RO	0
0x1C	POC_CTRL	11	poc_isolation_en indicates that power on controller has disconnected its input from link controller.	RO	0
0x1C	POC_CTRL	12	poc_csr_common_ready	RO	0

Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x1C	POC_CTRL	13	lc_poc_usb_osc_1m_calib_ready	RO	0
0x1C	POC_CTRL	14	poc_lc_ramp_ctrl_ready	RO	0
0x1C	POC_CTRL	15	poc_lc_osc_curr_tune_ready	RO	0
0x1C	POC_CTRL	16	lc_poc_usb_sx_sw_ctrl_ready	RO	0
0x1C	POC_CTRL	31:17	reserved	RO	0
0x1D	POC_OSC_SCALE	0	lc_poc_scale_latch cause power on controller to latch the value lc_poc_scale.	R/W Self CLR	0
0x1D	POC_OSC_SCALE	1	lc_poc_scale_latch_open	R/W	0
0x1D	POC_OSC_SCALE	2	poc_osc_scale_sel	R/W	0
0x1D	POC_OSC_SCALE	3	pll_cal_manual_mode	R/W	0
0x1D	POC_OSC_SCALE	4	poc_lc_scale_ready	RO	0
0x1D	POC_OSC_SCALE	5	reserved	RO	0
0x1D	POC_OSC_SCALE	6	fuse_to_poc_calibration_reg[8] - valid	RO	0
0x1D	POC_OSC_SCALE	7	fuse_to_poc_calibration_reg[9] - reserved	RO	0
0x1D	POC_OSC_SCALE	15:8	fuse_to_poc_calibration_reg	RO	0
0x1D	POC_OSC_SCALE	23:16	poc_lc_scale carry the actual value of POC scale (from power on controller)	RO	8'h7E
0x1D	POC_OSC_SCALE	31:24	pll_cal_force_value (forced value for osc calibration when in manual mode)	R/W	8'h7E
0x1E	POC_PWR_CTRL	2:0	lc_poc_ramp_ctrl_lc_3p3 carry the control bus to POC for LC domain 3.3 switch power up speed. Implemented for PA only.	R/W	0
0x1E	POC_PWR_CTRL	3	Reserved	RO	0
0x1E	POC_PWR_CTRL	6:4	lc_poc_ramp_ctrl_lc_0p9 carry the control bus to POC for LC domain 0.9 switch power up speed. Implemented for PA only.	R/W	0

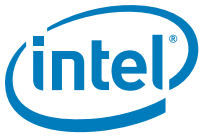


Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x1E	POC_PWR_CTRL	7	Reserved	RO	0
0x1E	POC_PWR_CTRL	10:8	poc_lc_ramp_ctrl_lc_3p3 carry value stored in POC for LC 3.3 switch power up speed.	RO	4
0x1E	POC_PWR_CTRL	11	reserved	RO	0
0x1E	POC_PWR_CTRL	14:12	poc_lc_ramp_ctrl_lc_0p9 carry value stored in POC for LC 0.9 switch power up speed.	RO	4
0x1E	POC_PWR_CTRL	15	reserved	RO	0
0x1E	POC_PWR_CTRL	20:16	lc_poc_osc_curr_tune	R/W	18
0x1E	POC_PWR_CTRL	23:21	reserved	RO	0
0x1E	POC_PWR_CTRL	28:24	poc_lc_osc_curr_tune	RO	18
0x1E	POC_PWR_CTRL	31:29	reserved	RO	0
0x1F	LINK_CTRL	0	filtered_ls_g1 carry the ls_g1 pin value after filter.	RO	0
0x1F	LINK_CTRL	1	filtered_ls_g2 carry the ls_g2 pin value after filter.	RO	0
0x1F	LINK_CTRL	2	filtered_ls_g3 carry the ls_g3 pin value after filter.	RO	0
0x1F	LINK_CTRL	3	filtered_power_ctrl carry power_ctrl pin value after filter.	RO	0
0x1F	LINK_CTRL	4	ls_g1_val carry the ls_g1 pin value before filter	RO	0
0x1F	LINK_CTRL	5	ls_g2_val carry the ls_g2 pin value before filter	RO	0
0x1F	LINK_CTRL	6	ls_g3_val carry the ls_g3 pin value before filter	RO	0
0x1F	LINK_CTRL	7	power_ctrl_val carry the power_ctrl pin value before filter	RO	0

Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x1F	LINK_CTRL	8	ls_g1_changed_sticky indicates that the ls_g1 has been changed from last time that this bit has been cleared	R/W SC	0
0x1F	LINK_CTRL	9	ls_g2_changed_sticky indicates that the ls_g2 has been changed from last time that this bit has been cleared	R/W SC	0
0x1F	LINK_CTRL	10	ls_g3_changed_sticky indicates that the ls_g3 has been changed from last time that this bit has been cleared	R/W SC	0
0x1F	LINK_CTRL	11	pwr_ctrl_changed_sticky indicates that the pwr_ctrl has been changed from last time that this bit has been cleared	R/W SC	0
0x1F	LINK_CTRL	12	ls_g1_change_interrupt_dis when asserted, it blocks the interrupt to the controller upon value change of ls_g1 pin as input.	R/W	0
0x1F	LINK_CTRL	13	ls_g2_change_interrupt_dis when asserted, it blocks the interrupt to the controller upon value change of ls_g2 pin as input.	R/W	0
0x1F	LINK_CTRL	14	ls_g3_change_interrupt_dis when asserted, it blocks the interrupt to the controller upon value change of ls_g3 pin as input.	R/W	0
0x1F	LINK_CTRL	15	pwr_ctrl_change_interrupt_dis when asserted, it blocks the interrupt to the controller upon value change of pwr_ctrl pin as input.	R/W	0
0x1F	LINK_CTRL	16	filtered_src0_hpd carry the src0_hpd pin value after filter.	RO	0
0x1F	LINK_CTRL	17	src0_hpd_val carry the src0_hpd pin value before filter	RO	0
0x1F	LINK_CTRL	18	src0_hpd_changed_sticky indicates that the src0_hpd has been changed from last time that this bit has been cleared	R/W SC	0
0x1F	LINK_CTRL	19	src0_hpd_change_interrupt_dis when asserted, it blocks the interrupt to the controller upon value change of src0_hpd pin as input.	R/W	0
0x1F	LINK_CTRL	20	filtered_src0_cfg1 carry src0_cfg1 pin value after filter.	RO	0

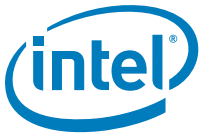


Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x1F	LINK_CTRL	21	src0_cfg1_val carry the src0_cfg1 pin value before filter	RO	0
0x1F	LINK_CTRL	22	src0_cfg1_changed_sticky indicates that the src0_cfg1 has been changed from last time that this bit has been cleared	R/W SC	0
0x1F	LINK_CTRL	23	src0_cfg1_change_interrupt_dis when asserted, it blocks the interrupt to the controller upon value change of src0_cfg1 pin as input.	R/W	0
0x1F	LINK_CTRL	24	ls_g1_pad_o carry the value to be driven on ls_g1 pin when set to be output.	R/W	0
0x1F	LINK_CTRL	25	ls_g2_pad_o carry the value to be driven on ls_g2 pin when set to be output.	R/W	0
0x1F	LINK_CTRL	26	ls_g3_pad_o carry the value to be driven on ls_g3 pin when set to be output.	R/W	0
0x1F	LINK_CTRL	27	power_ctrl_pad_o carry the value to be driven on power_ctrl pin when set to be output.	R/W	0
0x1F	LINK_CTRL	28	ls_g1_padoe_o when asserted, it set the ls_g1 pin direction to be output	R/W	0
0x1F	LINK_CTRL	29	ls_g2_padoe_o when asserted, it set the ls_g2 pin direction to be output	R/W	0
0x1F	LINK_CTRL	30	ls_g3_padoe_o when asserted, it set the ls_g3 pin direction to be output	R/W	0
0x1F	LINK_CTRL	31	power_ctrl_padoe_o when asserted, it set the power_ctrl pin direction to be output	R/W	0
0x20	LSOE	0	block_clc_lsoe_connect_rise_pulse_c0 When asserted, it blocks HW detection of lane 0 connect rise messages, from received uart packets.	R/W	1

Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x20	LSOE	1	block_clc_lsoe_connect_rise_pulse_c1 When asserted, it blocks HW detection of lane 1 connect rise messages, from received uart packets.	R/W	1
0x20	LSOE	2	block_clc_lsoe_connect_fall_pulse_c0 When asserted, it blocks HW detection of lane 0 connect fall messages, from received uart packets.	R/W	1
0x20	LSOE	3	block_clc_lsoe_connect_fall_pulse_c1 When asserted, it blocks HW detection of lane 1 connect fall messages, from received uart packets.	R/W	1
0x20	LSOE	4	block_clc_lsoe_resume_pulse_c0 When asserted, it blocks HW detection of lane 0 resume messages, from received uart packets.	R/W	1
0x20	LSOE	5	block_clc_lsoe_resume_pulse_c1 When asserted, it blocks HW detection of lane 1 resume messages, from received uart packets.	R/W	1
0x20	LSOE	6	reserved	R/W	1
0x20	LSOE	7	reserved	R/W	1
0x20	LSOE	8	clc_lsoe_connect_rise_pulse_c0 writing 1 to this bit will generate a connect rise pulse to lane 0.	R/W SC	0
0x20	LSOE	9	clc_lsoe_connect_rise_pulse_c1 writing 1 to this bit will generate a connect rise pulse to lane 1.	R/W SC	0
0x20	LSOE	10	clc_lsoe_connect_fall_pulse_c0 writing 1 to this bit will generate a connect fall pulse to lane 0.	R/W SC	0
0x20	LSOE	11	clc_lsoe_connect_fall_pulse_c1 writing 1 to this bit will generate a connect fall pulse to lane 1.	R/W SC	0
0x20	LSOE	12	clc_lsoe_resume_pulse_c0 writing 1 to this bit will generate a resume pulse to lane 0.	R/W SC	0
0x20	LSOE	13	clc_lsoe_resume_pulse_c1 writing 1 to this bit will generate a resume pulse to lane 1.	R/W SC	0
0x20	LSOE	14	reserved	R/W SC	0

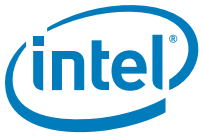


Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x20	LSOE	15	reserved	R/W SC	0
0x20	LSOE	16	clc_lsoe_resume_status_c0 indicates the resume status of lane 0: 0 - the lane hasn't received a resume pulse 1 - the lane has received a resume pulse	RO	0
0x20	LSOE	17	clc_lsoe_resume_status_c1 indicates the resume status of lane 1: 0 - the lane hasn't received a resume pulse 1 - the lane has received a resume pulse	RO	0
0x20	LSOE	31:18	reserved	RO	0
0x21	LSEO	0	block_hw_send_connect_fall_c0 when asserted, it blocks the hw generating LT rise uart packet on lstx as result of detection lane 0 LSEO fall.	R/W	1
0x21	LSEO	1	block_hw_send_250us_c0 when asserted, it blocks the hw generating LT rise uart packet on lstx as result of detection lane 0 LSEO connect rise.	R/W	1
0x21	LSEO	2	block_hw_send_2ms_c0 when asserted, it blocks the hw generating LT rise uart packet on lstx as result of detection lane 0 LSEO reset rise.	R/W	1
0x21	LSEO	3	block_hw_send_lseo_fall_c0 when asserted, it blocks the hw generating LT fall uart packet on lstx as result of detection lane 0 LSEO reset fall.	R/W	1
0x21	LSEO	4	block_hw_send_resume_c0 when asserted, it blocks the hw generating LT resume uart packet on lstx as result of detection lane 0 LSEO resume.	R/W	1
0x21	LSEO	5	reserved	R/W	0
0x21	LSEO	6	cio_lane0_connected_sync_c0 when 1 - indicates that the local cio lane0 is in connected state		
0x21	LSEO	7	clc_lseo_resume_status_c0 indicate the status of lane 0 LSEO resume: 0 - the lane has not yet generated a resume indication. 1 - the lane has generated a resume indication.	RO	0

Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x21	LSEO	8	block_hw_send_connect_fall_c1 when asserted, it blocks the hw generating LT rise uart packet on lstx as result of detection lane 1 LSEO fall.	R/W	1
0x21	LSEO	9	block_hw_send_250us_c1 when asserted, it blocks the hw generating LT rise uart packet on lstx as result of detection lane 1 LSEO connect rise.	R/W	1
0x21	LSEO	10	block_hw_send_2ms_c1 when asserted, it blocks the hw generating LT rise uart packet on lstx as result of detection lane 1 LSEO reset rise.	R/W	1
0x21	LSEO	11	block_hw_send_lseo_fall_c1 when asserted, it blocks the hw generating LT fall uart packet on lstx as result of detection lane 1 LSEO reset fall.	R/W	1
0x21	LSEO	12	block_hw_send_resume_c1 when asserted, it blocks the hw generating LT resume uart packet on lstx as result of detection lane 1 LSEO resume.	R/W	1
0x21	LSEO	13	reserved	R/W	0
0x21	LSEO	14	cio_lane1_connected_sync_c0 when 1 - indicates that the local cio lane1 is in connected state	R/W	0
0x21	LSEO	15	clc_lseo_resume_status_c1 indicate the status of lane 1 LSEO resume: 0 - the lane has not yet generated a resume indication. 1 - the lane has generated a resume indication.	RO	0
0x21	LSEO	16	fw_send_lseo_connect_fall_c0 Writing 1 to this bit, will send LT fall uart packet of lane 0 on lstx.	R/W SC	0
0x21	LSEO	17	fw_send_250us_c0 Writing 1 to this bit, will send LT rise uart packet of lane 0 on lstx.	R/W SC	0
0x21	LSEO	18	fw_send_2ms_c0 Writing 1 to this bit, will send LT rise uart packet of lane 0 on lstx	R/W SC	0
0x21	LSEO	19	fw_send_lseo_fall_c0 Writing 1 to this bit, will send LT fall uart packet of lane 0 on lstx.	R/W SC	0

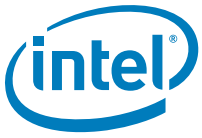


Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x21	LSEO	20	fw_send_resume_c0 Writing 1 to this bit, will send LT resume uart packet of lane 0 on lstx.	R/W SC	0
0x21	LSEO	23:21	reserved	RO	0
0x21	LSEO	24	fw_send_lseo_connect_fall_c1 Writing 1 to this bit, will send LT fall uart packet of lane 1 on lstx.	R/W SC	0
0x21	LSEO	25	fw_send_250us_c1 Writing 1 to this bit, will send LT rise uart packet of lane 0 on lstx.	R/W SC	0
0x21	LSEO	26	fw_send_2ms_c1 Writing 1 to this bit, will send LT rise uart packet of lane 0 on lstx.	R/W SC	0
0x21	LSEO	27	fw_send_lseo_fall_c1 Writing 1 to this bit, will send LT fall uart packet of lane 0 on lstx.	R/W SC	0
0x21	LSEO	28	fw_send_resume_c1 Writing 1 to this bit, will send LT resume uart packet of lane 0 on lstx.	R/W SC	0
0x21	LSEO	31:29	reserved	RO	0
0x22	FROM_LINK_ PARTNER	31:0	clc_from_link_uctl_partner this register carry the FW status of other controller. This can be read by the actual controller to decide on subjects that should consider the other controller status.	RO	0
0x23	TO_LINK_PAR TNER	31:0	clc_to_link_uctl_partner this register carry the FW status of actual controller. This can be read by the other controller to decide on subjects that should consider the other controller status.	R/W	0
0x24	TAR_DATA	31:0	clc_tar_wr_data When written - carry the data to be written to target interface upon write access setting on TAR_CTRL register When read – drive the last data has been read from target interface.	R/W	0
0x25	TAR_CTRL	12:0	clc_tar_dw_index this field carry the address of target register that is accessed through target interface.	R/W	0

Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x25	TAR_CTRL	18:13	clc_tar_port this field carry the port index of target register that is accessed through target interface.	R/W	0
0x25	TAR_CTRL	20:19	clc_tar_cs this field carry the chip select of target register that is accessed through target interface.	R/W	0
0x25	TAR_CTRL	21	clc_tar_wr1_rd0 this bit carry the access type, when a register is accessed through the target interface 0 - read access 1 - write access	R/W	0
0x25	TAR_CTRL	22	clc_cio_sw_regs_access when this bit is asserted, it indicate that the access is directed to cio switch register space.	R/W	0
0x25	TAR_CTRL	23	clc_pcie_sw_regs_access when this bit is asserted, it indicate that the access is directed to pcie switch register space.	R/W	0
0x25	TAR_CTRL	24	regs_init_done_pulse	R/W	0
0x25	TAR_CTRL	25	reserved	RO	0
0x25	TAR_CTRL	26	clc_master_lock will cause target arbiter to lock arbitration and allow access only to this link controller until this bit is cleared.	R/W	0
0x25	TAR_CTRL	29:27	Reserved	RO	0
0x25	TAR_CTRL	30	clc_tar_timeout target access completion status bit: 0 - indicates that the last target access was implemented successfully. 1 - indicates that the last target access did finish due to timeout.	RO	0
0x25	TAR_CTRL	31	clc_tar_pending target access status bit: 0 - indicates that the last target access was acknowledged, and target arbiter is ready to get another access. 1 - indicates that the last target access is still pending.	RO	0
0x26	SW_FW_MAILBOX_IN	0	got_iecs_cmd_from_sw this bit indicates that an iecs_cmd from CM is pending at SW_FW_MAILBOX_IN_DATA0.	R/W SC	0

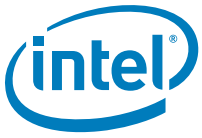


Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x26	SW_FW_MAIL BOX_IN	1	do_not_power_on_cio control for debug - this bit tell the FW not to power on the CIO domain when a TBT cable is detected	R/W	0
0x26	SW_FW_MAIL BOX_IN	2	debug_sw_stop_iecs_handshake for debug only: stop iecs handshake (if stuck), to allow clean packet generation by msg_out_ctrl	R/W	0
0x26	SW_FW_MAIL BOX_IN	3	Reserved	R/W	0
0x26	SW_FW_MAIL BOX_IN	4	debug_halt_fw halt LC fw in the beginning of the main loop (if it gets there). FW will continue once this bit is cleared	R/W	0
0x26	SW_FW_MAIL BOX_IN	5	sw_no_dpp allow sw to force no redriver. S	R/W	0
0x26	SW_FW_MAIL BOX_IN	6	sw_force_lstx_low forces lstx low as long as cio power is on	R/W	0
0x26	SW_FW_MAIL BOX_IN	7	sw_force_no_dpp_src0 Allow SW to force no redriver on src0	R/W	0
0x26	SW_FW_MAIL BOX_IN	8	force_power_off_enable when set will force a power cycle after some delay	R/W	0
0x26	SW_FW_MAIL BOX_IN	12:9	force_power_off_delay the delay before forcing a power cycle, in steps of ~2ms	R/W	0
0x26	SW_FW_MAIL BOX_IN	31:13	mailbox_in reserved for future definitions	R/W	0
0x27	SW_FW_MAIL BOX_OUT	31:0	mailbox_out carry the content of FW messages to SW	R/W	0
0x28	UCODE_LOAD	0	eep_done EPROM auto load status: 0 - indicates that the auto load has not finished yet. 1 - indicates that the auto load has finished	RO	0
0x28	UCODE_LOAD	1	ee_no_flash eprom exist status: 0 -EPROM exist 1 - EPROM less mode	RO	0
0x28	UCODE_LOAD	2	flash_ctrl_is_busy	RO	0

Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x28	UCODE_LOAD	3	ee_to_tar_ana_comm_done	RO	0
0x28	UCODE_LOAD	15:4	reserved	RO	0
0x28	UCODE_LOAD	31:16	ee_section_done indicate that the EPROM section load is done (with extra bits)	RO	0
0x29	GENERAL	0	ee_router_switch_n mode bit from EPROM 0: chip is in switch/endpoint configuration 1: chip is in Host Router configuration	R/W	0
0x29	GENERAL	1	ee_clc_connector_type mode bit from EPROM 0 indicate that the connector type is electrical 1 indicates that the connector type is optical	R/W	0
0x29	GENERAL	3:2	uctl_instance_num mode bit from EPROM indicate the actual controller index.	RO	0/1
0x29	GENERAL	4	ee_clc_port_enable mode bit from EPROM 1 port is enabled 0 port is disabled	R/W	0
0x29	GENERAL	5	ee_clc_tethered_cable mode bit from EPROM, indicates that the cable is not connected through connector - it is a tethered cable. When this bit is set - the external muxes control pins are used as GPIO.	R/W	0
0x29	GENERAL	6	ee_clc_debug_disable_uart 0 - uart is enabled 1 - uart is disabled	R/W	0
0x29	GENERAL	7	ee_clc_bypass_mode When this bit is asserted the controller set the mode due to external pins.	R/W	0
0x29	GENERAL	9:8	ee_clc_power_src 10 – self powered device (spd), 01 – bus powered device (bpd), 11 – dual power device (dpd).	R/W	0
0x29	GENERAL	11:10	ee_clc_lane_disabled When one of these bits is 1 - it indicates that the appropriate lane is disabled.	R/W	0

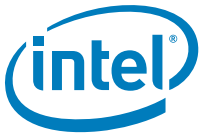


Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x29	GENERAL	12	ee_clc_power_cio_on_initial_wake When this bit is asserted cio will powered on each initial wake. If used, it is SW responsibility to reset this bit in order to release cio power to normal operation	R/W	0
0x29	GENERAL	13	ee_clc_power_cio_on_force_pwr_wake Controls whether LC will power on the cio domain upon assertion of gpio3_force_pwr. 0 – will not power on 1 – will power on	R/W	0
0x29	GENERAL	14	cp_clc_ok_to_go_to_sx when 1 Indication from CP that it is ok to move to sleep mode (SX)	RO	0
0x29	GENERAL	15	car_comm_perst_and_pwgd Status of the internal perst signal. LC uses this indication during Sx entry.	RO	0
0x29	GENERAL	16	cio_reset_asserted_sync indicates that the cio domain reset is being asserted.	RO	0
0x29	GENERAL	17	ior_strp_secur_en_sync reflects security strap value	RO	0
0x29	GENERAL	18	secure_en_sync When set to 1 indicates that security mode is enabled.	RO	0
0x29	GENERAL	19	ior_probe_mode_sync Indicates that the few functional pins are functioning in debug mode.	RO	0
0x29	GENERAL	20	ee_clc_debug_disable_uart_2 0 - uart_2 is enabled 1 - uart_2 is disabled	R/W	0
0x29	GENERAL	21	pcie_custom_l2_logic_reset_ad_Dn_p0	RO	0
0x29	GENERAL	22	pcie_custom_l2_logic_reset_ad_Dn_p1	RO	0
0x29	GENERAL	23	countdown_run1_done0	R/W SC	0
0x29	GENERAL	24	pcie_clkreq_disable disable assertion CLRREQ pin of pcie i/f	R/W	0
0x29	GENERAL	25	pad2mux_i_perst_n_sync reflects perst pin value	RO	0
0x29	GENERAL	28:26	reserved_lock_bits	RO	0

Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x29	GENERAL	29	snk1_release_request	RO	0
0x29	GENERAL	30	clc_cm_interrupt Writing 1 to this bit will cause an interrupt to connection manager controller		0
0x29	GENERAL	31	clc_cp_interrupt Writing 1 to this bit will cause an interrupt to the CP.	R/W SC	0
0x2A	LINK_MODE	0	clc_cio_swap_lanes indicate thet in the relevant port was connected inverted, and cio need to swap lanes.	R/W	0
0x2A	LINK_MODE	1	clc_dp_swap_lanes indicate thet in the relevant port was connected inverted, and dp need to swap lanes.	R/W	0
0x2A	LINK_MODE	2	lc_usb_lane_sel when 1 select lane 1, when 0 select lane 0.	R/W	0
0x2A	LINK_MODE	3	reserved	R/W	0
0x2A	LINK_MODE	4	xtal_dig_stable_lc indication from car that the xtal is stable	RO	0
0x2A	LINK_MODE	5	clc_xtal_rst reset to the clock logic active high	R/W	0
0x2A	LINK_MODE	6	lc_cio_speed indicated the lane speed (10G or 20G)	R/W	0
0x2A	LINK_MODE	7	clc_car_change_to_xtal indicate the clock logic to switch to crystal	R/W	0
0x2A	LINK_MODE	8	reserved	R/W	0
0x2A	LINK_MODE	9	lc_cio_mode	R/W	0
0x2A	LINK_MODE	10	lc_dp_mode	R/W	0
0x2A	LINK_MODE	11	lc_usb2_mode	R/W	0
0x2A	LINK_MODE	12	lc_usb3_mode	R/W	0
0x2A	LINK_MODE	13	lc_dp_multi_function_mode this mode ls usb and dp in the same mode	R/W	0
0x2A	LINK_MODE	14	reserved	R/W	0

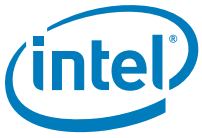


Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x2A	LINK_MODE	15	ee_cdr_mode_en read from eeprom bit.	RO	0
0x2A	LINK_MODE	18:16	lc_crux_sel internal muxes control. 0:unplugged, 1:snk0->pa/b, 2:snk1->pa/b, 3:cio, 4:reserved, 5-tunnel_h00, 6-tunnel_h01, 7-reserved	R/W	0
0x2A	LINK_MODE	19	reserved	R/W	0
0x2A	LINK_MODE	20	uuid_equals_ouuid when set, LC has detected that ouuid equals it's uuid	R/W	0
0x2A	LINK_MODE	21	clc_src_hdmi1_dp0 internal mux control. 0:dp, 1:hdmi**HDP In/ Out bypass mode** HDP IN -> OUT HDMI bypass enable	R/W	0
0x2A	LINK_MODE	22	clc_snk1_aux_n indication to snk1 adapter that the sink is free for tunneling (1) or used by a redriver (0).	R/W	1
0x2A	LINK_MODE	23	clc_snk0_aux_n indication to snk1 adapter that the sink is free for tunneling (1) or used by a redriver (0).	R/W	1
0x2A	LINK_MODE	24	src0_lc_hdmi1_dp0 internal mux control for src0. 0:dp, 1:hdmi**HDP In/Out bypass mode** HDP IN -> OUT HDMI bypass enable	R/W	0
0x2A	LINK_MODE	25	clc_power_down_req request an approval from CP to power down the CIO domain.	R/W	0
0x2A	LINK_MODE	26	clc_power_down_requested indication that both LCs requested to power off CIO domain.	RO	0
0x2A	LINK_MODE	27	cp_power_down_ack indication from CP that it is safe to power off the CIO domain.	RO	0
0x2A	LINK_MODE	30:28	src0_lc_crux_sel internal muxes control for src0. 0:unplugged, 1:snk0->pa/b, 2:snk1->pa/b, 3:cio, 4:reserved, 5-tunnel_h00, 6-tunnel_h01, 7-reserved	R/W	0
0x2A	LINK_MODE	31	lc_usb_plugged	R/W	0

Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x2B	CHICKEN_BITS	0	map_rom_to_ram for debug - rom accesses will be directed to the patch ram. Can only be set from flash.	R/W	From FLASH
0x2B	CHICKEN_BITS	1	link_20g_supported indicate that the device supports 20 link.	R/W	0
0x2B	CHICKEN_BITS	2	dual_lane_supported indicate that the device supports lane aggregation. Must align with digital section bits.	R/W	0
0x2B	CHICKEN_BITS	3	reserved	R/W	0
0x2B	CHICKEN_BITS	4	apple_host_mode Apple Cm sx entry flow and other Apple related host stuff.	R/W	0
0x2B	CHICKEN_BITS	5	sx_treat_interdomain_as_disconnected when set, interdomain links will be treated as disconnected	R/W	From FLASH
0x2B	CHICKEN_BITS	6	disable_sx_entry When set, sx entry is disabled. Automatically set in no_flash mode	R/W	From FLASH
0x2B	CHICKEN_BITS	7	src0_tunnel_only should be set on EPs and hosts with src0 connected to internal display.	R/W	0 Set on EP and hosts using SRC0
0x2B	CHICKEN_BITS	8	dp_allocation_port_preference select which snk is preferred when enable_special_dp_allocation is set.	R/W	0
0x2B	CHICKEN_BITS	9	do_dp_allocation_for_src0 select which snk is handles src0.	R/W	0
0x2B	CHICKEN_BITS	10	dp_allocation_src0_preference select which snk is preferred for src0 when enable_special_dp_allocation is set.	R/W	0
0x2B	CHICKEN_BITS	11	src0_tunnel_adapter_select HR only. choose which DP adapter to configure for SRC0 tunnel	R/W	0
0x2B	CHICKEN_BITS	12	dpp_cable_tunnel1_redriver0. should be set on Eps. Choose to connect a DP cable on the port to tunnel or redrive	R/W	0

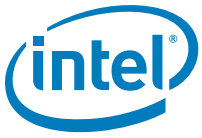


Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x2B	CHICKEN_BITS	13	sx_treat_bpd_as_disconnected Disconnect any BPDs on Sx entry (needed for AIC).	R/W	0
0x2B	CHICKEN_BITS	14	Reserved	R/W	0
0x2B	CHICKEN_BITS	15	Reserved	R/W	0
0x2B	CHICKEN_BITS	17:16	bus_powered_lane_enable lane_en bits for bpd or dpd w/o ac	R/W	From FLASH
0x2B	CHICKEN_BITS	18	low_voltage_bpd when set and the device is a bpd (or dpd without ac) - device behaves as a low voltage bpd. will set hv_req[7:7] to 0.	R/W	From FLASH
0x2B	CHICKEN_BITS	19	redriver_only_security_mode when set, cio domain will stay off, unless force_pwr is asserted. this setting is static, for hosts only	R/W	From FLASH
0x2B	CHICKEN_BITS	20	legacy_lt_use_loopback use loopback mode for lt handshake with legacy device.	R/W	0
0x2B	CHICKEN_BITS	21	enforce_plug_event_delay. enforce 5 sec delay b/w connecting / disconnecting PCIe entities	R/W	0
0x2B	CHICKEN_BITS	22	spd_wait_for_hv_ok_before_iecs when set, will wait for hv_ok also for SPDs. Used for silverbox power based devices.	R/W	0
0x2B	CHICKEN_BITS	23	pcie_only_device no need to turn on dp with cio.	R/W	0
0x2B	CHICKEN_BITS	24	delay_initial_wake	R/W	0
0x2B	CHICKEN_BITS	25	disable_delay_cio_shutdown_timer	R/W	0
0x2B	CHICKEN_BITS	26	Reserved	R/W	0
0x2B	CHICKEN_BITS	27	block_target_writes_when_secure_en	R/W	0
0x2B	CHICKEN_BITS	28	dft_fast_power_up_only do full chip fast power-up, then halt	R/W	0

Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x2B	CHICKEN_BITS	29	dft_fw_fast_sim	R/W	0
0x2B	CHICKEN_BITS	30	dft_skip_all_iecs	R/W	0
0x2B	CHICKEN_BITS	31	dft_dft_skip_cdr_iecs_stages	R/W	0
0x2C	UART_HW_CTRL	0	block_uart_tx When asserted, will block the uart tx, value of 0 will be driven on lstx.	RW	1
0x2C	UART_HW_CTRL	1	block_uart_rx When asserted, will block the uart rx.	RW	1
0x2C	UART_HW_CTRL	2	block_hw_tx_ls when asserted, will block detection of LT packets by hw.	RW	1
0x2C	UART_HW_CTRL	3	fw_lstx_oen 0 - force lstx been output. 1 - output enable of lstx is controlled by uart FSM	RW	1
0x2C	UART_HW_CTRL	4	fw_lstx_o drive the value of lstx output pad when fw_lstx_oen is set to 0.	RW	0
0x2C	UART_HW_CTRL	5	reserved	RW	0
0x2C	UART_HW_CTRL	6	en_hw_rx_fsm enable the uart receive FSM	RW	0
0x2C	UART_HW_CTRL	7	en_loopback enables loopback mode for lt puckets in legacy devices	RW	0
0x2C	UART_HW_CTRL	8	sw_rst_tx when written to 1 apply soft reset to uart tx FSM	RW SC	0
0x2C	UART_HW_CTRL	9	sw_rst_rx when written to 1 apply soft reset to uart rx FSM	RW SC	0
0x2C	UART_HW_CTRL	11:10	reserved	RO	0
0x2C	UART_HW_CTRL	12	fw_en_rx_tx_ctrl enables loopback mode for lt puckets in legacy devices	RW	1

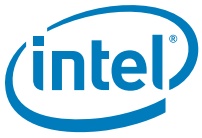


Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x2C	UART_HW_CTRL	13	disable_lsle_ctrl_fsm	RW	0
0x2C	UART_HW_CTRL	14	disable_lsod_detect_fsm	RW	0
0x2C	UART_HW_CTRL	23:15	reserved	RW	0
0x2C	UART_HW_CTRL	31:24	reserved	RW	0
0x2D	UART_RX	0	uart_during_rx status indicate that the uart is during receive traffic.	RO	0
0x2D	UART_RX	1	rx_pkt_has_err status indicates that the last rx packet had error.	RW	0
0x2D	UART_RX	2	urx_fifo_full status indicates that the receive fifo of uart AT packets is full	RO	0
0x2D	UART_RX	3	urx_fifo_empty status indicates that the receive fifo of uart AT packets is empty	RO	0
0x2D	UART_RX	4	crc_ok_rx status - indicates that the last received uart packet had good CRC	RO	0
0x2D	UART_RX	5	lr_off_lane_1 indicate that the lane index of last received LR off message was 1.	RO	0
0x2D	UART_RX	7:6	lsrx_sel 00:ls_g1, 01:ls_g2, 10:ls_g3, 11:pwr_ctrl	R/W	1
0x2D	UART_RX	15:8	urx_fifo_data_out carry the received data from uart receive fifo	RO	0
0x2D	UART_RX	16	read_rx_pkt Writing "1" to this bit will implement a byte read from uart receive fifo	R/W SC	0
0x2D	UART_RX	17	start_crc_rx Writing "1" to this bit will initialize crc machine to 16'hFFFF	R/W SC	0
0x2D	UART_RX	18	crc_byte_valid_rx Writing "1" to this bit will cause the crc machine to calculate crc on the byte carried on urx_fifo_data_out	R/W SC	0

Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x2D	UART_RX	19	check_crc_rx Writing "1" to this bit will reflect the crc ok indication from crc machine to crc_ok_rx bit	R/W SC	0
0x2D	UART_RX	23:20	rx_lt_index_head indicates the head address of the received lt packets fifo	RO	0
0x2D	UART_RX	31:24	rx_packet_index_head indicate the head address of the receive packets fifo.	RO	0
0x2E	UART_TX	0	uart_during_tx indicate that uart is during tx, controller need to poll this bit till is 0 - before sending a byte on lstx	RO	0
0x2E	UART_TX	1	transmit_tx_byte when this bit is written to 1 - it cause the uart tx machine sending the uart_tx_data on lstx.	R/W SC	0
0x2E	UART_TX	2	start_crc_tx when this bit starts CRC machine on following tx packet	R/W SC	0
0x2E	UART_TX	3	crc_byte_valid_tx when this bit is written to 1 - the CRC byte from tx CRC machine is sent on lstx.	R/W SC	0
0x2E	UART_TX	7:4	Reserved	RO	0
0x2E	UART_TX	15:8	uart_tx_data carry the byte content to be sent through lstx.	R/W	0
0x2E	UART_TX	31:16	crc_tx carry the value of tx CRC machine	RO	0
0x2F	UART_ERR_CNT	11:0	uart_rcv_err_cnt carry the amount of uart packet that were received with errors.	WClr	0
0x2F	UART_ERR_CNT	23:12	uart_rcv_byte_cnt carry the ammount byte that were received through lsrx	WClr	0
0x2F	UART_ERR_CNT	31:24	uart_crc_err_cnt carry the ammount byte that were received through lsrx	WClr	0
0x2F	UART_ERR_CNT	19:0	gpio_change sticky bit per each GPIO pin, it is asserted upon a GPIO pin change. bits 19:16 refer to PCIE_RST_N_n	CBW1	0

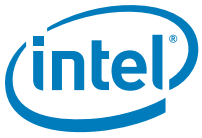


Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x2F	UART_ERR_CNT	31:20	reserved	RO	0
0x30	GPIO_CHANGE	19:0	gpio_change sticky bit per each GPIO pin, it is asserted upon a GPIO pin change. bits 19:16 refer to DDC_GPIOs	R/W	0
0x30	GPIO_CHANGE	31:20	Reserved	RO	0
0x31	GPIO_CHANGE_MASK	19:0	gpio_change_mask mask bit per each GPIO pin, if asserted it disable generating an interrupt when the GPIO pin changes. bits 19:16 refer to DDC_GPIOs	R/W	0
0x31	GPIO_CHANGE_MASK	31:20	Reserved	RO	0
0x32	GPIO_OWNERSHIP	19:0	gpio_ownership bit per each GPIO pin, indicate the controller own this GPIO pin. bits 19:16 refer to DDC_GPIOs	RO	0
0x32	GPIO_OWNERSHIP	31:20	Reserved	RO	0
0x33	GPIO_DATA_IN	19:0	gpio_data_in bit per each GPIO pin, indicate the value of GPIO pin. bits 19:16 refer to DDC_GPIOs	RO	0
0x33	GPIO_DATA_IN	31:20	reserved	RO	0
0x34	GPIO_DATA_OUT	19:0	gpio_data_out bit per each GPIO pin, carry the value for GPIO pin, when it is an output and owned by the controller.	R/W	0
0x34	GPIO_DATA_OUT	31:20	reserved	RO	0
0x35	GPIO_DATA_OE	19:0	gpio_data_output_enable bit per each GPIO pin, set direction of GPIO pin - when 1, pin is an output pin.	R/W	0
0x35	GPIO_DATA_OE	31:20	reserved	RO	0
0x36	GPIO_INVERT	19:0	gpio_invert_polarity when written to 1 - it will invert the data out polarity.	R/W	0
0x36	GPIO_INVERT	31:20	reserved	RO	0

Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x37	ICR	31:0	clc_reg_icr controller's interrupt cause register	RO	0
0x38	ICC	31:0	clc_reg_icc controller's interrupt clear register writing 1 to a bit in this register will clear the identical bit in clc_reg_icr register	R/W SC	0
0x39	ICS	31:0	clc_reg_ics soft interrupt register writing 1 to a bit in this register will set the identical bit in clc_reg_icr register	R/W SC	0
0x3A	IMR	31:0	clc_reg_imr mask interrupt register each bit in this register enable the identical bit ICS and ICR registers	R/W	0
0x3B	EE_CTRL	23:0	clc_ee_rd_addr carry the read address for reading EPROM through EPROM arbitrer	R/W	0
0x3B	EE_CTRL	24	ee_clc_dvalid status - indicate that the data is valid from last read access to EPROM	RO	0
0x3B	EE_CTRL	30:25	reserved	RO	0
0x3B	EE_CTRL	31	clc_ee_rd writing 1 to this bit will apply the read access to EPROM arbiter	R/W SC	0
0x3C	EE_DATA	31:0	ee_data carry the data read from EPROM in the last read access	RO	0
0x3D	IP_CMD (DFT)	0	ip_vld indicates that the memory read or write command is valid	R/W SC	0
0x3D	IP_CMD (DFT)	1	ip_wr1_rd0 0 - command is read 1 - command is write	R/W SC	0
0x3D	IP_CMD (DFT)	31:2	Reserved	RO	0
0x3E	IP_ADDR (DFT)	15:0	ip_addr carry the memory address for read or write command	R/W	0
0x3E	IP_ADDR (DFT)	31:16	Reserved	RO	0

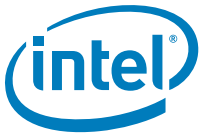


Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x3F	IP_WDATA (DFT)	31:0	ip_wdata carry the write data for memory write command	R/W	0
0x40	IP_RDATA (DFT)	31:0	ip_rdata carry the data read from last memory read command	RO	0
0x41	IP_PATCH_CTRL	0	clc_8051_sw_reset writing 1 to this bit will apply soft reset to the controller	R/W	0
0x41	IP_PATCH_CTRL	1	ucode_done_cb for debug - if set 1 will apply ucode done indication to hw.	R/W	0
0x41	IP_PATCH_CTRL	31:2	Reserved	RO	0
0x42	DEB_0	15:0	deb_addr_0 this field specifies the controller address value that cause an interrupt when accessed by the controller for write or read or code fetch.	R/W	0
0x42	DEB_0	16	follow_wr_0 When set to 1 will cause an interrupt to the link controller when value of deb_addr_0 is accessed for writing data by the controller	R/W	0
0x42	DEB_0	17	follow_rd_0 When set to 1 will cause an interrupt to the link controller when value of deb_addr_0 is accessed for reading data by the controller	R/W	0
0x42	DEB_0	18	follow_fetch_0 When set to 1 will cause an interrupt to the link controller when value of deb_addr_0 is accessed for fetching code by the controller. . data	R/W	0
0x42	DEB_0	23:19	Reserved	RO	0
0x42	DEB_0	24	wr_event_cought_0 indicates that the address indeb_addr_0 was accessed by controller. for writing data	RO	0
0x42	DEB_0	25	rd_event_cought_0 indicates that the address in deb_addr_0 was accessed by controller. for reading data.	RO	0

Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x42	DEB_0	26	fetch_event_cought_0 indicates that the address in deb_addr_0 was accessed by controller for fetching code.	RO	0
0x42	DEB_0	31:27	Reserved	RO	0
0x43	DEB_1	15:0	deb_addr_1 this field specifies the controller address value that cause an interrupt when accessed by the controller for write or read or code fetch.	R/W	0
0x43	DEB_1	16	follow_wr_1 When set to 1 will cause an interrupt to the link controller when value of deb_addr_11 is accessed for writing data by the controller	R/W	0
0x43	DEB_1	17	follow_rd_1 When set to 1 will cause an interrupt to the link controller when value of deb_addr_1 is accessed for reading data by the controller	R/W	0
0x43	DEB_1	18	follow_fetch_1 When set to 1 will cause an interrupt to the link controller when value of deb_addr_1 is accessed for fetching code by the controller. . data	R/W	0
0x43	DEB_1	23:19	Reserved	RO	0
0x43	DEB_1	24	wr_event_cought_1 indicates that the address indeb_addr_1 was accessed by controller. for writing data	RO	0
0x43	DEB_1	25	rd_event_cought_1 indicates that the address in deb_addr_1 was accessed by controller. for reading data.	RO	0
0x43	DEB_1	26	fetch_event_cought_1 indicates that the address in deb_addr_1 was accessed by controller for fetching code.	RO	0
0x43	DEB_1	31:27	reserved	RO	0

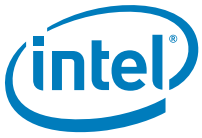


Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x44	DEB_2	15:0	locked_mem_addr carries the controller address (free running)	RO	0
0x44	DEB_2	31:16	reserved	RO	0
0x45	POWER_REQ_CTRL_TO_PARTNER	7:0	domain_power_up_request	R/W	0
0x45	POWER_REQ_CTRL_TO_PARTNER	15:8	domain_power_up_requested	R/W	0
0x45	POWER_REQ_CTRL_TO_PARTNER	23:16	domain_power_is_up	R/W	0
0x45	POWER_REQ_CTRL_TO_PARTNER	31:24	reserved	R/W	0
0x46	POWER_REQ_CTRL_FROM_PARTNER	31:0	domains_power_req_ctrl_from_partner	RO	0
0x47	EE_FORCE_POWER_DOMAIN	0	ee_force_dp_hdmi_power_on (read from EEPROM)**HDP In/Out bypass mode** HDP IN -> OUT HDMI bypass enable	RO	0
0x47	EE_FORCE_POWER_DOMAIN	1	ee_force_pcie_power_on (read from EEPROM)	RO	0
0x47	EE_FORCE_POWER_DOMAIN	2	ee_force_usb_xhci_power_on (read from EEPROM)	RO	0
0x47	EE_FORCE_POWER_DOMAIN	3	ee_force_cio_power_on (read from EEPROM)	RO	0
0x47	EE_FORCE_POWER_DOMAIN	4	ee_force_ana_comm_power_on (read from EEPROM)	RO	0
0x47	EE_FORCE_POWER_DOMAIN	5	ee_force_lc_power_on (read from EEPROM)	RO	0
0x47	EE_FORCE_POWER_DOMAIN	31:6	reserved	RO	0

Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x48	LINK_PADS_CTRL	1:0	ls_g1_out_sel select what will be the functionality of ls_g1 when act as output (00:uart1, 01:uart2, 10:ddc, 11: register)	R/W	0
0x48	LINK_PADS_CTRL	3:2	ls_g2_out_sel select what will be the functionality of ls_g2 when act as output (00:uart1, 01:uart2, 10:ddc, 11: register)	R/W	11
0x48	LINK_PADS_CTRL	5:4	ls_g3_out_sel select what will be the functionality of ls_g3 when act as output (00:uart1, 01:uart2, 10:ddc, 11: register)	R/W	11
0x48	LINK_PADS_CTRL	7:6	pwr_ctrl_out_sel select what will be the functionality of pwr_ctrl when act as output (00:uart1, 01:uart2, 10:ddc, 11: register)	R/W	11
0x48	LINK_PADS_CTRL	9:8	clc_hpd_sel (00:g1, 01:g2, 10:g3, 11:pwr_ctrl)	R/W	10
0x48	LINK_PADS_CTRL	11:10	clc_ddc_clk_sel	R/W	0
0x48	LINK_PADS_CTRL	13:12	clc_ddc_data_sel	R/W	0
0x48	LINK_PADS_CTRL	15:14	reserved	R/W	0
0x48	LINK_PADS_CTRL	17:16	ls_g1_selected_pulse_sel (Cotrol of debounce time. 2'b00->10us, 2'b01->1ms, 2'b10->10ms, 2'b11->100ms.)	R/W	0
0x48	LINK_PADS_CTRL	19:18	ls_g2_selected_pulse_sel (Cotrol of debounce time. 2'b00->10us, 2'b01->1ms, 2'b10->10ms, 2'b11->100ms.)	R/W	0
0x48	LINK_PADS_CTRL	21:20	ls_g3_selected_pulse_sel (Cotrol of debounce time. 2'b00->10us, 2'b01->1ms, 2'b10->10ms, 2'b11->100ms.)	R/W	0
0x48	LINK_PADS_CTRL	23:22	pwr_ctrl_selected_pulse_sel (Cotrol of debounce time. 2'b00->10us, 2'b01->1ms, 2'b10->10ms, 2'b11->100ms.)	R/W	0
0x48	LINK_PADS_CTRL	25:24	src0_hpd_selected_pulse_sel (Cotrol of debounce time. 2'b00->10us, 2'b01->1ms, 2'b10->10ms, 2'b11->100ms.)	R/W	0

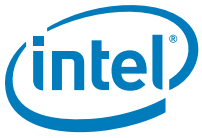


Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x48	LINK_PADS_CTRL	27:26	src0_cfg1_selected_pulse_sel (Cotrol of debounce time. 2'b00->10us, 2'b01->1ms, 2'b10->10ms, 2'b11->100ms.)	R/W	0
0x48	LINK_PADS_CTRL	31:28	reserved	R/W	0
0x49	LC_PHY_MAILBOX	30:0	lc_phy_mailbox	R/W	0
0x49	LC_PHY_MAILBOX	31	lc_phy_mailbox_valid	R/W SC	0
0x4A	PHY_LC_MAILBOX	31:0	phy_lc_mailbox	RO	0
0x4B	CHICKEN_BITS_2	1:0	reserved	R/W	0
0x4B	CHICKEN_BITS_2	2	dft_ignore_ls_for_connect	R/W	0
0x4B	CHICKEN_BITS_2	3	dft_skip_cp_powerdown_ack	R/W	0
0x4B	CHICKEN_BITS_2	4	reverse_connector_direction	R/W	0
0x4B	CHICKEN_BITS_2	5	dft_dp_multi_function_connected	R/W	0
0x4B	CHICKEN_BITS_2	6	dft_usb_cable_usb3_mode	R/W	0
0x4B	CHICKEN_BITS_2	7	dft_dpp_cable_hdmi_mode**HDP In/Out bypass mode** HDP IN -> OUT HDMI bypass enable	R/W	0
0x4B	CHICKEN_BITS_2	8	dft_cable_swapped	R/W	0
0x4B	CHICKEN_BITS_2	9	dft_tbt_cable_connected	R/W	0
0x4B	CHICKEN_BITS_2	10	dft_dp_cable_connected	R/W	0
0x4B	CHICKEN_BITS_2	11	dft_usb_cable_connected	R/W	0
0x4B	CHICKEN_BITS_2	12	dft_tbt_cable_tbt3	R/W	0
0x4B	CHICKEN_BITS_2	13	dft_tbt_passive_cable	R/W	0

Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x4B	CHICKEN_BITS_2	14	Reserved	R/W	0
0x4B	CHICKEN_BITS_2	15	dft_passive_cable_20g	R/W	0
0x4B	CHICKEN_BITS_2	16	init_no_stall_ack_wait (disable (possibly) waiting forever on stall_ee_ack & stall_tar_ack when powering on domains)	R/W	0
0x4B	CHICKEN_BITS_2	17	init_no_ramp_done_0p9_wait disable (possibly) waiting forever on ramp_done when powering on domains	R/W	0
0x4B	CHICKEN_BITS_2	18	init_no_ramp_done_3p3_wait disable (possibly) waiting forever on ramp_done when powering on domains	R/W	0
0x4B	CHICKEN_BITS_2	19	init_no_flash_wait (disable waits on flash load operations)	R/W	0
0x4B	CHICKEN_BITS_2	20	init_no_svr_calibrated_wait (disable wait on svr calibration)	R/W	0
0x4B	CHICKEN_BITS_2	21	init_no_osc_calibration_wait (skip osc calibration)	R/W	0
0x4B	CHICKEN_BITS_2	22	init_no_scratch_program_wait (skip wait for scratch program done)	R/W	0
0x4B	CHICKEN_BITS_2	23	init_no_xtal_stable_wait	R/W	0
0x4B	CHICKEN_BITS_2	24	Reserved	R/W	0
0x4B	CHICKEN_BITS_2	25	keep_pcie_powered (for host w/ pass-through PCIe devices)	R/W	0
0x4B	CHICKEN_BITS_2	26	Reserved	R/W	0
0x4B	CHICKEN_BITS_2	27	src0_use_only_snk0.	R/W	0
0x4B	CHICKEN_BITS_2	28	src0_force_cm_snk0_disconnect. when set, LC will force disconnect of CM snk0 ownership (depending on bit 31)	R/W	0
0x4B	CHICKEN_BITS_2	29	Reserved	R/W	0

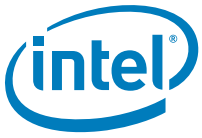


Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x4B	CHICKEN_BITS_2	30	src0_hdmi_only. src0 will force HDMI mode regardless of cfg1 state. For use in HDMI only systems**HDP In/Out bypass mode** HDP IN -> OUT HDMI bypass enable	R/W	0
0x4B	CHICKEN_BITS_2	31	src0_do_not_wait_for_free_sink. when set to 1, src0 will request snk0 owner to release it even if snk1 is also in use. When 0, src0 will only request snk0 release if snk1 is free	R/W	0
0x4C	POC_CSR_COMMON_IN	31:0	poc_lc_csr_common	RO	0
0x4D	POC_CSR_COMMON_OUT	31:0	lc_poc_csr_common	R/W	0
0x4E	UART_2_HW_CTRL	0	block_uart_2_tx (block all UART transactions. Serial lstx is OR'd with this bit)	R/W	1
0x4E	UART_2_HW_CTRL	1	block_uart_2_rx (Block UART RX packets. lsrx is OR'd with this bit)	R/W	1
0x4E	UART_2_HW_CTRL	2	block_hw_tx_2_ls (Block UART LT packets generated by HW from LSEO changes)	R/W	1
0x4E	UART_2_HW_CTRL	3	fw_lstx_2_oen	R/W	1
0x4E	UART_2_HW_CTRL	4	fw_lstx_2_o	R/W	0
0x4E	UART_2_HW_CTRL	5	hw_sent_lt_packet (not in use in Uart_2)	R/W	0
0x4E	UART_2_HW_CTRL	6	en_hw_rx_2_fsm (enable uart rx fsm. It will write the AT packets to the external RAM.)	R/W	0
0x4E	UART_2_HW_CTRL	7	reserved	RO	0
0x4E	UART_2_HW_CTRL	8	sw_rst_tx_2 (HW Will create a synchronous reset pulse to UART TX SM)	R/W SC	0
0x4E	UART_2_HW_CTRL	9	sw_rst_rx_2 (HW Will create a synchronous reset pulse to UART RX SM)	R/W SC	0
0x4E	UART_2_HW_CTRL	31:10	reserved	RO	0

Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x4F	UART_2_RX	0	uart_2_during_rx	RO	0
0x4F	UART_2_RX	1	rx_2_pkt_has_err	R/W	0
0x4F	UART_2_RX	2	urx_2_fifo_full	RO	0
0x4F	UART_2_RX	3	urx_2_fifo_empty	RO	0
0x4F	UART_2_RX	4	crc_ok_rx_2 (indicates if crc was 16'h0000 on check_crc rise)	RO	0
0x4F	UART_2_RX	5	lr_off_labe_1_2 (Indicate lane num in last lr_off LT packet)	RO	0
0x4F	UART_2_RX	7:6	lsrx_sel	R/W	1
0x4F	UART_2_RX	15:8	urx_2_fifo_data_out (RX data Byte from UART fifo)	RO	0
0x4F	UART_2_RX	16	read_rx_2_pkt Writing "1" to this bit will implement a byte read from uart receive fifo	R/W SC	0
0x4F	UART_2_RX	17	start_crc_rx_2 Writing "1" to this bit will initialize crc machine to 16'hFFFF	R/W SC	0
0x4F	UART_2_RX	18	crc_byte_valid_rx_2 Writing "1" to this bit will cuase the crc machine to claculate crc on the byte carried on urx_fifo_data_out	R/W SC	0
0x4F	UART_2_RX	19	check_crc_rx_2 Writing "1" to this bit will reflect the crc ok indication from crc machine to crc_ok_rx bit	R/W SC	0
0x4F	UART_2_RX	23:20	reserved	RO	0
0x4F	UART_2_RX	31:24	rx_2_packet_index_head	RO	0
0x50	UART_2_TX	0	uart_during_tx_2 UART sending a TX packet	RO	0
0x50	UART_2_TX	1	transmit_tx_2_byte UART sending a TX packet	R/W SC	0
0x50	UART_2_TX	2	start_crc_tx_2	R/W SC	0
0x50	UART_2_TX	3	crc_byte_valid_tx_2	R/W SC	0

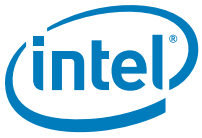


Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x50	UART_2_TX	7:4	reserved	RO	0
0x50	UART_2_TX	15:8	uart_tx_2_data TX data dwto UART fifo	R/W	0
0x50	UART_2_TX	31:16	crc_tx_2	RO	0
0x51	UART_2_ERR_CNT	11:0	uart_2_rcv_err_cnt Number of UART ERROR bytes received	R/W SV	0
0x51	UART_2_ERR_CNT	23:12	uart_2_rcv_byte_cnt Number of UART bytes received	R/W SV	0
0x51	UART_2_ERR_CNT	31:24	uart_2_crc_err_cnt Number of UART AT packets with CRC errors	R/W SV	0
0x52	LC_POC_USB2_CTRL	7:0	lc_poc_usb_osc_1m_calib [6:0] - calibration bits. [7] valid bit	R/W	40
0x52	LC_POC_USB2_CTRL	8	lc_poc_switch_en_on	R/W	0
0x52	LC_POC_USB2_CTRL	9	lc_poc_switch_en_off	R/W	0
0x52	LC_POC_USB2_CTRL	10	lc_poc_fw_force_on_en	R/W	0
0x52	LC_POC_USB2_CTRL	11	lc_poc_ramp_done	R/W	0
0x52	LC_POC_USB2_CTRL	12	lc_poc_bleeder_en_usb_sx	R/W	0
0x52	LC_POC_USB2_CTRL	15:13	lc_poc_slope_control	R/W	4
0x52	LC_POC_USB2_CTRL	23:16	poc_lc_usb_osc_1m_calib	RO	40
0x52	LC_POC_USB2_CTRL	24	poc_lc_switch_en_on	RO	0
0x52	LC_POC_USB2_CTRL	25	poc_lc_switch_en_off	RO	0
0x52	LC_POC_USB2_CTRL	26	poc_lc_fw_force_on_en	RO	0
0x52	LC_POC_USB2_CTRL	27	poc_lc_ramp_done	RO	0
0x52	LC_POC_USB2_CTRL	28	poc_lc_bleeder_en_usb_sx	RO	0

Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x52	LC_POC_USB 2_CTRL	31:29	poc_lc_slope_control	RO	4
0x53	FW_COUNTE R_1	7:0	1us_counter	R/W	0
0x53	FW_COUNTE R_1	15:8	10us_counter	R/W	0
0x53	FW_COUNTE R_1	23:16	100us_counter	R/W	0
0x53	FW_COUNTE R_1	31:24	1ms_counter	R/W	0
0x54	FW_COUNTE R_2	7:0	1ms_counter_second	R/W	0
0x54	FW_COUNTE R_2	15:8	1ms_counter_third	R/W	0
0x54	FW_COUNTE R_2	23:16	1ms_counter_fourth	R/W	0
0x54	FW_COUNTE R_2	31:24	1ms_counter_fifth	R/W	0
0x55	FW_COUNTE R_3	7:0	10ms_counter	R/W	0
0x55	FW_COUNTE R_3	15:8	10ms_counter_second	R/W	0
0x55	FW_COUNTE R_3	23:16	10ms_counter_third	R/W	0
0x55	FW_COUNTE R_3	31:24	10ms_counter_fourth	R/W	0
0x56	FW_COUNTE R_4	7:0	10ms_counter_fifth	R/W	0
0x56	FW_COUNTE R_4	15:8	10ms_counter_sixth	R/W	0
0x56	FW_COUNTE R_4	23:16	100ms_counter	R/W	0
0x56	FW_COUNTE R_4	31:24	100ms_counter_second	R/W	0
0x57	FW_COUNTE R_5	7:0	100ms_counter_third	R/W	0
0x57	FW_COUNTE R_5	15:8	100ms_counter_fourth	R/W	0

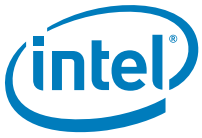


Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x57	FW_COUNTER_5	23:16	1s_counter	R/W	0
0x57	FW_COUNTER_5	31:24	1s_counter_second	R/W	0
0x58	PHY_RX_TX_EN_REG	0	fw_en_rx_null_l0	R/W	0
0x58	PHY_RX_TX_EN_REG	1	fw_en_rx_null_l1	R/W	0
0x58	PHY_RX_TX_EN_REG	2	fw_en_tx_null_l0	R/W	0
0x58	PHY_RX_TX_EN_REG	3	fw_en_tx_null_l1	R/W	0
0x58	PHY_RX_TX_EN_REG	4	fw_en_rx_phy_l0	R/W	0
0x58	PHY_RX_TX_EN_REG	5	fw_en_rx_phy_l1	R/W	0
0x58	PHY_RX_TX_EN_REG	6	fw_en_tx_phy_l0	R/W	0
0x58	PHY_RX_TX_EN_REG	7	fw_en_tx_phy_l1	R/W	0
0x58	PHY_RX_TX_EN_REG	15:8	delay_legacy_rx_en	R/W	128
0x58	PHY_RX_TX_EN_REG	16	hw_en_rx_null_l0_status	RO	0
0x58	PHY_RX_TX_EN_REG	17	hw_en_rx_null_l1_status	RO	0
0x58	PHY_RX_TX_EN_REG	18	hw_en_tx_null_l0_status	RO	0
0x58	PHY_RX_TX_EN_REG	19	hw_en_tx_null_l1_status	RO	0
0x58	PHY_RX_TX_EN_REG	20	hw_en_rx_phy_l0_status	RO	0
0x58	PHY_RX_TX_EN_REG	21	hw_en_rx_phy_l1_status	RO	0
0x58	PHY_RX_TX_EN_REG	22	hw_en_tx_phy_l0_status	RO	0
0x58	PHY_RX_TX_EN_REG	23	hw_en_tx_phy_l1_status	RO	0

Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x58	PHY_RX_TX_EN_REG	30:24	reserved	R/W	0
0x58	PHY_RX_TX_EN_REG	31	disable_delay_legacy_rx	R/W	0
0x59	LC_NULL_CTRL	1:0	target_link_width (lane0)	R/W	0
0x59	LC_NULL_CTRL	3:2	target_link_speed (lane0)	R/W	0
0x59	LC_NULL_CTRL	4	link disable (lane0)	R/W	0
0x59	LC_NULL_CTRL	5	link retrain (lane0)	R/W	0
0x59	LC_NULL_CTRL	7:6	reserved	R/W	0
0x59	LC_NULL_CTRL	9:8	target_link_width (lane1)	R/W	0
0x59	LC_NULL_CTRL	11:10	target_link_speed (lane1)	R/W	0
0x59	LC_NULL_CTRL	12	link disable (lane1)	R/W	0
0x59	LC_NULL_CTRL	13	link retrain (lane1)	R/W	0
0x59	LC_NULL_CTRL	30:14	reserved	R/W	0
0x59	LC_NULL_CTRL	31	lc_cio_en_rs	R/W	0
0x5A	SUSPEND_RESUME_CTRL	0	lc_usb_controls_valid	R/W	0
0x5A	SUSPEND_RESUME_CTRL	1	lc_usb_cable_connected	R/W	0
0x5A	SUSPEND_RESUME_CTRL	2	lc_usb_overcurrent_indication	R/W	0
0x5A	SUSPEND_RESUME_CTRL	3	reserved	R/W	0
0x5A	SUSPEND_RESUME_CTRL	4	lc_usb_power_good_ack	R/W	0
0x5A	SUSPEND_RESUME_CTRL	5	lc_usb_force_pgcb_power_up_request	R/W	0

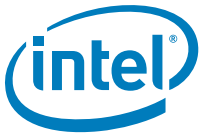


Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x5A	SUSPEND_RESUME_CTRL	6	lc_usb_force_pgcb_power_down_request	R/W	0
0x5A	SUSPEND_RESUME_CTRL	7	lc_usb_force_reset	R/W	0
0x5A	SUSPEND_RESUME_CTRL	8	usb_lc_controls_used	RO	0
0x5A	SUSPEND_RESUME_CTRL	9	usb_lc_power_good_request	RO	0
0x5A	SUSPEND_RESUME_CTRL	15:10	reserved	R/W	0
0x5A	SUSPEND_RESUME_CTRL	16	lc_cio_tx_pll_enable	R/W	0
0x5A	SUSPEND_RESUME_CTRL	17	lc_cio_prepare_to_sleep	R/W	0
0x5A	SUSPEND_RESUME_CTRL	18	lc_cio_resume	R/W	0
0x5A	SUSPEND_RESUME_CTRL	23:19	reserved	R/W	0
0x5A	SUSPEND_RESUME_CTRL	24	phy_port_init_done	RO	0
0x5A	SUSPEND_RESUME_CTRL	25	phy_dp_port_init_done	RO	0
0x5A	SUSPEND_RESUME_CTRL	26	cio_usb_pll_clk_stable	RO	0
0x5A	SUSPEND_RESUME_CTRL	27	phy_to_lc_sleep_ready	RO	0
0x5A	SUSPEND_RESUME_CTRL	31:28	reserved	R/W	0
0x5B	reserved	31:0	reserved	RO	0
0x5C	OSC_CALIBRATION_ADDR	0	pll_cal_inc_decn	R/W	0
0x5C	OSC_CALIBRATION_ADDR	14:1	pll_cal_measure_cyc	R/W	2048
0x5C	OSC_CALIBRATION_ADDR	31:15	pll_cal_target_cyc	R/W	8192

Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x5D	OSC_CALIBRATION_ADDR_2	0	clc_pll_cal_enable	R/W	0
0x5D	OSC_CALIBRATION_ADDR_2	1	pll_cal_done	RO	0
0x5D	OSC_CALIBRATION_ADDR_2	2	pll_cal_usb_osc_select	R/W	0
0x5D	OSC_CALIBRATION_ADDR_2	5:3	reserved	R/W	0
0x5D	OSC_CALIBRATION_ADDR_2	23:6	pll_cal_output_count	RO	0
0x5D	OSC_CALIBRATION_ADDR_2	31:24	pll_cal_calib_ctrl	RO	0
0x5E	POWER_SWITCH_SEL	3:0	switch_sel_0p9 bit 0: dp, 1: pcie, 2: usb_xhci, 3: cio	R/W	0
0x5E	POWER_SWITCH_SEL	7:4	reserved	RO	0
0x5E	POWER_SWITCH_SEL	10:8	switch_sel_3p3 bit 8: dp, 9: pcie, 10: usb_xhci	R/W	0
0x5E	POWER_SWITCH_SEL	11	reserved	RO	0
0x5E	POWER_SWITCH_SEL	12	switch_sel_3p3 12:ana_cio	R/W	0
0x5E	POWER_SWITCH_SEL	15:13	reserved	RO	0
0x5E	POWER_SWITCH_SEL	19:16	switch_sel_0p9	RO	0
0x5E	POWER_SWITCH_SEL	23:20	reserved	RO	0
0x5E	POWER_SWITCH_SEL	26:24	switch_sel_3p3	RO	0
0x5E	POWER_SWITCH_SEL	27	reserved	RO	0

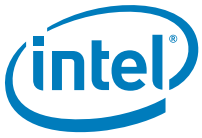


Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x5E	POWER_SWITCH_SEL	28	switch_sel_3p3	RO	0
0x5E	POWER_SWITCH_SEL	31:29	reserved	RO	0
0x5F	POWER_CTRL	2:0	slope_control_0p9 bits that control the 0p9 switch slope (default 100)	R/W	4
0x5F	POWER_CTRL	3	reserved	RO	0
0x5F	POWER_CTRL	6:4	slope_control_3p3 bits that control the 3p3 switch slope (default 100)	R/W	4
0x5F	POWER_CTRL	7	reserved	RO	0
0x5F	POWER_CTRL	8	slope_enable_on_0p9 enables to power on in the 0_9 switch the domains that are set in the switch_sel_0p9	R/W	0
0x5F	POWER_CTRL	9	slope_enable_on_3p3 enables to power on in the 3_3 switch the domains that are set in the switch_sel_3p3	R/W	0
0x5F	POWER_CTRL	10	slope_enable_off_0p9 enables to power off in the 0_9 switch the domains that are set in the switch_sel_0p9	R/W	0
0x5F	POWER_CTRL	11	slope_enable_off_3p3 enables to power off in the 3_3 switch the domains that are set in the switch_sel_3p3	R/W	0
0x5F	POWER_CTRL	12	ramp_done_0p9 indicates that the 0_9 switch finished powering on/off	RO	0
0x5F	POWER_CTRL	13	ramp_done_3p3 indicates that the 3_3 switch finished powering on/off	RO	0
0x5F	POWER_CTRL	14	fw_force_on_en_0p9	R/W	0
0x5F	POWER_CTRL	15	fw_force_on_en_3p3	R/W	0
0x5F	POWER_CTRL	16	svr_en	R/W	0
0x5F	POWER_CTRL	17	svr_calibrated	RO	0
0x5F	POWER_CTRL	18	enable_s0_switches	R/W	0

Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x5F	POWER_CTRL	31:19	reserved	R/W	0
0x60	FLASH_CTRL	15:0	lc_flash_ctrl_rd_request_mask	R/W	0
0x60	FLASH_CTRL	16	lc_flash_ctrl_rd_request	R/W	0
0x60	FLASH_CTRL	17	flsh_erase_req1_ack0	R/W SC	0
0x60	FLASH_CTRL	18	flsh_program_req1_ack0	R/W SC	0
0x60	FLASH_CTRL	19	flsh_cm_generic_access	RO	0
0x60	FLASH_CTRL	31:20	reserved	R/W	0
0x61	POWER_UP_INDICATIONS	4:0	power_is_active indicates that the power is active at the domain (matches the EE_FORCE_POWER_DOMAIN bits)	R/W	0
0x61	POWER_UP_INDICATIONS	7:5	reserved	RO	0
0x61	POWER_UP_INDICATIONS	8	stall_tar_accesses_req	R/W	0
0x61	POWER_UP_INDICATIONS	9	stall_ee_accesses_req	R/W	0
0x61	POWER_UP_INDICATIONS	10	stall_tar_ack	RO	0
0x61	POWER_UP_INDICATIONS	11	stall_ee_ack	RO	0
0x61	POWER_UP_INDICATIONS	15:12	reserved	RO	0
0x61	POWER_UP_INDICATIONS	16	car_comm_cio_ana_ucode_clk_is_valid	RO	0
0x61	POWER_UP_INDICATIONS	17	car_comm_dp_ucode_clk_is_valid	RO	0
0x61	POWER_UP_INDICATIONS	18	car_comm_arc_cp_ucode_clk_is_valid	RO	0
0x61	POWER_UP_INDICATIONS	23:19	reserved	RO	0
0x61	POWER_UP_INDICATIONS	24	xhc_EMEP_DLIsActive (from PCIE)	RO	0

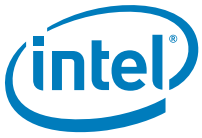


Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x61	POWER_UP_INDICATIONS	31:25	reserved	RO	0
0x62	HVREQ	6:0	ee_clc_port_reg_max_wats IECS (addr 10) HVREQ register [6:0]	R/W	0
0x62	HVREQ	7	hvreq IECS (addr 10) HVREQ register [7]	R/W	0
0x62	HVREQ	31:8	reserved	R/W	0
0x63	MSG_OUT_CTRL	7:0	stx_byte carry the stx field value of outgoing AT message through uart	R/W	0
0x63	MSG_OUT_CTRL	15:8	reg_addr carry the register address field of outgoing AT packet	R/W	0
0x63	MSG_OUT_CTRL	22:16	length indicate the length field of the outgoing AT packet	R/W	0
0x63	MSG_OUT_CTRL	23	write1_read0 indicate if the access is read or write to remote register address	R/W	0
0x63	MSG_OUT_CTRL	24	transaction_invalid iecs transaction was invalid	R/W	0
0x63	MSG_OUT_CTRL	25	transaction_timeout iecs transaction did not complete within 100ms	R/W	0
0x63	MSG_OUT_CTRL	29:26	reserved	R/W	0
0x63	MSG_OUT_CTRL	30	at1_lt0 0 - indicate that the outgoing message is an LT packet 1 - indicate that the outgoing message is an AT packet	R/W	0
0x63	MSG_OUT_CTRL	31	msg_valid sw sets this bit to 1 to trigger an iecs transaction. LC will clear this bit once the transaction is done (whether successfully or not)	R/W	0
0x64	MSG_OUT_WDATA0	31:0	wdata0 carry the 1st double word write data of outgoing message out data field	R/W	0

Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x65	MSG_OUT_WDATA1	31:0	wdata1 carry the 2nd double word write data of outgoing message out data field	R/W	0
0x66	MSG_OUT_WDATA2	31:0	wdata2 carry the 3rd double word write data of outgoing message out data field	R/W	0
0x67	MSG_OUT_WDATA3	31:0	wdata3 carry the 4th double word write data of outgoing message out data field	R/W	0
0x68	MSG_OUT_WDATA4	31:0	wdata4 carry the 5th double word write data of outgoing message out data field	R/W	0
0x69	MSG_OUT_WDATA5	31:0	wdata5 carry the 6th double word write data of outgoing message out data field	R/W	0
0x6A	MSG_OUT_WDATA6	31:0	wdata6 carry the 7th double word write data of outgoing message out data field	R/W	0
0x6B	MSG_OUT_WDATA7	31:0	wdata7 carry the 8th double word write data of outgoing message out data field	R/W	0
0x6C	MSG_OUT_WDATA8	31:0	wdata8 carry the 9th double word write data of outgoing message out data field	R/W	0
0x6D	MSG_OUT_WDATA9	31:0	wdata9 carry the 10th double word write data of outgoing message out data field	R/W	0
0x6E	MSG_OUT_WDATA10	31:0	wdata10 carry the 11th double word write data of outgoing message out data field	R/W	0
0x6F	MSG_OUT_WDATA11	31:0	wdata11 carry the 12th double word write data of outgoing message out data field	R/W	0
0x70	MSG_OUT_WDATA12	31:0	wdata12 carry the 13th double word write data of outgoing message out data field	R/W	0
0x71	MSG_OUT_WDATA13	31:0	wdata13 carry the 14th double word write data of outgoing message out data field	R/W	0
0x72	MSG_OUT_WDATA14	31:0	wdata14 carry the 15thdouble word write data of outgoing message out data field	R/W	0

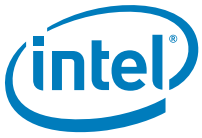


Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x73	MSG_OUT_WDATA15	31:0	wdata15 carry the 16th double word write data of outgoing message out data field	R/W	0
0x74	MSG_OUT_RDATA0	31:0	rdata0 carry the 1st double word read data of outgoing message out data field	R/W	0
0x75	MSG_OUT_RDATA1	31:0	rdata1 carry the 2nd double word read data of outgoing message out data field	R/W	0
0x76	MSG_OUT_RDATA2	31:0	rdata2 carry the 3rd double word read data of outgoing message out data field	R/W	0
0x77	MSG_OUT_RDATA3	31:0	rdata3 carry the 4th double word read data of outgoing message out data field	R/W	0
0x78	MSG_OUT_RDATA4	31:0	rdata4 carry the 5th double word read data of outgoing message out data field	R/W	0
0x79	MSG_OUT_RDATA5	31:0	rdata5 carry the 6th double word read data of outgoing message out data field	R/W	0
0x7A	MSG_OUT_RDATA6	31:0	rdata6 carry the 7th double word read data of outgoing message out data field	R/W	0
0x7B	MSG_OUT_RDATA7	31:0	rdata7 carry the 8th double word read data of outgoing message out data field	R/W	0
0x7C	MSG_OUT_RDATA8	31:0	rdata8 carry the 9th double word read data of outgoing message out data field	R/W	0
0x7D	MSG_OUT_RDATA9	31:0	rdata9 carry the 10th double word read data of outgoing message out data field	R/W	0
0x7E	MSG_OUT_RDATA10	31:0	rdata10 carry the 11th double word read data of outgoing message out data field	R/W	0
0x7F	MSG_OUT_RDATA11	31:0	rdata11 carry the 12th double word read data of outgoing message out data field	R/W	0
0x80	MSG_OUT_RDATA12	31:0	rdata12 carry the 13th double word read data of outgoing message out data field	R/W	0

Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x81	MSG_OUT_RDATA13	31:0	rdata13 carry the 14th double word read data of outgoing message out data field	R/W	0
0x81	MSG_OUT_RDATA14	31:0	rdata14 carry the 15thdouble word read data of outgoing message out data field	R/W	0
0x83	MSG_OUT_RDATA15	31:0	rdata15 carry the 16th double word read data of outgoing message out data field	R/W	0
0x84	SW_FW_MAILBOX_DATA_IN0	31:0	sw_fw_mailbox_data_in0 See Appendix A.4 for details	R/W	N/A
0x85	SW_FW_MAILBOX_DATA_IN1	31:0	sw_fw_mailbox_data_in1 See Appendix A.4 for details	R/W	N/A
0x86	SW_FW_MAILBOX_DATA_IN2	31:0	sw_fw_mailbox_data_in2 See Appendix A.4 for details	R/W	N/A
0x87	SW_FW_MAILBOX_DATA_IN3	31:0	sw_fw_mailbox_data_in3 See Appendix A.4 for details	R/W	N/A
0x88	SW_FW_MAILBOX_DATA_OUT0	31:0	sw_fw_mailbox_data_out0 See Appendix A.4 for details	R/W	N/A
0x89	SW_FW_MAILBOX_DATA_OUT1	31:0	sw_fw_mailbox_data_out1 See Appendix A.4 for details	R/W	N/A
0x8A	SW_FW_MAILBOX_DATA_OUT2	31:0	sw_fw_mailbox_data_out2 See Appendix A.4 for details	R/W	N/A
0x8B	SW_FW_MAILBOX_DATA_OUT3	31:0	sw_fw_mailbox_data_out3 See Appendix A.4 for details	R/W	N/A
0x8C	IECS_reserved_7	7:0	reserved	R/W	0
0x8C	IECS_reserved_7	31:8	Reserved	R/W	0
0x8D	IECS_12_ACTIVE_LANES	0	lane0_is_active when set, lane0 is active	R/W	0
0x8D	IECS_12_ACTIVE_LANES	1	Lane1_is_active when set, lane0 is active	R/W	0

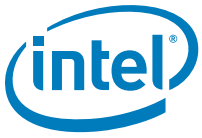


Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x8D	IECS_12_ACTIVE_LANES	7:2	Reserved	R/W	0
0x8D	IECS_12_ACTIVE_LANES	8	lane0_available when set, lane0 can be used	R/W	From FLASH
0x8D	IECS_12_ACTIVE_LANES	9	Lane1_available when set, lane1 can be used	R/W	From FLASH
0x8D	IECS_12_ACTIVE_LANES	11:10	Reserved	R/W	0
0x8D	IECS_12_ACTIVE_LANES	12	dual_lane_supported	R/W	0
0x8D	IECS_12_ACTIVE_LANES	13	link_20g_supported	R/W	0
0x8D	IECS_12_ACTIVE_LANES	31:14	Reserved	R/W	0
0x8E	IECS_TXFFE	31:0	txffe status IECS register	R/W	0
0x8F	reserved	31:0	reserved	R/W	0
0x90	IECS_reserved_14	31:0	reserved	R/W	0
0x91	reserved	31:0	reserved	R/W	
0x92	LC_CM_MAILBOX	31:0	mailbox for internal messaging between LC and CM	R/W	0
0x93	CM_LC_MAILBOX	31:0	mailbox for internal messaging between LC and CM	R/W	0
0x94	LC_SX_ENTRY_CTRL	0	go2sx_wake indicates LC is entering Sx with wake support	R/W	0
0x94	LC_SX_ENTRY_CTRL	1	go2sx_no_wake indicates LC is entering Sx without wake support		
0x94	LC_SX_ENTRY_CTRL	3:2	reserved		
0x94	LC_SX_ENTRY_CTRL	4	go2sx_from_pcie2tbt indicates LC sx entry was triggered by a pcie2tbt command		
0x94	LC_SX_ENTRY_CTRL	31:5	reserved		

Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x95	LC_SX_STATUS	19	exit_was_forced Indicates that the sx entry was aborted (using initial wake).	R/W	0
0x95	LC_SX_STATUS	22:20	exit_state Indicates the state before entering Sx. 1XX = cio (100 = downstream, 101 = upstream, 110 = interdomain), 010 =dpp, 000 = disconnected	R/W	0
0x95	LC_SX_STATUS	23	exit_power_up_state system state at power up (0=S0/1=Sx)	R/W	0
0x95	LC_SX_STATUS	27:24	reserved	R/W	0
0x95	LC_SX_STATUS	30:28	entering_sx_state Indicates the state for the current sx entry. 1XX = cio (100 = downstream, 101 = upstream, 110 = interdomain), 011 = DP multi-function, 010 = dpp, 001 = USB, 000 = disconnected	R/W	0
0x95	LC_SX_STATUS	31	entering_sx When set, LC is in the process of entering Sx	R/W	0
0x96	LC_SX_CTRL	10:0	sx_wake_events defines on which events to wake on in Sx mode. Bit mapping is as follows: 0x001 – wake on perst_n deassertion 0x002 – wake on cio connect 0x004 – wake on cio disconnect 0x008 – wake on DP connect 0x010 – wake on DP disconnect 0x020 – wake on TBT_wake 0x040 – wake on wake_n assertion 0x080 – wake on slp_s3# deassertion 0x100 – wake on force_pwr assertion 0x200 - wake on USB connect 0x400 - wake on USB disconnect SW is allowed to change the settings. LC will set it to default on initial wake.	R/W	Hosts: 0x180 Devices: 0x140
0x96	LC_SX_CTRL	15:11	reserved	R/W	0
0x96	LC_SX_CTRL	16	link_1_configured link of null port 1 (or 3) is plugged and configured. Updated by CM. Unless in Sx flow, should be cleared by LC after cio is powered down (when cp_power_down_ack is handled).	R/W	0

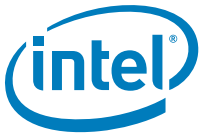


Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x96	LC_SX_CTRL	17	link_1_interdomain_configured link of null port 1 (or 3) is plugged and configured as an interdomain link (for future use). Updated by CM. Unless in Sx flow, should be cleared by LC after cio is powered down (when cp_power_down_ack is handled). [16] link_1_configured -link of null port 1	R/W	0
0x96	LC_SX_CTRL	19:18	reserved	R/W	0
0x96	LC_SX_CTRL	20	link_2_configured link of null port 2 (or 4) is plugged and configured. Updated by CM. Unless in Sx flow, should be cleared by LC after cio is powered down	R/W	0
0x96	LC_SX_CTRL	21	link_2_interdomain_configured link of null port 2 (or 4) is plugged and configured as an interdomain link (for future use). Updated by CM. Unless in Sx flow, should be cleared by LC after cio is powered down	R/W	0
0x96	LC_SX_CTRL	28:22	reserved	R/W	0
0x96	LC_SX_CTRL	29	cm_sx_exit for disconnected/interdomain ports exiting Sx, LC waits for this to be set before enabling high speed training	R/W	0
0x96	LC_SX_CTRL	30	port_is_upstream One of the lanes on this port is the upstream port	R/W	0
0x96	LC_SX_CTRL	31	CM_go2sx LC should start GO2SX flow once this bit is set. Updated by CM.	R/W	0
0x97	reserved	31:0	reserved	R/W	0
0x98	reserved	31:0	reserved	R/W	0
0x99	reserved	31:0	reserved	R/W	0
0x9A	LC_SX_TIMERS	7:0	sx_entry_timeout_seconds Defines the timeout duration for Sx entry, in seconds. Accuracy will be +/- 100ms. LC sets the default on every power up. SW can modify the value (must repeat before any Sx entry)	R/W	40

Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x9A	LC_SX_TIMERS	31:8	reserved	R/W	0
0x9B	LC_FLASH_ACCESS_DATA	31:0	data_r Carry the data that was read from Flash	R/W	0
0x9C	LC_FLASH_ACCESS_CTRL	23:0	byte_addr carry the byte address in the FLASH to access. Address must be dw aligned, so bits [1:0] must be set to 0	R/W	0
0x9C	LC_FLASH_ACCESS_CTRL	28:24	access_length when data_register_select is set, determines how many DWs should be read. It is SW responsibility to ensure the accessed flash supports the requested length	R/W	0
0x9C	LC_FLASH_ACCESS_CTRL	29	data_register_select selects where the read data should be taken from. Set 0 for using LC_FLASH_ACCESS_DATA. Set 1 for using MSG_OUT_RDATA	R/W	
0x9C	LC_FLASH_ACCESS_CTRL	30	Read_error Indicates that last read transaction ended with error		
0x9C	LC_FLASH_ACCESS_CTRL	31	Start1_done0 this bit should be set to 1 when starting transaction, cleared by controller for indicating the transaction is done.	R/W	0
0x9D	FW_STATE	7:0	fw_version carry the controller FW version	R/W	
0x9D	FW_STATE	15:8	can_be_upstream Used for upstream negotiation between LCs	R/W	

Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value

0x9D	FW_STATE	23:16	fw_sub_state:
			// tbt sub states
			TBT_IECS_LINK_ESTABLISH 0x34
			TBT_POWER_ON_CIO 0x35
			TBT_HIGH_SPEED 0x36
			TBT_WAIT_CIO_ON 0x37
			TBT_LT_SYNC 0x38
			TBT_TX_EN 0x39
			TBT_LINK_NEGOTIATE 0x3A
			// DP_MF sub states
			DP_MF_DP_CONNECTING 0xB3
			DP_MF_DP_CONNECTED 0xB4
			DP_MF_DP_DISCONNECTING 0xB5
			DP_MF_DP_DISCONNECTED 0xB6
				R/W	

0x9D	FW_STATE	31:24	fw_main_state:
			// main states
			NA 0x0
			DISCONNECTING 0x10
			DISCONNECTED 0x11
			// DPP
			DPP_CONNECTING 0x20
			DPP_CONNECTED 0x21
			DPP_DISCONNECTING 0x22
			// TBT
			TBT_CONNECTING 0x30
			TBT_CONNECTED 0x31
			TBT_DISCONNECTING 0x32
			// USB
			USB_CONNECTING 0x60
			USB_CONNECTED 0x61
			USB_DISCONNECTING 0x62
			// DP MULTI_FUNCTION
			DP_MF_CONNECTING 0xB0
			DP_MF_CONNECTED 0xB1
			DP_MF_DISCONNECTING 0xB2
				R/W	

0x9E	FW_DELAYS	7:0	delay_before_uart additional delay before sending the first uart message. Delay will be value * 1ms.	R/W	0x5
0x9E	FW_DELAYS	15:8	delay_before_dpp additional delay before setting internal muxes for dpp. Delay will be value * 10ms.	R/W	20

Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0x9E	FW_DELAYS	23:16	delay_before_lc_turn_off Minimum idle time before LC turns itself off * 10ms	R/W	host:25 device: 5
0x9E	FW_DELAYS	31:24	iecs_no_response_timeout	R/W	10
0x9F	LC_TARGET_ACCESS_DATA (IECS 16)	31:0	clc_tar_wr_data target write data for write access. Target read data for read access	R/W	0
0xA0	LC_TARGET_ACCESS_CTRL (IECS 16)	12:0	clc_tar_dw_index target address to be accessed	R/W	0
0xA0	LC_TARGET_ACCESS_CTRL (IECS 16)	18:13	clc_tar_port target port to be accesses	R/W	0
0xA0	LC_TARGET_ACCESS_CTRL (IECS 16)	20:19	clc_tar_cs target config space to be accessed	R/W	0
0xA0	LC_TARGET_ACCESS_CTRL (IECS 16)	21	target access type 0 for read. 1 for write.		
0xA0	LC_TARGET_ACCESS_CTRL (IECS 16)	22	clc_cio_sw_regs_access when this bit is asserted, it indicates that the access is directed to cio switch register space	R/W	0
0xA0	LC_TARGET_ACCESS_CTRL (IECS 16)	23	clc_pcie_sw_regs_access when this bit is asserted, it indicates that the access is directed to pcie switch register space	R/W	0
0xA0	LC_TARGET_ACCESS_CTRL (IECS 16)	25:24	Reserved	R/W	0
0xA0	LC_TARGET_ACCESS_CTRL (IECS 16)	26	clc_master_lock will cause target arbiter to lock arbitration and allow access only to this link controller until this bit is cleared	R/W	0
0xA0	LC_TARGET_ACCESS_CTRL (IECS 16)	29:27	Reserved	R/W	0
0xA0	LC_TARGET_ACCESS_CTRL (IECS 16)	30	clc_tar_timeout target access completion status bit: 0 - indicates that the last target access completed successfully. 1 - indicates that the last target access timed out	R/W	0

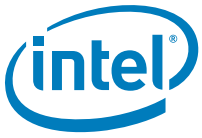


Table 34. Link Controller Vendor-Specific Capability per Controller Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default value
0xA0	LC_TARGET_ACCESS_CTRL (IECS 16)	31	Start1_done0 set to 1 to start the transaction. Cleared by controller for indicating the transaction is done	R/W	0
0xA1	LC_IECS_DATA_0 (IECS 9)	31:0	iecs_data IECS (addr 9) data register 0	R/W	
0xA2	LC_IECS_DATA_1 (IECS 9)	31:0	iecs_data IECS (addr 9) data register 1	R/W	
0xA3	LC_IECS_DATA_2 (IECS 9)	31:0	iecs_data IECS (addr 9) data register 2	R/W	
0xA4	LC_IECS_DATA_3 (IECS 9)	31:0	iecs_data IECS (addr 9) data register 3	R/W	

Table 35. POC_CSR POC Control/Status Register (Per Controller)

Bit offset	Field name	Functionality	Power-on Reset Value
[15:0]	wake_enables	When set, enables respective wake cause. [0]: ls_g1_change [1]: ls_g2_change [2]: ls_g3_change [3]: dpsrc_hpd_change [4]: cio_cable_disconnect [5]: dp_cable_disconnect [6]: usb_wake [7]: pwr_ctrl_change (gpio_0/1) [8]: cio_cable_disconnect_2 [9]: GPIO_2 change (rtd3_usb_pwr_en) [10]: GPIO_3 change (force_pwr) [11]: GPIO_4 assertion (wake_n/batlow) [12]: GPIO_5 change (slp_s3_n) [13]: GPIO_6 change (rtd3_cio_pwr_en) [14]: PERST_N change [15]: initial wake	0x8000
[31:16]	wake_cause	Latched cause of the last LC wakeup. Expected to have only 1 bit set, unless few events occurred exactly at the same time. Note: as LC domain can be woken up due to one of the ports, the other might report 0 in its wake_cause.	0x0000 (LC will see 0x8000 due to initial wake)
[32+0]	PWR_CTRL_SUSTAIN	When set, POC will sustain PWR_CTRL pin value using control bits, will take the data from PWR_CTRL_DATA.	0
[32+1]	PWR_CTRL_DATA	See PWR_CTRL_SUSTAIN	0
[32+2]	LS_G1_SUSTAIN	When set, POC will sustain LS_G1 pin value using control bits, will take the data from LS_G1_DATA.	0
[32+3]	LS_G1_DATA	see LS_G1_SUSTAIN	0
[32+4]	LS_G2_SUSTAIN	When set, POC will sustain LS_G2 pin value using control bits, will take the data from LS_G2_DATA.	0
[32+5]	LS_G2_DATA	See LS_G2_SUSTAIN	0
[32+6]	LS_G3_SUSTAIN	When set, POC will sustain LS_G3 pin value using control bits, will take the data from LS_G3_DATA.	0
[32+7]	LS_G3_DATA	See LS_G3_SUSTAIN	0
[32+8]	CSR_LS_G1_PU_RES_10K_EN	When set, LS_G1 pad connected to 10K PU.	0
[32+9]	CSR_LS_G1_PU_RES_2K_EN	When set, LS_G1 pad connected to 2K PU.	0

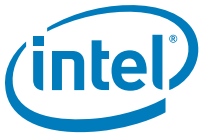


Table 35. POC_CSR POC Control/Status Register (Per Controller) (Continued)

Bit offset	Field name	Functionality	Power-on Reset Value
[32+10]	CSR_LS_G2_PU_RES_10K_EN	When set, LS_G2 pad connected to 10K PU.	1
[32+11]	CSR_LS_G2_PU_RES_2K_EN	When set, LS_G2 pad connected to 2K PU.	0
[32+12]	CSR_LS_G3_PU_RES_10K_EN	When set, LS_G2 pad connected to 10K PU.	0
[32+13]	CSR_LS_G3_PU_RES_2K_EN	When set, LS_G3 pad connected to 2K PU.	0
[32+14]	CSR_LSRX_EN_FAST_LINK	When set, and lsrx_change happened, CIO fast link bringup happens, and pause being sent on lstx – bought ports	0
[32+15]	SLP_S3#_EN_FAST_LINK	When set, and GPIO_5 change happened, CIO fast link bringup happens, and pause being sent on lstx	0
[32+16]	RTD3_PWR_EN_FAST_LINK	When set, and GPIO_6 change event happened, CIO fast link bringup happens, and pause being sent on lstx.	0
[32+17]	FORCE_PWR_EN_FAST_LINK	When set, and FORCE_PWR change happened, CIO fast link bringup happens, and pause being sent on lstx	0
[32+18]	BLOCK_LSTX_PULSE	When set, blocks lstx pulse that comes as a response to fast_link.	0
[32+19]	reserved		0
[32+20-21]	LSRX_CABLE_SELECT	Select which ls pin is the lsrx: 00: g1, 01:g2, 10: g3, default:g2.	01
[32+22-23]	LSTX_CABLE_SELECT	Select which ls pin is the lstx: 00: g1, 01:g2, 10: g3, default:g1.	0
[32+24-25]	HPD_CABLE_SELECT	Select which ls pin is the hpd: 00: g1, 01:g2, 10: g3, default:g3.	10
[32+26-27]	LSRX_2_CABLE_SELECT	Select which ls pin is the lsrx_2: 00: g1, 01:g2, 10: g3, default:g1.	0
[32+28-31]	reserved		0

Table 36. Control/Status register common (common register)

Bit offset	Field name	Functionality	Power-on Reset Value
[0]	GPIO_5_SUSTAIN (SLP_S3#)	When set, POC will sustain GPIO_5 pin value using GPIO_5_DATA	0
[1]	GPIO_5_DATA	see GPIO_5_SUSTAIN	0
[2]	GPIO_6_SUSTAIN (RTD3_CIO_PWR_EN)	When set, POC will sustain GPIO_6 pin value using GPIO_6_DATA	0
[3]	GPIO_6_DATA	see GPIO_6_SUSTAIN	0
[4]	BATLOW_SUSTAIN (GPIO_4)	When set, POC will sustain GPIO_4 pin value using BATLOW_DATA	0
[5]	BATLOW_DATA	see BATLOW_SUSTAIN	0

Table 36. Control/Status register common (common register)

Bit offset	Field name	Functionality	Power-on Reset Value
[6]	FORCE_PWR_SUSTAIN	When set, POC will sustain GPIO_3 pin value using FORCE_PWR_DATA	0
[7]	FORCE_PWR_DATA	see FORCE_PWR_SUSTAIN	0
[8]	GPIO2_SUSTAIN (RTD3_USB_PWR_EN)	When set, POC will sustain GPIO_2 pin value using GPIO_2_DATA	0
[9]	GPIO2_DATA	see GPIO2_SUSTAIN	0
[10]	GATE_WAKE_BY_BATLOW	When set, and GPIO_4 goes low, wake event won't occur.	0
[11]	WAKE_CAUSE_RESET	Allow manually clear latch_events. Meaning we can make the wake_cause transparent in this way.	0
[12]	CSR_SEL_CLK	bit that allow control on which clock goes out in OSC_CLK_DFT	0
[13]	OSC_CLK_DFT	When , POC 50MHz oscillator clock is driven on FORCE_PWR pin	0
[14]	LVR_REF_SVR	When set, the LVR uses the SVR as reference in order to change to use the SVR instead.	0
[15]	LVR_DISABLE_SVR_SW_ON	Can turn on/off the LVR - the LC is setting it at least 100ms after LVR_REF_SVR	0
[16]	LVR_DISABLE_SVR_SW_ON_DONE	indicate the the LVR switch SVR is done	0
[17-18]	TIME_LVR_DIS_TO_SVR_SW	set the scaling between disabling LVR and connecting the SVR switch	0
[19]	BLOCK_FUSE_LATCH	Blocks the fuses osc scaling even if we have fuse valid bit.	0
[20]	FORCE_OSC_EN	When set will leave the osc working even when going to sx.	0
[21]	CSR_PUT_1M_OSC_ON_FORCE_PWR	When set together with OSC_CLK_DFT the 1m clock will be driven on FORCE_PWR pin	0
[22-31]	reserved		0

Table 37. PCIE2TBT Register Description

Bit offset	Field name	Functionality	Power-on Reset Value
0	Valid	Set by the host indicating a new command sent, generates interrupt to LC and CM. Cleared by Host SW	0

Table 37. PCIE2TBT Register Description (Continued)

Bit offset	Field name	Functionality	Power-on Reset Value
7:1	Command	Defined commands: 0x01:0x00 Reserved 0x02 Go2Sx 0x03 Go2Sx_No_Wake 0x04 Sx_Exit_TBT_Connected 0x05 Sx_Exit_No_TBT_Connected 0x06 OS_Up 0x07 Reserved 0x08 Set_Security_Level (Data, see Table 428) 0x09 Get_Security_Level (Data, Table 428) 0x0A Set_lc_sw_fw_mailbox_bits 0x7F:0x0A Reserved	0
31:8	Data	Data associated (Defined specific per command)	0

Table 38. TBT2PCIE Register Description

Bit offset	Field name	Functionality	Power-on Reset Value
0	Done	Set by LC acknowledging the command sent from the host	0
7:1	Status	Defined statuses: 0x01:0x00 Reserved 0x02 Ok2Go2Sx[1] 0x03 Reserved 0x04 Sx_Exit_Tunneling_Done 0x05 Sx_Exit_received 0x06 OS_Up_Received 0x07 Reserved 0x08 Set_Security_Level Done (Data, Table 428) 0x09 Get_Security_Level Done (Data, Table 428) 0x0A Set_lc_sw_fw_mailbox_bits_done 0x7F:0x0A Reserved	0
11:8	Data	Data associated (Defined specific per status)	0
15:12	Error	Error Indication 0x0Command completed successfully 0x1General Error 0x2Error - Illegal Data 0x3Error – Timeout on command 0xF:4Reserved	0
31:16	Data	Data associated (Defined specific per command)	0

1. For this command the TBT2PCIE "Done" bit will not get cleared after the PCIE2TBT Valid bit was cleared as the device and the system are in their Sx entry flow

4.3.1.4.8 Flash Controller Vendor Specific Registers

The attributes of the Flash Controller vendor-specific capability registers are described in Table 39.

Note: The register offset is relative to DEV_VSEC_7_BASE in Table 19.

Table 39. Flash Controller Vendor-Specific Capability Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	VSEC_FC_CS_0	7:0	VSEC 7 Header Next Capability Pointer	RO	0
0	VSEC_FC_CS_0	15:8	VSEC 7 Header Capability ID This field must contain the value 05h indicating this is the start of the Vendor-Specific capability register set.	RO	5
0	VSEC_FC_CS_0	23:16	VSEC 7 Header VSEC ID This field is a vendor-defined ID number that indicates the nature and format of the VSEC structure.	RO	7
0	VSEC_FC_CS_0	31:24	VSEC 7 Header Length	RO	0
1	VSEC_FC_CS_1	15:0	VSEC 7 extended Header Next Capability Pointer	RO	0
1	VSEC_FC_CS_1	31:16	VSEC 7 extended Header LENGTH indicates the length of this configuration space	RO	0x40
2	FLASH_CTRL_REG2	23:0	Flash Active Region Base	RO	0xFFFFFF
2	FLASH_CTRL_REG2	31:24	reserved	RO	0xFF
3	FLASH_CTRL_REG3	15:0	Read pointer to digital section	R/W	0
3	FLASH_CTRL_REG3	31:16	Read pointer to SVR_ANA section	R/W S	0
4	FLASH_CTRL_REG4	15:0	Read pointer to Scratch section	R/W S	0
4	FLASH_CTRL_REG4	31:16	Read pointer to CP_UCODE section	R/W S	0
5	FLASH_CTRL_REG5	15:0	Read pointer to DP_OUT_UCODE section	R/W S	0
5	FLASH_CTRL_REG5	31:16	Read pointer to DP_IN_UCODE section	R/W S	0
6	FLASH_CTRL_REG6	15:0	Read pointer to LC_UCODE section	R/W S	0
6	FLASH_CTRL_REG6	31:16	Read pointer to ARC_UCODE section	R/W S	0
7	FLASH_CTRL_REG7	15:0	Read pointer to CIO_IRAM_UCODE section	R/W S	0
7	FLASH_CTRL_REG7	31:16	Read pointer to CIO_DRAM_UCODE section	R/W S	0
8	FLASH_CTRL_REG8	15:0	Read pointer to DP2HDMI_IRAM_UCODE section**HDP In/Out bypass mode** HDP IN -> OUT HDMI bypass enable	R/W S	0
8	FLASH_CTRL_REG8	31:16	Read pointer to DP2HDMI_DRAM_UCODE section**HDP In/Out bypass mode** HDP IN -> OUT HDMI bypass enable	R/W S	0
9	FLASH_CTRL_REG9	15:0	reserved	R/W S	0
9	FLASH_CTRL_REG9	31:16	Length of data to read from ARC_CACHE section, B	R/W	0
10	FLASH_CTRL_REG10	23:0	Read pointer to ARC_CACHE section	R/W	0
10	FLASH_CTRL_REG10	31:24	reserved	R/W	0
11	FLASH_CTRL_REG11	15:0	Last stored length of section to read	R/W	0

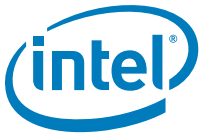


Table 39. Flash Controller Vendor-Specific Capability Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
11	FLASH_CTRL_REG11	23:16	Last stored analog registers address (for strobing)	R/W	0
11	FLASH_CTRL_REG11	31:24	Last stored analog registers data (for strobing)	R/W	0
12	FLASH_CTRL_REG12	31:0	Dword of microde data read from SPI before stored in ucode_data register	R/W	0
13	FLASH_CTRL_REG13	31:0	Stable Data for strobing to microcode clients	R/W	0
14	FLASH_CTRL_REG14	23:0	Address for legacy dword read	R/W	0
14	FLASH_CTRL_REG14	31:24	Reserved	R/W	0
15	FLASH_CTRL_REG15	31:0	Reserved	R/W	0
16	FLASH_CTRL_REG16	31:0	Generic Access Data register bits 511:480 (MSB)	R/W	0
17	FLASH_CTRL_REG17	31:0	Generic Access Data bits 479:448	R/W	0
18	FLASH_CTRL_REG18	31:0	Generic Access Data bits 447:416	R/W	0
19	FLASH_CTRL_REG19	31:0	Generic Access Data bits 415:384	R/W	0
20	FLASH_CTRL_REG20	31:0	Generic Access Data bits 383:352	R/W	0
21	FLASH_CTRL_REG21	31:0	Generic Access Data bits 352:320	R/W	0
22	FLASH_CTRL_REG22	31:0	Generic Access Data bits 319:288	R/W	0
23	FLASH_CTRL_REG23	31:0	Generic Access Data bits 287:256	R/W	0
24	FLASH_CTRL_REG24	31:0	Generic Access Data bits 255:224	R/W	0
25	FLASH_CTRL_REG25	31:0	Generic Access Data bits 223:192	R/W	0
26	FLASH_CTRL_REG26	31:0	Generic Access Data bits 191:160	R/W	0
27	FLASH_CTRL_REG27	31:0	Generic Access Data bits 159:128	R/W	0
28	FLASH_CTRL_REG28	31:0	Generic Access Data bits 127:96	R/W	0
29	FLASH_CTRL_REG29	31:0	Generic Access Data bits 95:64	R/W	0
30	FLASH_CTRL_REG30	31:0	Generic Access Data bits 63:32	R/W	0
31	FLASH_CTRL_REG31	31:0	Generic Access Data bits 31:0 (LSB)	R/W	0
32	FLASH_CTRL_REG32	23:0	SPI 24bit address for Generic Access, valid if gen_spi_address_present is asserted	R/W	0
32	FLASH_CTRL_REG32	31:24	SPI Instruction for Generic Access, valid if gen_spi_address_present is asserted	R/W	0
33	FLASH_CTRL_REG33	7:0	Amount of bytes to shift in/out	R/W	0
33	FLASH_CTRL_REG33	11:8	Amount of dummy bytes to shift out after 24bit address, before shifting in/out the data	R/W	0
33	FLASH_CTRL_REG33	26:12	reserved	R/W	0
33	FLASH_CTRL_REG33	27	CM GENERIC access enable. CM should set this bit for the *entire* operation it intends to perform thru GENERIC mechanism, set before start and clear only after finish	R/W	0
33	FLASH_CTRL_REG33	28	Gen NVM Accesses Allowed 0: allowed, 1: not allowed	RO	0
33	FLASH_CTRL_REG33	29	Gen SPI Address Present 1: need to shift out address from SPI_CMD_ADDR after command; 0: command without address	R/W	0
33	FLASH_CTRL_REG33	30	Gen SPI Shift In1 Out0 in: read, out:write	R/W	0

Table 39. Flash Controller Vendor-Specific Capability Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
33	FLASH_CTRL_REG33	31	Gen Req1 Ack0 SW to set to 1, HW to clear upon completion	SC	0
34	FLASH_CTRL_REG34	15:0	Digital section offset in Bytes	R/W	0
34	FLASH_CTRL_REG34	23:16	Data in to write into digital section, Data out when reading from digital section	R/W	0
34	FLASH_CTRL_REG34	30:24	Reserved	R/W	0
34	FLASH_CTRL_REG34	31	When set to 1, data_in will be written to respective internal array offset and the bit will be cleared. when 0, data_in/out will represent the respective internal array offset value	R/W SC	0
35-60	FLASH_CTRL_REG35-60	31:0	Reserved	R/W	0
61	FLASH_CTRL_REG61	15:0	Length of data to read from DP2HDMI_CACHE section, B**HDP In/Out bypass mode** HDP IN -> OUT HDMI bypass enable	R/W S	0
61	FLASH_CTRL_REG61	31:16	Reserved	R/W	0
62	FLASH_CTRL_REG62	23:0	Read pointer to DP2HDMI_CACHE section**HDP In/Out bypass mode** HDP IN -> OUT HDMI bypass enable	R/W	0
62	FLASH_CTRL_REG62	30:24	Reserved	R/W	0
62	FLASH_CTRL_REG62	31	Read pointer to DP2HDMI_CACHE section**HDP In/Out bypass mode** HDP IN -> OUT HDMI bypass enable	R/W	0
63	FLASH_CTRL_REG63	29:0	Reserved	R/W	0
63	FLASH_CTRL_REG63	30	Scratch erase - FW/SW to set to 1, HW to clear upon completion	R/W SC	0
63	FLASH_CTRL_REG63	31	Scratch program - FW/SW to set to 1, HW to clear upon completion	R/W SC	0

4.3.1.4.9 Thunderbolt Phy Vendor Specific Registers

The attributes of the Thunderbolt Phy vendor-specific capability registers are described in Table 40.

Note: The registers offsets are relative to DEV_VSEC_9_BASE in Table 19.

Figure 22 describes the phy vendor specific memory map. The first section controls logic common to the entire chip. The following sections control logic common per port, and the last sections control logic per lane.

The per_port and per_lane sections are further divideded into hw mapped registers and memory mapped registers.

The number of ports, number of lanes, section sizes, etc., are all readable in the first offsets of the vsec.

Figure 22. VSEC9 Registers Map

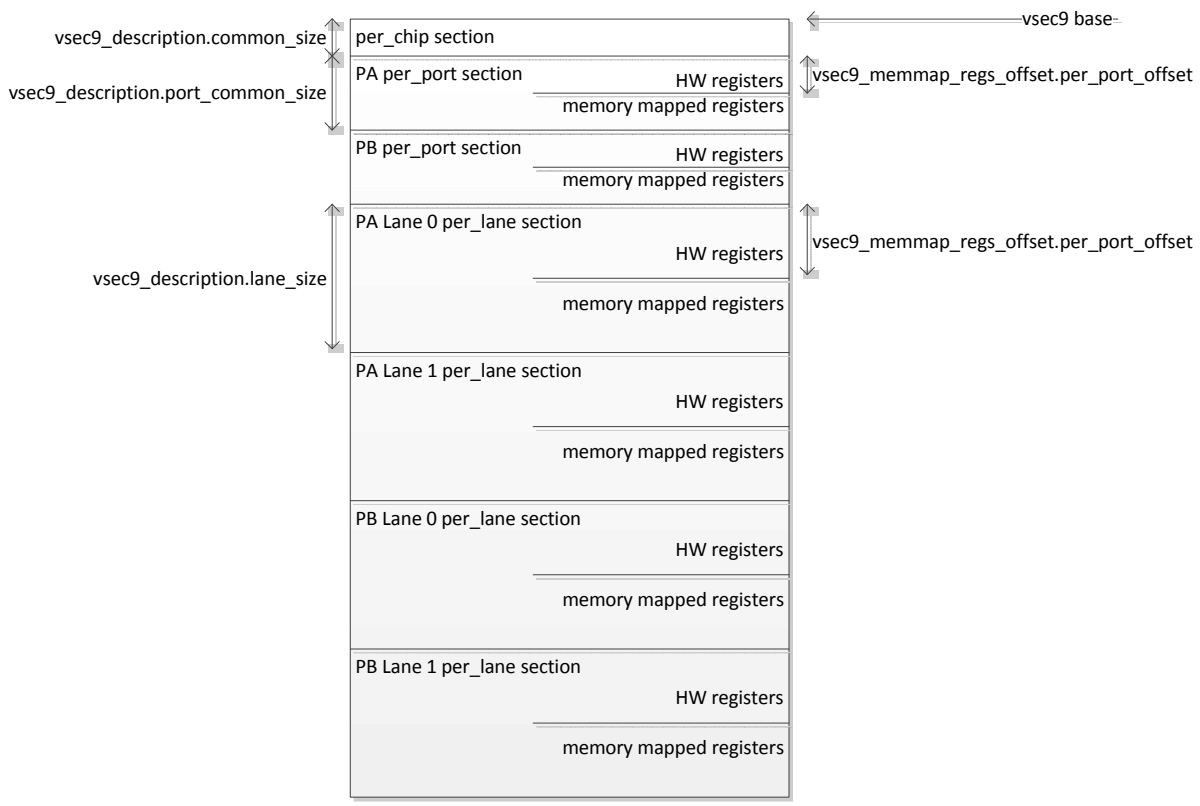


Table 40. Thunderbolt Phy Vendor-Specific Capability Register Attributes

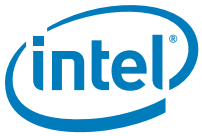
Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	VSEC9_HEADER	7:0	next Capability Pointer	RO	0
		15:8	vsec_cap Capability ID - This field must contain the value 05h indicating this is the start of the Vendor-Specific capability register set.	RO	5
		23:16	vsec_id This field is a vendor-defined ID number that indicates the nature and format of the VSEC structure.	RO	9
		31:24	vsec_length (0-extended)	RO	0
1	VSEC9_EXTENDED_HEADER	15:0	next Capability Pointer	RO	4087
		31:16	vsec_length indicates the length of this configuration space	RO	1344

Table 40. Thunderbolt Phy Vendor-Specific Capability Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
2	VSEC9_DESCRIPTION	3:0	port_count number of tbt ports (each has 2 lanes)	RO	2
		15:4	lane_size number of registers per lane	RO	256
		23:16	common_size number of registers per common section (one such section per chip)	RO	64
		31:24	port_common_size number of registers per port common section (number of sections according to port_count)	RO	128
3	VSEC_MEM_MAP_REGS_OFFSET	7:0	per_port_offset sw regs offset within each port space	RW	64
		19:8	per_lane_offset sw regs offset within each lane space	RW	128
		31:20	reserved	RO	0
4	TMU_PLL_CTRL0	3:0	reserved	RW	
		4	locked PLL lock indication	RO	0
		31:5	reserved		

Table 41. Per Port Registers

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
8:0	Reserved				
9	COMMON_SAMPLE_CTRL	23:0	reserved		
		24	cio0_tx_en cio lane 0 tx enable status	RO	0
		25	cio1_tx_en cio lane 1tx enable status	RO	0
		26	usb0_tx_en usb lane 0 tx enable status	RO	0
		27	usb1_tx_en usb lane 1 tx enable status	RO	0
		28	dp0_tx_en dp lane 0 tx enable status	RO	0
		29	dp1_tx_en dp lane 1 tx enable status	RO	0
		30	dp2_tx_en dp lane 2 tx enable status	RO	0
		31	dp3_tx_en dp lane 3 tx enable status	RO	0
10	RESERVED				
11	COMMON_INFO	15:0	reserved	RO	0
		16	controller_id 0-PA, 1-PB	RO	0/1
		31:17	reserved		
12-15	RESERVED				

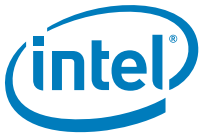


16	COMMON_FW	7:0	fw_state_0 updated by the fw	RW	0
		15:8	fw_state_1 updated by the fw	RW	0
		23:16	fw_state_2 updated by the fw	RW	0
		31:24	fw_version updated by the fw	RW	0
17-20	RESERVED	31:0			
21	COMMON_LC_LINK_MODE	0	lc_cio_mode cio mode indication from lc	RO	0
		1	lc_dp_mode dp mode indication from lc	RO	0
		2	lc_usb2_mode usb2 mode indication from lc	RO	0
		3	lc_usb3_mode usb3 mode indication from lc	RO	0
		4	lc_dock_port_mode dock_port mode indication from lc	RO	0
		5	c_usb_lane_sel usb3 mode lane select from lc	RO	0
		6	lc_cio_link_speed link speed when in cio mode: 0-10G, 1-20G	RO	0
		7	lc_swap_lanes lanes are swapped (informative. the controller has noting to do with it)	RO	0
		16:8	reserved	RW	0
		17	phy_port_init_done port initialization completed	RW	0
		31:18	reserved	RO	0
28-22	RESERVED	**31:0**	reserved	RO	0
29	TX_PLL_ANA_CTRL	3:0	reserved	RW	
		4	pll_stable_to_car set to notify car that cio pll is stable	RW	0
		31:5	reserved	RO	0
51:30	RESERVED	31:0	reserved	RO	0

52	USB_TX_SWING	2:0	gen2_pre_cursor_swing TX 1st pre-cursor swing control for usb3.1 gen2. Per port.	RW	0
		3	reserved	RW	0
		10:4	gen2_invert_swing TX invert swing control for usb3.1 gen2. Per port.	RW	0
		11	gen2_select_pre1_post2 select pre or post2 emphasis, 0: CIOTXn_SW_PRE is post2-emphasis 1: CIOTXn_SW_PRE is pre-emphasis for usb3.1 gen2. Per port.	RW	1
		15:12	gen2_post1_cursor_swing TX 1st post-cursor swing control for usb3.1 gen2. Per port.	RW	0
		18:16	gen1_pre_cursor_swing TX 1st pre-cursor swing control for usb3.1 gen1. Per port.	RW	0
		19	reserved	RW	0
		26:20	gen1_invert_swing TX invert swing control for usb3.1 gen1. Per port.	RW	0
		27	gen1_select_pre1_post2 select pre or post2 emphasis, 0: CIOTXn_SW_PRE is post2-emphasis 1: CIOTXn_SW_PRE is pre-emphasis for usb3.1 gen1. Per port.	RW	1
		31:28	gen1_post1_cursor_swing TX 1st post-cursor swing control for usb3.1 gen1. Per port.	RW	0
53	USB_TX_SWING1	2:0	lfps_pre_cursor_swing TX 1st pre-cursor swing control for usb3.1 lfps. Per port.	RW	0
		3	reserved	RW	0
		10:4	lfps_invert_swing TX invert swing control for usb3.1 lfps. Per port.	RW	0
		11	lfps_select_pre1_post2 select pre or post2 emphasis, 0: CIOTXn_SW_PRE is post2-emphasis 1: CIOTXn_SW_PRE is pre-emphasis for usb3.1 lfps. Per port.	RW	1
		15:12	lfps_post1_cursor_swing TX 1st post-cursor swing control for usb3.1 lfps. Per port.	RW	0
		31:16	reserved	RW	0

Table 42. Per Port - Memory Mapped Registers

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	PORT_SW_FW_MAILBOX	31:0	sw_fw_mailbox-See section 8.8.6 for details.	RW	0



1	PORT_SW_0	5:0	tx_pll_calibration_value valid when tx_pll_calibrated is set.	RW	0
		6	reserved	RW	0
		7	tx_pll_calibrated	RW	0
		15:8	current_mode 8'h0:disconnected, 8'h1:cio, 8'h2:dp, 8'h8:usb3, 8'h10:multi function DP	RW	0
		17:16	current_speed 2'b00:20G, 2'b01:10G, 2'b10:5G, 2'b11:reserved	RW	0
		31:18	reserved	RW	0

Table 43. per lane registers

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	GENERAL_LANE	15:0	reserved	RW	0
		23:16	lane_tx_state updated by fw	RW	0
		31:24	lane_rx_state updated by fw	RW	0
1	RESERVED	31:0	reserved	RW	0
2	CAR_CTRL	23:0	reserved	RW	0
		24	rx_eq_done indication that rx is locked. car can release rx clock/reset to null/port/usb	RW	0
		25	rx_is_active indication that rx is active, ready to start (or already started) equalization	RW	0
		31:26	reserved	RO	0
9-3	RESERVED	31:0			
10	TX_CTRL	1:0	reserved	RW	1
		2	tx_is_active indication from tx sync machine that cio tx lane was enabled	RO	0
		15:3	reserved	RO	0
		18:16	pre_cursor_swing TX 1st pre-cursor swing control. in cio mode, used for TXn.	RW	0
		19	reserved	RW	0
		26:20	Invert_swing TX invert swing control. in cio mode, used for TXn.	RW	0
		27	select_pre1_post2 select pre or post2 emhasis, 0: CIOTXn_SW_PRE is post2-emphasis 1: CIOTXn_SW_PRE is pre-emphasis. in cio mode, used for TXn.	RW	1
		31:28	post1_cursor_swing TX 1st post-cursor swing control. in cio mode, used for TXn.	RW	0
22-11	RESERVED	31:0			

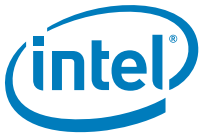
23	RX_CDR_CAL_CTRL2	3:0	reserved	RW	0
		4	Freq_lock cdr lock indication from lock detection logic	RO	0
		5	Force_cdr_lock cdr lock indication force	RW	0
		6	Force_cdr_lock_value cdr lock indication force value	RW	0
		31:7	reserved	RW	
24	RESERVED	31:0	reserved	RW	
25	RX_SOURCE_SELECT	27:0	reserved	RW	0
		28	update_force_value self cleared. Generates a sample of the translator-force value (only where select value applies)	RWC	0
		31:29	reserved	RW	0
31-26	RESERVED	31:0	reserved		
32	RX_C1_MONITOR	7:0	c1do_monitor data odd c1 monitor. 2's compliment.	RO	0
		15:8	c1de_monitor data even c1 monitor. 2's compliment.	RO	0
		31:16	reserved	RO	0
33	RX_VREF_VALUE	8:0	vrefeo_init_value odd error slicer vref value. 2's compliment. Bit 0 ignored.	RW	0
		15:9	reserved	RO	0
		24:16	vrefee_init_value even error slicer vref value. 2's compliment. Bit 0 ignored.	RW	0
		31:25	reserved	RO	0
34	RX_VREF_MONITOR	8:0	vrefeo_monitor vrefe to ana monitor. 2’s compliment.	RO	0
		15:9	reserved	RO	0
		24:16	vrefee_monitor vrefo to ana monitor. 2’s compliment.	RO	0
		31:25	reserved	RO	0
37-35	RESERVED	31:0	reserved		
38	EYEMON_ANA	7:0	reserved		0
38	EYEMON_ANA	14:8	pi_phase_monitor. Error slicer time offset. Unsigned (wraps)	RO	0
38	EYEMON_ANA	15	reserved	RO	0
38	EYEMON_ANA	25:16	pi_phase. Error slicer time offset control. Unsigned (wraps).	RW	0
38	EYEMON_ANA	31:26	reserved	RO	0

39	EYEMON_CTRL0	1:0	search_type Eye Monitor mode, 0 - alignment search, 1- single search	RW	0
		2	reserved	RW	0
		3	go Activation for eye monitor measurement only. Level - triggered by rising edge	RW	0
		4	done Eye monitor operation done. Level. Deasserted when reset_and_go/go are deasserted.	RO	0
		7:5	reserved	RW	0
		10:8	mask_select Compare type. 0: all, 1: after_1, 2: after_0	RW	0
		11	reserved	RW	0
		13:12	mask_even_odd_select 0-compare all. 1- compare odd only. 2 - compare even only	RW	0
		15:14	reserved	RW	0
		22:16	align_location best alignment location	RO	0
		31:23	reserved		0
40	EYEMON_CTRL1	19:0	symbol_count Number of cycles for compare	RW	0
		31:20	reserved	RW	0
41	EYEMON_ERROR_COUNTER	25:0	error_count Number of compare mismatches	RO	0
		31:26	reserved	RO	0
42	EYEMON_CHECK_COUNTER	25:0	check_count Number of compared bits after masking	RO	0
		31:26	reserved	RO	0
69-43	RESERVED	31:0	reserved		
70	LC_CTRL	7:0	reserved		0
		11:8	txffe_from_partner_current_value partner txffe current value	RO	0
		12	reserved	RO	0
		13	lc_enable_cio_tx link tx should be enabled	RO	0
		14	lc_enable_cio_rx link rx should be enabled	RO	0
		23:15	reserved		0
		27:24	txffe_to_partner_current_value txffe current value	RW	0
		31:28	reserved	RW	0
71	USB_REGS_CTRL0	0	tx_enable usb enable tx indication	RO	0
		31:1	reserved	RO	0
73-72	RESERVED	31:0	reserved		

74	TX_DFT_CTRL	0	dft_en_tx_prbs actiave the prbs	RW	0
		3:1	dft_tx_prbs_sel select the PRBS algorithm to be driven on tx. 0-prbs7, 1-prbs9, 2-prbs11, 3-prbs15, 4-prbs23, 5-prbs31, 6-prbs58, 7-reserved	RW	0
		4	dft_init_tx_prbs pulse self cleared set PRBS seed to be tx_prbs_init_high/low	RWC	0
		31:8	reserved		0
75	TX_DFT_DEBUG0	31:0	tx_prbs_init_low tx prbs init value low	RW	0
76	TX_DFT_DEBUG1	31:0	tx_prbs_init_high tx prbs init value high	RW	0
80-77	RESERVED	31:0	reserved	RW	0
81	RX_DFT_CTRL	0	dft_en_rx_prbs actiave the prbs	RW	0
		3:1	rft_rx_prbs_sel select the PRBS algorithm to be checked on rx. 0-prbs7, 1-prbs9, 2-prbs11, 3-prbs15, 4-prbs23, 5-prbs31, 6-prbs58, 7-reserved	RW	0
		12:4	reserved	RW	0
		13	rx_ber_counter_en activate bit error rate counter / symbol counter	RW	0
		14	rx_ber_counter_clr clear bit error rate counter / symbol counter	RWC	0
		31:15	reserved	RO	0
82	RX_DFT_STATUS	0	dft_rx_prbs_ber_lock indicates that PRBS detector is locked	RO	0
		1	dft_rx_prbs_lock_failed indicates that PRBS detector failed to lock	RO	0
		31:2	reserved	RO	0
83	RX_DFT_BER_COUNTER	15:0	ber_cntr BER counter - increments on every bit error	RO	0
		31:16	reserved	RO	0
84	RX_DFT_SYMBOL_COUNTER_LOW	31:0	sym_cntr_low symbol counter increments on every received 32UI, whenever ber counter is enabled - low bits	RO	0
85	RX_DFT_SYMBOL_COUNTER_HIGH	11:0	sym_cntr_high symbol counter increments on every received 32UI, whenever ber counter is enabled - high bits	RO	0
		31:12	reserved	RO	0

Table 44. Per Lane - Memory Mapped Registers

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	LANE_SW_FW_MAILBOX	31:0	sw_fw_mailbox per lane sw fw mailbox. See section 8.8.6 for details.	RW	0
3:1	reserved registers	31:0		RW	0



4	LANE_MM4	15:0	reserved	RW	0
		23:16	best eye width. Best eye width, in PI steps.	RW	0
		31:24	reserved	RW	0

4.3.1.4.10 USB Vendor Specific Registers

The attributes of the USB vendor-specific capability registers are described in Table 45.

Note: The register offset is relative to DEV_VSEC_10_BASE in Table 19.

Table 45. USB Vendor-Specific Capability Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	VSEC_USB	7:0	VSEC 10 Header Next Capability Pointer	RO	0
0	VSEC_USB	15:8	VSEC 10 Header Capability ID This field must contain the value 05h indicating this is the start of the Vendor-Specific capability register set.	RO	5
0	VSEC_USB	23:16	VSEC 10 Header VSEC ID This field is a vendor-defined ID number that indicates the nature and format of the VSEC structure.	RO	10
0	VSEC_USB	31:24	VSEC 10 Header Length	RO	0
1	VSEC_USB_EXT_HEADER	15:0	VSEC 10 extended Header Next Capability Pointer	RO	0
1	VSEC_USB_EXT_HEADER	31:16	VSEC 10 extended Header LENGTH - indicates the length of this configuration space	RO	25
2	VSEC_USB_DESC	3:0	Number of USB_TOP structures	RO	1
2	VSEC_USB_DESC	7:4	Reserved	RO	0
2	VSEC_USB_DESC	15:8	POC_USB_Size	RO	10
2	VSEC_USB_DESC	31:16	USB_TOP_Size	RO	15
3	VSEC_USB_PA_UTMI_STS	23:0	UTMI {rx_rcv, rxerror, rxactive, rxvalid, txready, hostdisconnect,linestate[1:0]} {tx_se0, tx_enable_n, tx_dat, fslsserialmode, suspendm, l1_en, xcvrselect[1:0]}; {opmode[1:0], termselect, dppulldown, auxreset_b, txvalid, bisterror, bistcomplete};	RO	
3	VSEC_USB_PA_UTMI_STS	31:24	TIF_RDATA USB2 Phy TIF register read value	RO	

Table 45. USB Vendor-Specific Capability Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
4	VSEC_USB_PB_UTMI_STS	23:0	UTMI {rx_rcv, rxerror, rxactive, rxvalid, txready, hostdisconnect,linestate[1:0]} {tx_se0, tx_enable_n, tx_dat, fslsserialmode, suspendm, l1_en, xcvrselect[1:0]}; {opmode[1:0], termselect, dppulldown, auxreset_b, txvalid, bisterror, bistcomplete};	RO	
4	VSEC_USB_PB_UTMI_STS	31:24	TIF_RDATA USB2 Phy TIF register read value	RO	
5	VSEC_USB_POC_CFG0	7:0	cfg_rx_lfps_thr_tune CIORX1_USB_LFPS_THR_TUNE/ CIORX0_USB_LFPS_THR_TUNE default values	R/W	0
5	VSEC_USB_POC_CFG0	15:8	cfg_tx_discharge_duration Defines, in resolution of 4us, how much time it takes to discharge tx line	R/W	75
5	VSEC_USB_POC_CFG0	23:16	cfg_rxdet_duration Defines, in resolution of 4us, after how much time (since usb_tx_rxdetect_en assertion) phy_to_usb_tx_rxdet_status should be checked	R/W	75
5	VSEC_USB_POC_CFG0	24	cfg_rxdet_status_polarity Defines polarity of phy_to_usb_tx_rxdet_status, i.e. what value should be considered as "partner's presence"	R/W	0
5	VSEC_USB_POC_CFG0	28:25	cfg_hostdic_filt_thresh Number of usec to force hostdisconnect down after de-assertion of fslsserialmode	R/W	3
5	VSEC_USB_POC_CFG0	29	cfg_pgcb_fdfx_pgcb_bypass Force PGCB to initiate power gate/ungate based on cfg_pgcb_fdfx_pgcb_ovr	R/W	0
5	VSEC_USB_POC_CFG0	30	cfg_pgcb_fdfx_pgcb_ovr	R/W	0
5	VSEC_USB_POC_CFG0	31	cfg_leg_rcba_xhd Function disable	R/W	0
6	VSEC_USB_POC_CFG1	1:0	cfg_frc_txrx_trans_done When set, tx_trans_done/rx_trans_done will be forced to '1'	R/W	0
6	VSEC_USB_POC_CFG1	3:2	cfg_frc_ownership When set, requests the port ownership regardless of lc_usb3_mode state	R/W	0
6	VSEC_USB_POC_CFG1	4	cfg_ownership_taking_en When set, enables handshake for port ownership based on lc_usb3_mode state	R/W	1
6	VSEC_USB_POC_CFG1	6:5	cfg_frc_pipe_rxeidle_val Value to force on PIPE RxEidle	R/W	0

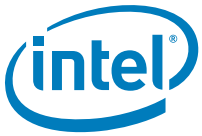


Table 45. USB Vendor-Specific Capability Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
6	VSEC_USB_POC_CFG1	8:7	cfg_frc_pipe_rxeidle_pre When set, PIPE RxEidle is forced to cfg_frc_pipe_rxeidle_val	R/W	0
6	VSEC_USB_POC_CFG1	10:9	cfg_frc_pipe_rxeidle_pre When '1' written into this bit, PIPE RxEidle is forced down for two PCLK cycle	R/W	0
6	VSEC_USB_POC_CFG1	11	cfg_fake_usb3_mode_en When set, usb3_digphy_ctrl will allow the controller to go out of P3 even in non-usb3_mode. In this case PCLK won't have the correct frequency	R/W	1
6	VSEC_USB_POC_CFG1	13:12	cfg_frc_rxdet_val Value to force in RxDet flow	R/W	0
6	VSEC_USB_POC_CFG1	15:14	cfg_frc_rxdet_pre When set, RxDet flow will be terminated based on cfg_frc_rxdet_val	R/W	0
6	VSEC_USB_POC_CFG1	17:16	cfg_frc_tx2rx_eidle_lpbk_pre When set, usb_tx_eidle is looped back on PIPE RxElecIdle	R/W	0
6	VSEC_USB_POC_CFG1	20:18	cfg_visa_sel When set, usb_tx_eidle is looped back on PIPE RxElecIdle	R/W	0
6	VSEC_USB_POC_CFG1	25:21	cfg_rx_lfps_filt_tune When set, usb_tx_eidle is looped back on PIPE RxElecIdle	R/W	7
7	VSEC_USB_PA_UTMI_CFG	0	pa_usb2_phy_tif_clk_en USB2 Phy TIF register access: Clock enable (should be enabled to access TIF)	R/W	0
7	VSEC_USB_PA_UTMI_CFG	1	pa_usb2_phy_tif_rstb USB2 Phy TIF register access: RESET# (should be de-asserted (set to '1') to access TIF)	R/W	0
7	VSEC_USB_PA_UTMI_CFG	2	pa_usb2_phy_tif_wen USB2 Phy TIF register access: write-enable	R/W	0
7	VSEC_USB_PA_UTMI_CFG	4	pa_usb2_phy_bistmodesel USB2 Phy BIST: mode select: 0/1 - HS/FS mode	R/W	0
7	VSEC_USB_PA_UTMI_CFG	5	pa_usb2_phy_biston USB2 Phy BIST: Enable: Active High. Assertion of this signal starts the BIST operation.	R/W	0
7	VSEC_USB_PA_UTMI_CFG	7:6	pa_usb2_phy_loopback USB2 Phy Loopback Mode: 00: Loopback OFF 01: LS Loopback ON 10: FS Loopback ON 11: HS Loopback ON	R/W	0

Table 45. USB Vendor-Specific Capability Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
7	VSEC_USB_PA_UTMI_CFG	15:8	pa_usb2_phy_tif_addr USB2 Phy TIF register access: ADDRESS	R/W	0
7	VSEC_USB_PA_UTMI_CFG	23:16	pa_usb2_phy_tif_wdata USB2 Phy TIF register access: WRITE DATA	R/W	0
7	VSEC_USB_PA_UTMI_CFG	25:24	pa_frc_utmi_linestate_val USB2 Phy UTMI force: value to be forced on linestate	R/W	0
7	VSEC_USB_PA_UTMI_CFG	26	pa_frc_utmi_linestate USB2 Phy UTMI force: when set, pa_frc_utmi_linestate_val[1:0] is forced on UTMI linestate	R/W	0
7	VSEC_USB_PA_UTMI_CFG	27	pa_frc_utmi_hostdisconnect_val USB2 Phy UTMI force: value to be forced on hostdisconnect	R/W	0
7	VSEC_USB_PA_UTMI_CFG	28	pa_frc_utmi_hostdisconnect USB2 Phy UTMI force: when set, pa_frc_utmi_hostdisconnect_val is forced on UTMI hostdisconnect	R/W	0
7	VSEC_USB_PA_UTMI_CFG	29	pa_usb2_phy_polarity USB2 Phy D+/D- polarity	R/W	0
7	VSEC_USB_PA_UTMI_CFG	30	cfg_gpio_oc_mask[0] Ignore overcurrent from GPIO	R/W	0
7	VSEC_USB_PA_UTMI_CFG	31	cfg_frc_rxlfpsen[0] When set, Rx LFPS monitoring is forced to enabled state	R/W	0
8	VSEC_USB_PB_UTMI_CFG	0	pb_usb2_phy_tif_clk_en USB2 Phy TIF register access: Clock enable (should be enabled to access TIF)	R/W	0
8	VSEC_USB_PB_UTMI_CFG	1	pb_usb2_phy_tif_rstb USB2 Phy TIF register access: RESET# (should be de-asserted (set to '1') to access TIF)	R/W	0
8	VSEC_USB_PB_UTMI_CFG	2	pb_usb2_phy_tif_wen USB2 Phy TIF register access: write-enable	R/W	0
8	VSEC_USB_PB_UTMI_CFG	4	pb_usb2_phy_bistmodesel USB2 Phy BIST: mode select: 0/1 - HS/FS mode	R/W	0
8	VSEC_USB_PB_UTMI_CFG	5	pb_usb2_phy_biston USB2 Phy BIST: Enable: Active High. Assertion of this signal starts the BIST operation.	R/W	0

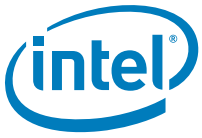


Table 45. USB Vendor-Specific Capability Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
8	VSEC_USB_PB_UTMI_CFG	7:6	pb_usb2_phy_loopback USB2 Phy Loopback Mode: 00: Loopback OFF 01: LS Loopback ON 10: FS Loopback ON 11: HS Loopback ON	R/W	0
8	VSEC_USB_PB_UTMI_CFG	15:8	pb_usb2_phy_tif_addr USB2 Phy TIF register access: ADDRESS	R/W	0
8	VSEC_USB_PB_UTMI_CFG	23:16	pb_usb2_phy_tif_wdata USB2 Phy TIF register access: WRITE DATA	R/W	0
8	VSEC_USB_PB_UTMI_CFG	25:24	pb_frc_utmi_linestate_val USB2 Phy UTMI force: value to be forced on linestate	R/W	0
8	VSEC_USB_PB_UTMI_CFG	26	pb_frc_utmi_linestate USB2 Phy UTMI force: when set, pb_frc_utmi_linestate_val[1:0] is forced on UTMI linestate	R/W	0
8	VSEC_USB_PB_UTMI_CFG	27	pb_frc_utmi_hostdisconnect_val USB2 Phy UTMI force: value to be forced on hostdisconnect	R/W	0
8	VSEC_USB_PB_UTMI_CFG	28	pb_frc_utmi_hostdisconnect USB2 Phy UTMI force: when set, pb_frc_utmi_hostdisconnect_val is forced on UTMI hostdisconnect	R/W	0
8	VSEC_USB_PB_UTMI_CFG	29	pb_usb2_phy_polarity USB2 Phy D+/D- polarity	R/W	0
8	VSEC_USB_PB_UTMI_CFG	30	cfg_gpio_oc_mask[1] Ignore overcurrent from GPIO	R/W	0
8	VSEC_USB_PB_UTMI_CFG	31	cfg_frc_rxlfpsen[1] When set, Rx LFPS monitoring is forced to enabled state	R/W	0
9	VSEC_USB_PAPB_UTMI_CFG	0	pa_frc_utmi_en USB2 Phy UTMI force: forces various UTMI signals (instead of their value from xHC)	R/W	0
9	VSEC_USB_PAPB_UTMI_CFG	2	pa_frc_utmi_auxreset_b USB2 Phy UTMI force: RESET value	R/W	0
9	VSEC_USB_PAPB_UTMI_CFG	3	pa_frc_utmi_dmpulldown USB2 Phy UTMI force: DMPULLDOWN value	R/W	0
9	VSEC_USB_PAPB_UTMI_CFG	4	pa_frc_utmi_dppulldown USB2 Phy UTMI force: DPPULLDOWN value	R/W	0
9	VSEC_USB_PAPB_UTMI_CFG	5	pa_frc_utmi_termselect USB2 Phy UTMI force: TERMSELECT value	R/W	0
9	VSEC_USB_PAPB_UTMI_CFG	7:6	pa_frc_utmi_opmode USB2 Phy UTMI force: OPMODE value	R/W	0
9	VSEC_USB_PAPB_UTMI_CFG	9:8	pa_frc_utmi_xcvrselect USB2 Phy UTMI force: XCVRSELECT value	R/W	0

Table 45. USB Vendor-Specific Capability Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
9	VSEC_USB_PAPB_UTMI_CFG	10	pa_frc_utmi_l1_en USB2 Phy UTMI force: L1_EN value	R/W	0
9	VSEC_USB_PAPB_UTMI_CFG	11	pa_frc_utmi_suspendm USB2 Phy UTMI force: SUSPENDM value	R/W	0
9	VSEC_USB_PAPB_UTMI_CFG	12	pa_frc_utmi_fslsserialmode USB2 Phy UTMI force: FSLSSERIALMODE value	R/W	0
9	VSEC_USB_PAPB_UTMI_CFG	13	pa_frc_utmi_tx_dat USB2 Phy UTMI force: TX_DAT value	R/W	0
9	VSEC_USB_PAPB_UTMI_CFG	14	pa_frc_utmi_tx_enable_n USB2 Phy UTMI force: TX_ENABLE_N value	R/W	0
9	VSEC_USB_PAPB_UTMI_CFG	15	pa_frc_utmi_tx_se0 USB2 Phy UTMI force: TX_SE0 value	R/W	0
9	VSEC_USB_PAPB_UTMI_CFG	16	pb_frc_utmi_en USB2 Phy UTMI force: forces various UTMI signals (instead of their value from xHC)	R/W	0
9	VSEC_USB_PAPB_UTMI_CFG	18	pb_frc_utmi_auxreset_b USB2 Phy UTMI force: RESET value	R/W	0
9	VSEC_USB_PAPB_UTMI_CFG	19	pb_frc_utmi_dmpulldown USB2 Phy UTMI force: DMPULLDOWN value	R/W	0
9	VSEC_USB_PAPB_UTMI_CFG	20	pb_frc_utmi_dppulldown USB2 Phy UTMI force: DPPULLDOWN value	R/W	0
9	VSEC_USB_PAPB_UTMI_CFG	21	pb_frc_utmi_termselect USB2 Phy UTMI force: TERMSELECT value	R/W	0
9	VSEC_USB_PAPB_UTMI_CFG	23:22	pb_frc_utmi_opmode USB2 Phy UTMI force: OPMODE value	R/W	0
9	VSEC_USB_PAPB_UTMI_CFG	25:24	pb_frc_utmi_xcvrselect USB2 Phy UTMI force: XCVRSELECT value	R/W	0
9	VSEC_USB_PAPB_UTMI_CFG	26	pb_frc_utmi_l1_en USB2 Phy UTMI force: L1_EN value	R/W	0
9	VSEC_USB_PAPB_UTMI_CFG	27	pb_frc_utmi_suspendm USB2 Phy UTMI force: SUSPENDM value	R/W	0
9	VSEC_USB_PAPB_UTMI_CFG	28	pb_frc_utmi_fslsserialmode USB2 Phy UTMI force: FSLSSERIALMODE value	R/W	0
9	VSEC_USB_PAPB_UTMI_CFG	29	pb_frc_utmi_tx_dat USB2 Phy UTMI force: TX_DAT value	R/W	0
9	VSEC_USB_PAPB_UTMI_CFG	30	pb_frc_utmi_tx_enable_n USB2 Phy UTMI force: TX_ENABLE_N value	R/W	0
9	VSEC_USB_PAPB_UTMI_CFG	31	pb_frc_utmi_tx_se0 USB2 Phy UTMI force: TX_SE0 value	R/W	0
10	VSEC_USB_ECC_STS	31:0	ECC ECC error status of various xHC RAM's	R/Clr	0
11	VSEC_USB3_GEN2_LPBK_ERR_CNT	31:0	gen2_lpbk_err_cnt USB3 Gen2 Loopback error counter	R/Clr	0

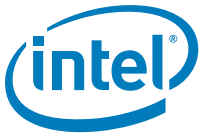


Table 45. USB Vendor-Specific Capability Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
12	VSEC_USB3_GEN1_LPBK_ERR_CNT	15:0	bert_remote_err_cnt_wide[15:0] USB3 Gen1 Remote Loopback error counter [15:0] (valid in master lopoback mode)	R/Clr	0
12	VSEC_USB3_GEN1_LPBK_ERR_CNT	31:16	bert_local_err_cnt_wide[15:0] USB3 Gen1 Local Loopback error counter [15:0] (valid in master and slave lopoback modes)	R/Clr	0
13	VSEC_USB3_GEN1_LPBK_ERR_CNT	15:0	bert_remote_err_cnt_wide[31:16] USB3 Gen1 Remote Loopback error counter [31:16] (valid in master lopoback mode)	R/Clr	0
13	VSEC_USB3_GEN1_LPBK_ERR_CNT	31:16	bert_local_err_cnt_wide[31:16] USB3 Gen1 Local Loopback error counter [31:16] (valid in master and slave loopoback modes)	R/Clr	0
14	VSEC_USB2_PRBS_ERR_CNT	14:0	pa_prbs_err_cnt USB2: PRBS error counter	R/Clr	0
14	VSEC_USB2_PRBS_ERR_CNT	15	pa_prbs_lock USB2: PRBS pattern found/locked	RO	0
14	VSEC_USB2_PRBS_ERR_CNT	30:16	pb_prbs_err_cnt USB2: PRBS error counter	R/Clr	0
14	VSEC_USB2_PRBS_ERR_CNT	31	pb_prbs_lock USB2: PRBS pattern found/locked	RO	0
15	VSEC_USB_TOP_STS0	31:0	Reserved	RO	0
16	VSEC_USB_TOP_STS1	0	ux_pmc_smi SMI status	RO	0
16	VSEC_USB_TOP_CFG0	5:0	cfg_wait_period_2start_eq Indicates the amount of time (in resolution of 16us) to verify there is no lfps or equalization duration before Rx high-speed is enabled (i.e. rx_eidle is de-asserted)	R/W	4
16	VSEC_USB_TOP_CFG0	7:6	cfg_min_lfps_absence_during_recov Indicates the amount of time (in resolution of 16us) to verify there is no lfps during recovery	R/W	0
16	VSEC_USB_TOP_CFG0	8	cfg_wait4_no_eq_done_before_Px Wait for cio_usb_rx_eq_done to go down before the transition to P1/P2/P3 is accomplished	R/W	0
16	VSEC_USB_TOP_CFG0	9	cfg_cnt_rx_eq_dur If set, usec_timer takes into account the time passed since Rx equalization activation	R/W	1

Table 45. USB Vendor-Specific Capability Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
16	VSEC_USB_TOP_CFG0	10	cfg_ignore_tx_lfps_in_progress If set, tx_lfps_in_progress is not taken into account in order to enter tx electrical idle	R/W	0
16	VSEC_USB_TOP_CFG0	11	cfg_cnt_no_tx_lfps_during_eq If set, usec_timer takes into account tx_lfps absence duration	R/W	0
16	VSEC_USB_TOP_CFG0	12	cfg_cnt_no_rx_lfps_during_eq If set, usec_timer takes into account rx_lfps_ser_det absence duration	R/W	0
16	VSEC_USB_TOP_CFG0	13	cfg_rxdis_in_p2 Enables de-assertion of usb_rx_enable in P2	R/W	0
16	VSEC_USB_TOP_CFG0	14	cfg_use_pls_for_recov_det Indicates that pipe3_pls should be used to deduce Recovery state instead of pipe3_Recov	R/W	0
16	VSEC_USB_TOP_CFG0	15	cfg_rx_recal_en Enable recal_req/recal_done management by the FW	R/W	0
16	VSEC_USB_TOP_CFG0	19:16	cfg_tx_frc_precharge_dur Duration of Tx lane precharge to Vdd/2 in resolution of 16us	R/W	9
16	VSEC_USB_TOP_CFG0	20	cfg_tx_frc_precharge_dis Disables precharge of Tx lane to Vdd/2 during transitions from P2/P3 to P0	R/W	0
16	VSEC_USB_TOP_CFG0	21	cfg_terminate_rxdet_on_u2_exit When set, u2_exit_cond_met will cause to reply RCV_PRESENT during RxDet flow without waiting for its termination	R/W	1
16	VSEC_USB_TOP_CFG0	22	cfg_use_rxstandby_en Use pipe3_RxStandb	R/W	0
16	VSEC_USB_TOP_CFG0	23	cfg_precise_tx_eidle_in_p0_en When set, usb_tx_eidle in P0 is controlled directly by the logic in car_usb_phy_clk domain which is much more informed about the state of Tx LFPS	R/W	1
16	VSEC_USB_TOP_CFG0	24	cfg_frc_rxlfpsen_in_p0 When set, Rx LFPS monitoring is enabled automatically in P0	R/W	1

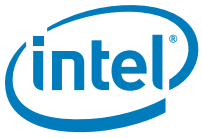


Table 45. USB Vendor-Specific Capability Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
17	VSEC_USB_TOP_CFG1	7:0	cfg_ser_lfps_trans_max_dur Defines the maximal time duration it takes LFPS to toggle, i.e. more than that period will invalidate the signal	R/W	3
17	VSEC_USB_TOP_CFG1	15:8	cfg_ser_lfps_elec_idle_min_dur Defines for how long no signal should be detected in order to deduce electrical idle	R/W	5
17	VSEC_USB_TOP_CFG1	23:16	cfg_ser_lfps_non_elec_idle_min_dur Defines what signal duration during electrical idle should be considered as a noise	R/W	0
17	VSEC_USB_TOP_CFG1	24	cfg_ser_lfps_limit_max_lfps_en Indicates validity of lfps_max_half_period_dur	R/W	1
17	VSEC_USB_TOP_CFG1	25	cfg_frc_uxb_uxp_actvreq Force value on uxb_uxp_actvreq	R/W	0
17	VSEC_USB_TOP_CFG1	26	cfg_frc_uxb_uxp_actvreq_val Value forced on uxb_uxp_actvreq when cfg_frc_uxb_uxp_actvreq is set	R/W	0
17	VSEC_USB_TOP_CFG1	27	cfg_dont_idle_on_prim_ckreq When set to '1', ux_prim_ckreq should cancel idleness	R/W	0
17	VSEC_USB_TOP_CFG1	29:28	cfg_tx_lfps_ip_dly Defines how much u3digphy_tx_lfps_in_progress is stretched in the end of Tx LFPS transmission - it influences activation of usb_tx_eidle	R/W	0
17	VSEC_USB_TOP_CFG1	30	cfg_single_dn_pkt_burst_pcie_gen3_en If set, uhost gasket will buffer all EMEP->USB traffic to prevent bubbles in rx_data_valid (_dput)	R/W	0
17	VSEC_USB_TOP_CFG1	31	cfg_ushost_p_dget_by_davail_en If set, uhost gasket will use uxp_uxb_ushost_p_davail indication to decide when to assert _dget for upstream posted data	R/W	0
18	VSEC_USB_TOP_CFG2	7:0	cfg_ser_lfps_lfps_max_half_period_dur If the same signal state lasted for more than this period of time and limit_max_lfps_en is set, lfps_det will be de-asserted	R/W	40

Table 45. USB Vendor-Specific Capability Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
18	VSEC_USB_TOP_CFG2	15:8	cfg_ser_lfps_lfps_min_half_period_dur If the same signal state lasted for less than this period of time, lfps_det will be de-asserted	R/W	4
18	VSEC_USB_TOP_CFG2	23:16	cfg_ser_lfps_max_high_speed_sig_dur The same signal that lasts for more than this period of time will set lfps_det	R/W	6
18	VSEC_USB_TOP_CFG2	31:24	cfg_ser_lfps_start_sig_min_dur Defines for how much time the signal should be detected to consider it as a valid signal	R/W	4
19	VSEC_USB_TOP_CFG3	4:0	cfg_par_min_lfps_fragment_gen2 0's burst length or 1's burst length that indicates parallel LFPS detection (gen2)	R/W	31
19	VSEC_USB_TOP_CFG3	9:5	cfg_par_min_lfps_fragment_gen1 0's burst length or 1's burst length that indicates parallel LFPS detection (gen1)	R/W	31
19	VSEC_USB_TOP_CFG3	10	cfg_last_tx_lfps_phase_zero_only If set, the last Tx LFPS must terminated with 0's. (otherwise can be any)	R/W	0
19	VSEC_USB_TOP_CFG3	11	cfg_corrupt_single_skp_en when set, if a single SKP is detected without repair (non-loopback mode), then substitute it to SUB	R/W	1
19	VSEC_USB_TOP_CFG3	12	cfg_skp_rep_en when set, if a skp and almost SKP is detected, then treat almost-SKP as SKP	R/W	1
19	VSEC_USB_TOP_CFG3	13	cfg_realign_in_lpbk_dis when set, and loopback mode, disable comma realignment	R/W	1
19	VSEC_USB_TOP_CFG3	14	cfg_eb_mode_gen2 Gen2 Elasticity Buffer Mode; 0-HalfFull Mode, 1- Empty Mode	R/W	0
19	VSEC_USB_TOP_CFG3	15	cfg_eb_mode_gen1 Gen1 Elasticity Buffer Mode; 0-HalfFull Mode, 1- Empty Mode	R/W	0
19	VSEC_USB_TOP_CFG3	19:16	cfg_par_lfps_trans_max_dur Defines the number of rx_clk cycles without low speed signal detection that will cause to u3digphy_rx_lfps_par_det de-assertion	R/W	2
19	VSEC_USB_TOP_CFG3	22:20	cfg_tx_lfps_stop_ahead_gen2 Defines the number of tx_clk cycles to start wraping up Tx LFPS before termination of the current tPeriod (in gen2 mode)	R/W	0

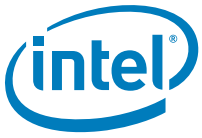


Table 45. USB Vendor-Specific Capability Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
19	VSEC_USB_TOP_CFG3	25:23	cfg_tx_lfps_stop_ahead_gen1 Defines the number of tx_clk cycles to start wraping up Tx LFPS before termination of the current tPeriod (in gen1 mode)	R/W	0
19	VSEC_USB_TOP_CFG3	28:26	cfg_tx_num_of_stages_in_ana Defines the depth of the tx data path in Tx transmitter, i.e. the number of 32b data sampling stages	R/W	4
19	VSEC_USB_TOP_CFG3	31:29	cfg_tx_lfps_period Defines half LFPS tPeriod in resolution of 6.4ns	R/W	4
20	VSEC_USB_TOP_CFG4	3:0	cfg_idle_to_emep_delay_count	R/W	0
20	VSEC_USB_TOP_CFG4	7:4	cfg_prim_clk_delay_count	R/W	0
20	VSEC_USB_TOP_CFG4	8	cfg_frc_side_clkreq_en Force side_clkreq to '1'	R/W	0
20	VSEC_USB_TOP_CFG4	9	cfg_frc_prim_clkreq_en Force uxp_uxb_ckreq to '1'	R/W	0
20	VSEC_USB_TOP_CFG4	10	cfg_fismpdfx_force_clkreq	R/W	0
20	VSEC_USB_TOP_CFG4	11	cfg_fismpdfx_clkgate_ovrd	R/W	0
20	VSEC_USB_TOP_CFG4	12	cfg_gasket_byte_swap_en	R/W	0
20	VSEC_USB_TOP_CFG4	16	cfg_pa_utmi_prbs_gen_en PA USB2: enable PRBS7 generation on Tx	R/W	0
20	VSEC_USB_TOP_CFG4	17	cfg_pa_utmi_prbs_chk_en PA USB2: enable PRBS7 check on Rx	R/W	0
20	VSEC_USB_TOP_CFG4	18	cfg_pb_utmi_prbs_gen_en PB USB2: enable PRBS7 generation on Tx	R/W	0
20	VSEC_USB_TOP_CFG4	19	cfg_pb_utmi_prbs_chk_en PB USB2: enable PRBS7 check on Rx	R/W	0
20	VSEC_USB_TOP_CFG4	22:20	cfg_gen1_err_ignore Masks Gen1 errors that shouldn't be communicated over usb_rx_error_detected_tog	R/W	0
20	VSEC_USB_TOP_CFG4	25:23	cfg_gen2_err_ignore Masks Gen2 errors that shouldn't be communicated over usb_rx_error_detected_tog	R/W	0
20	VSEC_USB_TOP_CFG4	30:28	cfg_ecc_info_sel Select ECC info to be read from VSEC_USB_ECC_STS	R/W	0
20	VSEC_USB_TOP_CFG4	31	cfg_func_ecc_enable ECC enable	R/W	0

Table 45. USB Vendor-Specific Capability Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
21	VSEC_USB_TOP_CFG5	15:0	cfg_berc2berc_len Defines the number of tx_clk cycles between any two BERC transmissions	R/W	0x8000
21	VSEC_USB_TOP_CFG5	23:16	cfg_brst_period Defines after how many BERC's need to send BRST	R/W	0x10
21	VSEC_USB_TOP_CFG5	31:24	cfg_bert_skp_period Defines the number of tx_clk cycles between any two SKP set (4 SKP symbols) transmissions in master loopback mode (i.e. BERT)	R/W	0x80
22	VSEC_USB_TOP_CFG6	1:0	cfg_tx_master_lpbk_en Enables Tx master loopback mode per port	R/W	0
22	VSEC_USB_TOP_CFG6	3:2	cfg_rx_master_lpbk_en Enables Rx master loopback mode per port	R/W	0
22	VSEC_USB_TOP_CFG6	11:4	cfg_gen2_lpbk_skp_period Defines the number of tx_clk cycles between any two SKP_OS transmissions in master loopback mode (gen2)	R/W	32
22	VSEC_USB_TOP_CFG6	12	cfg_master_lpbk_sds If set, gen2_lpbk_err_cnt is cleared on SDS_OS reception	R/W	1
22	VSEC_USB_TOP_CFG6	25:16	cfg_usb2_prbs_pkt_size Size of the packet that contains PRBS fragment (0 means 1 Byte)	R/W	0
22	VSEC_USB_TOP_CFG6	30:26	cfg_usb2_prbs_ipg IPG between packets that carry PRBS fragments (in resolution of 8 utmi cycles; 0 means that PRBS is not packetized and sent continuously)	R/W	0
22	VSEC_USB_TOP_CFG6	31	cfg_prbs_err_cnt_res Resolution of prbs_err_cnt: 0/1 - bits/Bytes	R/W	0
23	VSEC_USB_TOP_CFG7	1:0	cfg_dtfus_usb3portcfg Defines the number of usb3 ports that should be subtracted from the actual number (which is 2) before being advertised in the capabilities to the SW	R/W	0
23	VSEC_USB_TOP_CFG7	3:2	cfg_dtfus_usb2portcfg Defines the number of usb2 ports that should be subtracted from the actual number (which is 2) before being advertised in the capabilities to the SW	R/W	0

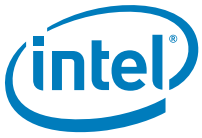


Table 45. USB Vendor-Specific Capability Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
23	VSEC_USB_TOP_CFG7	4	cfg_dtfus_valid In order to have cfg_dtfus_usb2portcfg/ cfg_dtfus_usb3portcfg be taken into account this signal should be de-asserrted and re-asserted back	R/W	1
23	VSEC_USB_TOP_CFG7	7:5	cfg_txoneszeros_len Defines the number of ones/zeros in CP7/ CP8 compliance pattern in resolution of 32b: 0 = 32b, ..., 7 = 256b	R/W	1
23	VSEC_USB_TOP_CFG7	9:8	cfg_frc_rx_dis_pre If set, Rx data path is disabled	R/W	0
23	VSEC_USB_TOP_CFG7	11:10	cfg_frc_tx_dis_pre If set, Tx data path is disabled	R/W	0
23	VSEC_USB_TOP_CFG7	13:12	cfg_frc_realign_pulse A pulse that causes Gen1/Gen2 Rx data path to re-align symbol/block	R/W	0
23	VSEC_USB_TOP_CFG7	15:14	cfg_frc_gen2_align_en_pre If set, align_en of Gen2 Rx data path is enabled, otherwise it depends on BlockAlignControl from MAC	R/W	0
23	VSEC_USB_TOP_CFG7	17:16	cfg_frc_gen1_align_en_pre If set, align_en of Gen1 Rx data path is enabled	R/W	3
23	VSEC_USB_TOP_CFG7	18	cfg_lfps_ser_det_mode Selects between two implementations of serial LFPS detection	R/W	0
23	VSEC_USB_TOP_CFG7	31:30	io_ux_cfg_port_select If cleared, the port works in legacy (i.e. Gen1) mode. Can be changed only while disconnected	R/W	3
23	VSEC_USB_TOP_CFG6	31	cfg_prbs_err_cnt_res Resolution of prbs_err_cnt: 0/1 - bits/Bytes	R/W	0
24	VSEC_USB_TOP_CFG7	1:0	cfg_dtfus_usb3portcfg Defines the number of usb3 ports that should be subtracted from the actual number (which is 2) before being advertised in the capabilities to the SW	R/W	0
24	VSEC_USB_TOP_CFG7	3:2	cfg_dtfus_usb2portcfg Defines the number of usb2 ports that should be subtracted from the actual number (which is 2) before being advertised in the capabilities to the SW	R/W	0

Table 45. USB Vendor-Specific Capability Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
24	VSEC_USB_TOP_CFG7	4	cfg_dtfus_valid In order to have cfg_dtfus_usb2portcfg/ cfg_dtfus_usb3portcfg be taken into account this signal should be de-asserrted and re-asserted back	R/W	1
24	VSEC_USB_TOP_CFG7	7:5	cfg_txoneszeros_len Defines the number of ones/zeros in CP7/ CP8 compliance pattern in resolution of 32b: 0 = 32b, ..., 7 = 256b	R/W	1
24	VSEC_USB_TOP_CFG7	9:8	cfg_frc_rx_dis_pre If set, Rx data path is disabled	R/W	0
24	VSEC_USB_TOP_CFG7	11:10	cfg_frc_tx_dis_pre If set, Tx data path is disabled	R/W	0
24	VSEC_USB_TOP_CFG7	13:12	cfg_frc_realign_pulse A pulse that causes Gen1/Gen2 Rx data path to re-align symbol/block	R/W	0
24	VSEC_USB_TOP_CFG7	15:14	cfg_frc_gen2_align_en_pre If set, align_en of Gen2 Rx data path is enabled, otherwise it depends on BlockAlignControl from MAC	R/W	0
24	VSEC_USB_TOP_CFG7	17:16	cfg_frc_gen1_align_en_pre If set, align_en of Gen1 Rx data path is enabled	R/W	3
24	VSEC_USB_TOP_CFG7	18	cfg_lfps_ser_det_mode Selects between two implementations of serial LFPS detection	R/W	0
24	VSEC_USB_TOP_CFG7	31:30	io_ux_cfg_port_select If cleared, the port works in legacy (i.e. Gen1) mode. Can be changed only while disconnected	R/W	3

4.3.2 Port Configuration Space

Figure 23 shows the port configuration space registers that must be implemented by every CIO Switch port. The port configuration space has a total of 256 double words.

The first nine double words describe the basic attributes of a CIO Switch port. The remaining 248 double words are organized into a linked list of optional or required capability structures. The required capabilities include Time Management, Power Management and Physical Layer configuration registers.

Vendor specific and Adapter capability structures are optional.

Figure 23. Port Configuration Space

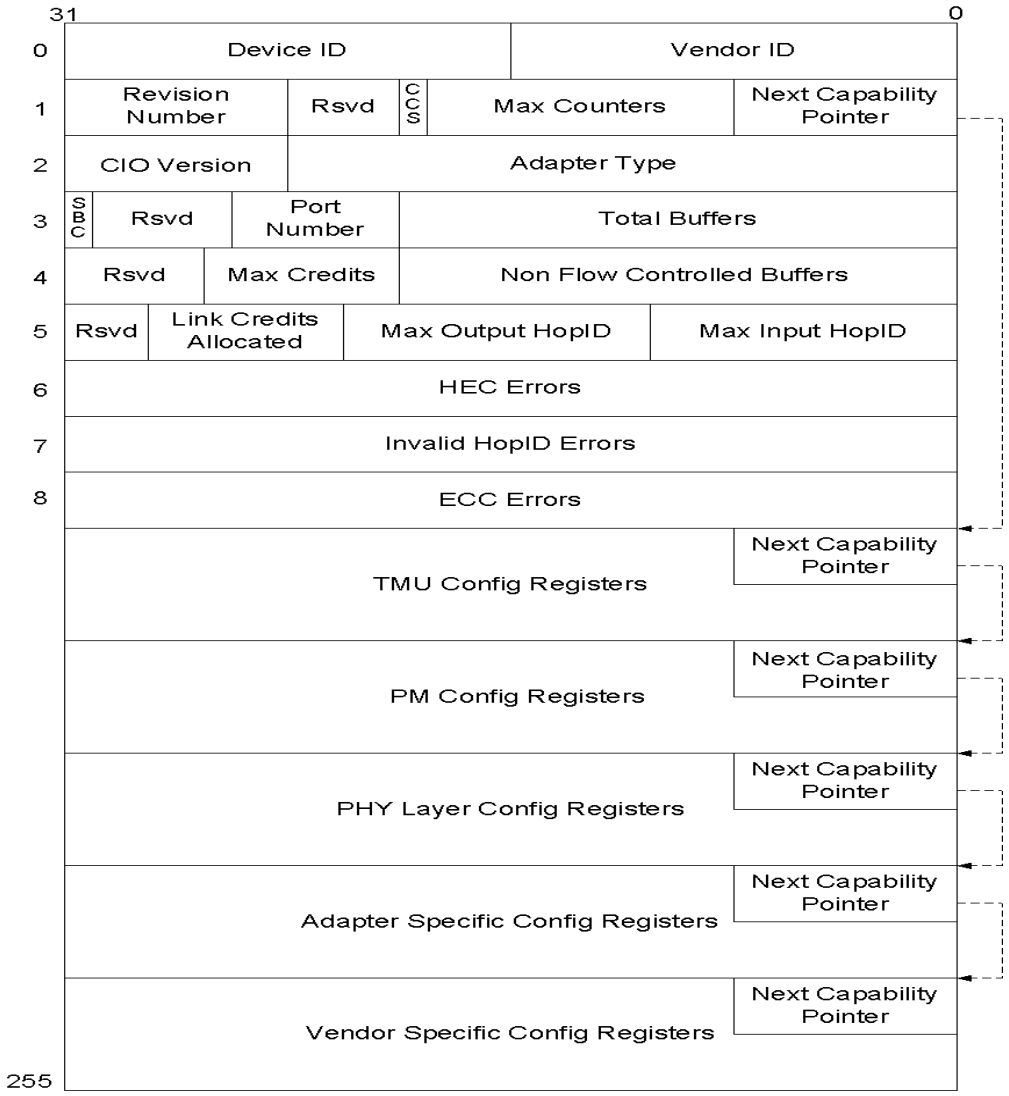


Table 46 specifies the next capability pointers of the port configuration space for the different port types.

Table 46. Next Capability Pointers for Port Configuration Space

Pointer Number	Pointer Name	Pointer Value	Comments
1	PORT_TMU_BASE	0xA	
3	PORT_PHY_BASE	0x36	
4	PORT_ADP_BASE	0x39	
5	PORT_VSEC_BASE	0x4F for DP Ports 0x3E for other ports	src_pA, src_pB vsec in ports 9,10 respectively
6	PORT_VSEC_BASE	0x8F available in ports 9,10 only	sink_1, sink_2 vsec in ports 9,10 respectively

4.3.2.1 Basic Configuration

The basic attributes of the port configuration space registers are described in Table 47.

Table 47. Port Configuration Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	PORT_CS_0	15:0	Vendor ID This field identifies the manufacturer of the device.	R/W	0x8086
0	PORT_CS_0	31:16	Device ID This field is assigned by the manufacturer and identifies the type of the device.	R/W	0x1578
1	PORT_CS_1	7:0	Next Capability Pointer This field defines the doubleword index of the first capability register set in the port configuration space.	RO	CIO–See pointer#1 (TMU) CTRL/ DMA-0 DPout – See pointer#3 DPin/PCIe–See pointer#4 (ADP)
1	PORT_CS_1	18:8	Max Counters This field specifies the maximum number of performance counters implemented by the port.	RO	DP–2 PCIe–2 CIO/DMA–16 CTRL–8
1	PORT_CS_1	19	Counter Configuration Space (CCS) Flag This flag indicates if the port supports the counter configuration space.	RO	1

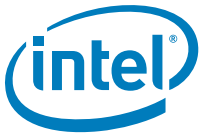


Table 47. Port Configuration Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
1	PORT_CS_1	23:20	Reserved Must be set to 0.	RO	0
1	PORT_CS_1	31:24	Revision Number This value is assigned by the manufacturer and identifies the revision number of the device.	RO	0
2	PORT_CS_2	23:0	Adapter Type This field identifies the native protocol implemented by the Adapter connected to the Switch port. The information is contained in three bytes with the names BaseClass, SubClass, and Protocol.	RO	See Table 48
2	PORT_CS_2	31:24	reserved	RO	1
3	PORT_CS_3	19:0	Total Buffers This field specifies the total buffer space available at the port in number of credit units (1 packet).	RO	CIO–60 DP_IN-16 DMA-16 Others-8
3	PORT_CS_3	25:20	Port Number This register specifies the CIO Switch port number for the port.	RO	See Table 48
3	PORT_CS_3	30:26	Reserved Must be set to 0.	RO	0
3	PORT_CS_3	31	Shared Buffering Capable This capability bit indicates if the port is capable of sharing the port's flow control buffer among the flow controlled paths. This bit is set to 0 if shared buffering is not implemented. If this bit is set to 1, the total shared buffer space is given by the Total Buffers minus Non Flow Controlled Buffers minus buffers allocated to paths using dedicated buffering.	RO	1
4	PORT_CS_4	19:0	Non Flow Controlled Buffers This register specifies the number of buffers set aside for use by non flow controlled paths out of the total buffer space available at the port. All non flow controlled paths at the port share this buffer space.	R/W	0
4	PORT_CS_4	26:20	Max Credits This field specifies the maximum value of the Credits Allocated field (in credit units) supported by the port for a path.	RO	CIO–60 Others-8
4	PORT_CS_4	31:27	Reserved Must be set to 0.	RO	0

Table 47. Port Configuration Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
5	PORT_CS_5	10:0	Max Input HopID This field specifies the maximum HopID value the port can support on receive. The maximum number of paths that can be supported on receive is given by (Max Input HopID + 1).	RO	CIO-15 DMA-11 CTRL–7 PCIe–8 DP-9
5	PORT_CS_5	21:11	Max Output HopID This field specifies the maximum HopID value the port can support on transmit. The maximum paths number of paths that can be supported on transmit is given by (Max Output HopID + 1).	RO	CIO-15 DMA-11 CTRL–7 PCIe–8 DP-9
5	PORT_CS_5	28:22	Link Credits Allocated This field specifies the initial value of the Link Credits Allocated field to be used by the receiver side of the link.	R/W	CTRL–7 Others-0
5	PORT_CS_5	31:29	Reserved Must be set to 0.	RO	0
6	PORT_CS_6	31:0	HEC Errors This field contains a count of the number of CIO packets dropped on account of HEC errors. The counter value increments from 0 and saturates at 0xFFFFFFFF. Software can write to this field to clear the counter value to 0.	W/Clr	0
7	PORT_CS_7	31:0	Invalid HopID Errors This field contains a count of the number of CIO packets received with an un-initialized HopID. The counter increments from 0 and saturates at 0xFFFFFFFF. Software can write to this field to clear the counter value to 0.	W/Clr	0
8	PORT_CS_8	31:0	ECC Errors This register contains a count of the number of CIO packets dropped on account of ECC errors. The counter value increments from 0 and saturates at 0xFFFFFFFF. Software can write to this register to clear the counter value to 0.	W/Clr	0

Table 48. Defined Adapter Type and Port Number Values

Port #	Kind	Meaning	Base-Class	Sub-Class	Protocol
0	Control Port	Port does not contain an Adapter	00h	00h	01h
1	CIO null adapter 0	Port does not contain an Adapter	00h	00h	01h
2	CIO null adapter 1	Port does not contain an Adapter	00h	00h	01h
3	CIO null adapter 2	Port does not contain an Adapter	00h	00h	01h
4	CIO null adapter 3	Port does not contain an Adapter	00h	00h	01h
5	DMA	Host Interface Adapter	00h	00h	02h
6	PCIe adapter 0	PCIe Downstream/Upstream Adapter	10h	01h	01h/02h[1]
7	PCIe adapter 1	PCIe Downstream Adapter	10h	01h	01h

Table 48. Defined Adapter Type and Port Number Values (Continued)

Port #	Kind	Meaning	Base-Class	Sub-Class	Protocol
8	DP OUT adapter	DisplayPort out Adapter.	0Eh	01h	04h
9	DP IN adapter 0	DisplayPort In Adapter.	0Eh	01h	03h
10	DP IN adapter 1	DisplayPort In Adapter.	0Eh	01h	03h
11	DP OUT adapter	DisplayPort out Adapter.	0Eh	01h	04h

1.01h Host Router, 02h if Endpoint.

4.3.2.2 TMU Configuration

In Alpine-Ridge DP the Time Sync registers exist in the CIO and DPout ports only.

Note: The register offset is relative to PORT_TMU_BASE in Table 49.

4.3.2.2.1 CIO Null Port

Figure 24 shows the configuration registers in the device configuration space for the Time Sync capability register set. The register attributes are described in Table 49.

Figure 24. Time Sync Port Configuration Space Registers

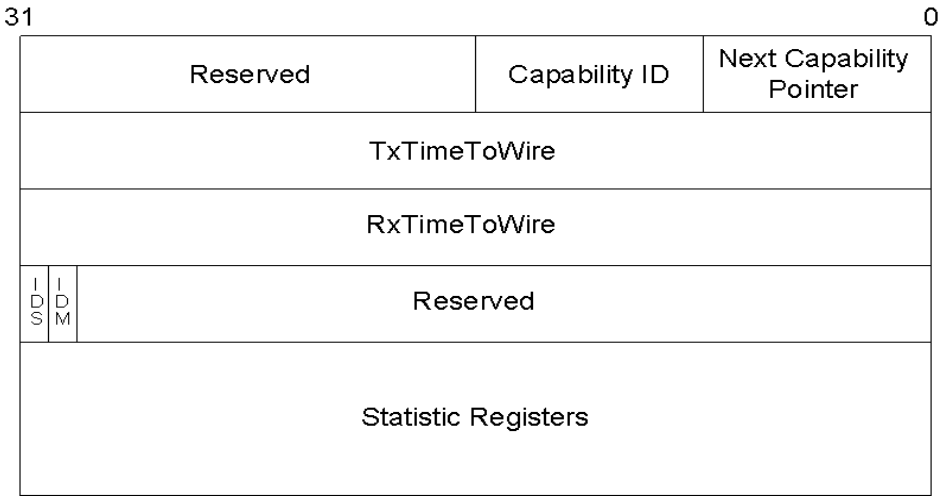


Table 49. Time Sync Port Configuration Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	TMU_PORT_CS_0	7:0	Next Capability Pointer This field defines the doubleword index of the next capability register set in the port configuration space. It is set to 00h if this is the last register set in port configuration space.	RO	CIO
0	TMU_PORT_CS_0	15:8	Capability ID This field must contain the value 03h indicating this is the start of the Time Sync capability register set.	RO	3

Table 49. Time Sync Port Configuration Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	TMU_PORT_CS_0	31:16	Reserved Must be set to 0.	RO	0
1	TMU_PORT_CS_1	31:0	TxTimeToWire This field specifies the time duration from the instant the timestamp is taken at the physical layer to the instant when the first bit of the TSNOS is transmitted on the wire. The time is specified in nanoseconds multiplied by 2^{16}. For example, 2.5ns is represented as 0x000000028000. Loaded from FLASH (see FLASH map, bytes 0x20-0x27	RO	0x00240000
2	TMU_PORT_CS_2	31:0	RxTimeToWire This field specifies the time duration from the instant the first bit of the TSNOS is received at the wire to the instant when the timestamp is taken at the physical layer. The time is specified in nanoseconds multiplied by 2^{16}. For example, 2.5ns is represented as 0x000000028000. Loaded from FLASH (see FLASH map, bytes 0x28-0x2F)	RO	0x002E0000
3	TMU_PORT_CS_3	29:0	Reserved; Must be set to 0.	RO	0
3	TMU_PORT_CS_3	30	Inter-domain Master (IDM) This bit must be set to 1 if the domain is configured as an inter-domain master domain and inter-domain Time Sync packet exchange must be enabled on this port. On reset, this bit must default to 0.	R/W	0
3	TMU_PORT_CS_3	31	Inter-domain Slave (IDS) This bit must be set to 1 if the domain is configured as an inter-domain slave domain and inter-domain Time Sync packet exchange must be enabled on this port. On reset, this bit must default to 0.	R/W	0
4	TMU_PORT_CS_4	15:0	RX TSNOS counter Statistics counter that counts the number of TSNOS received by TMU. The counter gets stuck on 65535. Clears itself on read.	R/Clr	0
4	TMU_PORT_CS_4	31:16	TX TSNOS counter Statistics counter that counts the number of TSNOS sent by TMU. The counter gets stuck on 65535. Clears itself on read.	R/Clr	0
5	TMU_PORT_CS_5	15:0	RX Packet counter Statistics counter that counts the number of TMU packets received by TMU. The counter gets stuck on 65535. Clears itself on read.	R/Clr	0
5	TMU_PORT_CS_5	31:16	TX Packet counter Statistics counter that counts the number of TMU packets sent by TMU. The counter gets stuck on 65535. Clears itself on read.	R/Clr	0

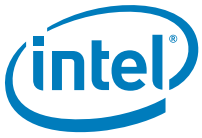


Table 49. Time Sync Port Configuration Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
6	TMU_PORT_CS_6	0	Ignore RX CRC If set to 1 then CRC integrity on RX TMU packets will not be checked.	R/W	0
6	TMU_PORT_CS_6	1	Disable Time sync If set to 1 this port will not initiate time sync requests.	R/W	0
6	TMU_PORT_CS_6	31:2	Reserved	RSV	0
7	TMU_PORT_CS_7	9:0	Lost OS Counter Statistics counter that counts the number of occurrences when OS was not returned by time sync master. Gets stuck on 1023. Cleared on read.	R/Clr	0
7	TMU_PORT_CS_7	19:10	Lost Pkt Counter Statistics counter that counts the number of occurrences when Follow-up packet was not returned by time sync master. Gets stuck on 1023. Cleared on read.	R/Clr	0
7	TMU_PORT_CS_7	29:20	Bad Pkt Counter Statistics counter that counts the number of TMU packets with bad CRC. Gets stuck on 1023. Cleared on read.	R/Clr	0
7	TMU_PORT_CS_7	31:30	Reserved	RSV	0
8	TMU_PORT_CS_8	2:0	Slave FSM state	R/W	0
8	TMU_PORT_CS_8	5:3	Send FSM state	RW	0
8	TMU_PORT_CS_8	6	Force Slave FSM state	R/W	0
8	TMU_PORT_CS_8	7	Force Send FSM state	R/W	0
8	TMU_PORT_CS_8	31:8	Reserved	RSV	0

4.3.2.2.2 Display Port (DP) OUT

The DP Out TMU capability registers are for internal use only.

The attributes of the DP out TMU capability registers are described in Table 50.

Table 50. DP out TMU Configuration Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	TMU_DP_CS_0	7:0	Next Capability Pointer This field defines the doubleword index of the next capability register set in the port configuration space. It is set to 00h if the Time Sync configuration register set is the final register set in the linked list of capability register sets in the port configuration space.	RO	0x39
0	TMU_DP_CS_0	15:8	Capability ID This field must contain the value 03h indicating this is the start of the Time Sync capability register set.	RO	3
0	TMU_DP_CS_0	19:16	Gain FBS Low.	R/W	0
0	TMU_DP_CS_0	23:20	Gain FBS High.	R/W	0

Table 50. DP out TMU Configuration Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	TMU_DP_CS_0	30:24	Reserved	RSV	0
0	TMU_DP_CS_0	31	Enable uC Modulator Switch from default modulator to uC modulator.	R/W	0
1	TMU_DP_CS_1	7:0	Filter Strength Power of 2 of LPF filter strength. A=2^P.	R/W	5
1	TMU_DP_CS_1	11:8	Loop Gain Rough	R/W	0
1	TMU_DP_CS_1	15:12	Loop Gain Fine	R/W	0
1	TMU_DP_CS_1	19:16	Loop Atten Rough	R/W	1
1	TMU_DP_CS_1	23:20	Loop Atten Fine	R/W	1
1	TMU_DP_CS_1	24	Turn Off Rough High	R/W	0
1	TMU_DP_CS_1	25	Turn Off Rough Low	R/W	0
1	TMU_DP_CS_1	26	Turn Off Fine High	R/W	0
1	TMU_DP_CS_1	27	Turn Off Fine Low	R/W	0
1	TMU_DP_CS_1	29:28	Reserved	RO	0
1	TMU_DP_CS_1	30	Disable Modulator Disable all LS modulations.	R/W	1
1	TMU_DP_CS_1	31	Reserved	RO	0
2	TMU_DP_CS_2	31:0	CMD to uC modulator	R/W	0
3	TMU_DP_CS_3	31:0	DATA to uC modulator	R/W	0
4	TMU_DP_CS_4	31:0	DATA from uC modulator	RO	0xFFFFFFFF
5	TMU_DP_CS_5	31:0	Reserved	RO	0
6	TMU_DP_CS_6	15:0	SSC PPM Shift Shift in PPM in case SSC is enabled in DP_IN.	R/W	2500
6	TMU_DP_CS_6	31:16	Reserved	RO	0
7	TMU_DP_CS_7	7:0	SSC Step Size Step size of default modulator.	R/W	2
7	TMU_DP_CS_7	15:8	Reserved	RO	0
7	TMU_DP_CS_7	23:16	SSC Amplitude Amplitude of default modulator.	R/W	200
7	TMU_DP_CS_7	31:24	Reserved	RO	0
8	TMU_DP_CS_8	14:0	PLL Param PLL frequency can be changed by SW. Writing to this register will cause PLL frequency to change to. Param Default=10,000 (1GHz). Param Min=0 (99.0464Mhz), Param Max=20,000(1.009536Ghz). 1 step is 0.9536ppm of the main frequency.	R/W	0

Table 50. DP out TMU Configuration Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
8	TMU_DP_CS_8	15	PLL Direction PLL SW change can be relative to current value. This bit states the direction: 1 - step up, 0 - step down. Relevant only if bit16 of this register is 1.	R/W	0
8	TMU_DP_CS_8	16	PLL Change Relative/Absolute PLL SW change relative or absolute: 0 - PLL Param is taken as is, 1 - PLL Param is taken relative to previous value depending on PLL change direction.	R/W	0
8	TMU_DP_CS_8	31:17	Reserved	RO	0
9	TMU_DP_CS_9	15:0	Max Fix Amplitude Max amplitude of PPM fix.	R/W	6000
9	TMU_DP_CS_9	31:16	Reserved	RO	0

4.3.2.3 PHY Configuration

Figure 25 shows the Physical Layer Logical Block port configuration space registers that must be implemented by every CIO Switch port. The registers are described in Table 51. In Alpine-Ridge DP the Physical Layer registers exist in the CIO ports only.

Note: The register offset is relative to PORT_PHY_BASE in Table 46.

Figure 25. Physical Layer Logical Block Configuration Registers

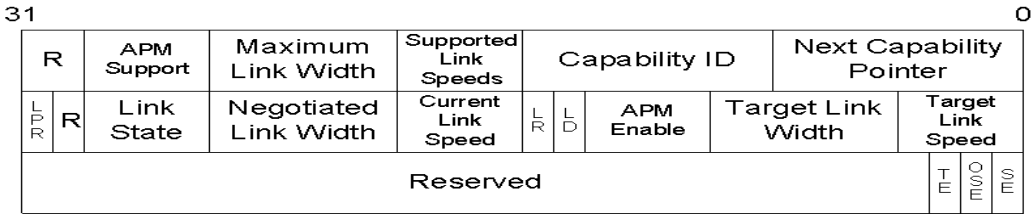


Table 51. Physical Layer Logical Block Configuration Register Descriptions

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	PHY_PORT_CS_0	7:0	Next Capability Pointer This field defines the doubleword index of the next capability register set in the port configuration space. It is set to 00h if the PHY configuration register set is the final register set in the linked list of capability register sets in the port configuration space.	RO	0x3E
0	PHY_PORT_CS_0	15:8	Capability ID This field must contain the value 01h indicating this is the start of the PHY capability register set.	RO	1

Table 51. Physical Layer Logical Block Configuration Register Descriptions (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	PHY_PORT_CS_0	19:16	Supported Link Speeds This field indicates the supported Link speed(s) of the associated Port. Defined encodings are: 1000b 10.0 GT/s Link speed supported 1100b 10.0 GT/s and 20.0 GT/s Link speed supported All other encodings are reserved.	RO	1100b
0	PHY_PORT_CS_0	25:20	Supported Link Width This field indicates the supported Link width (xN – corresponding to N electrical lanes or wavelengths) implemented by the component. Defined encodings are: 000000b x1 000001b x1 000011b x2, x1 000111b x4, x2, x1 001111b x8, x4, x2, x1 011111b x16, x8, x4, x2, x1 111111b x32, x16, x8, x4, x2, x1 All other encodings are reserved.	RO	1
0	PHY_PORT_CS_0	29:26	Automated Management Support Reserved	RO	4'b0001
0	PHY_PORT_CS_0	31:30	Reserved Must be set to 0	RO	0
1	PHY_PORT_CS_1	3:0	Target Link Speed This field specifies the Link speed that the PHY layer must attempt to maintain for the associated Port. Defined encodings are: 1000b 10.0 GT/s 0100b 20.0 GT/s All other encodings are reserved. The default value for this field must be 1000b. If software writes an undefined value to this field the resulting behavior is undefined.	R/W	0100b

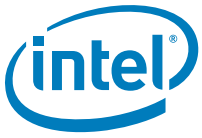


Table 51. Physical Layer Logical Block Configuration Register Descriptions (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
1	PHY_PORT_CS_1	9:4	Target Link Width This field specifies the Link width (xN – corresponding to N electrical lanes or wavelengths) that the PHY layer must attempt to maintain for the associated Port. Defined encodings are: 000001b x1 000010b x2 000100b x4 001000b x8 010000b x16 100000b x32 All other encodings are reserved. The default value for this field is implementation specific. If software writes an undefined value to this field the resulting behavior is undefined.	R/W	1
1	PHY_PORT_CS_1	13:10	Reserved	R/W	0
1	PHY_PORT_CS_1	14	Link Disable This bit disables the Link by directing the LTSSM to the Disabled state when set to 1b. Writes to this bit are immediately reflected in the value read from the bit, regardless of actual Link state. Default value of this bit is 0b.	R/W	0
1	PHY_PORT_CS_1	15	Link Retrain A write of 1b to this bit initiates Link retraining. If the Link is already in training, re-training after completion is permitted but not required. Writing 0b to this bit must have no effect. This bit always returns 0b when read.	R/W SC	0
1	PHY_PORT_CS_1	19:16	Current Link Speed This field indicates the negotiated Link speed of the associated Port. Defined encodings are: 1000b 10.0 GT/s 0100b 20.0 GT/s All other encodings are reserved. This field is undefined if the Link is not up.	RO	0100b
1	PHY_PORT_CS_1	25:20	Negotiated Link Width This field indicates the negotiated Link width (xN – corresponding to N electrical lanes or wavelengths) for the associated port. 000001b x1 000010b x2 000100b x4 001000b x8 010000b x16 100000b x32 All other encodings are reserved. This field is undefined if the Link is not up.	RO	1

Table 51. Physical Layer Logical Block Configuration Register Descriptions (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
1	PHY_PORT_CS_1	29:26	Link State This field indicates the state of the link. Defined encodings are: 0000b: Link Disabled 0001b: Connection detected, Link Training but not up 0010b: CL0 0111b: Cld - Link Down All other encodings are reserved.	RO	0
1	PHY_PORT_CS_1	30	Reserved Must be set to 0	RO	0
1	PHY_PORT_CS_1	31	Link Partner Reset A write of 1b to this bit initiates the transmission of a reset sequence on the link. The reception of the reset sequence at the link partner must result in the link partner being reset to power-on reset state. Reads of this bit return 1b immediately after being written to 1b and continue to do so until the link is up; at all other times reads must return 0b.	R/W SC	0
2	PHY_PORT_CS_2	0	Aligner Lock Error (ALE) This bit when set to 1 indicates that sync bits are lost.	R/Clr	0
2	PHY_PORT_CS_2	1	Order Set Error (OSE) This bit when set to 1 indicates that an unknown OS symbol (bits 1:0 = b10) was received. This bit is cleared on read.	R/Clr	0
2	PHY_PORT_CS_2	2	Timing Error (TE) This bit when set to 1 indicates that: No SLOS2 was received while in LOCK state for 100usec. No TS2 was received (after TS1) for 100usec. This bit is cleared on read.	R/Clr	0
2	PHY_PORT_CS_2	3	Elastic Buffer Error This bit when set to 1 indicates that the elastic buffer reached full state.	R/Clr	0
2	PHY_PORT_CS_2	4	De-skew Buffer Error This bit when set to 1 indicates that the de-skew buffer reached full state.	R/Clr	0
2	PHY_PORT_CS_2	5	RS decoder Error This bit when set to 1 indicates that the RS decoder identified uncorrectable error	R/Clr	0
2	PHY_PORT_CS_2	6	RX aligner timeout This bit when set to 1 indicates that the Rx aligner did not lock on sync bits during 1.5 usec	R/Clr	0
2	PHY_PORT_CS_2	31:7	Reserved Must be set to 0	RO	0

4.3.2.4 Adapter Specific Configuration

Note: The register offset is relative to PORT_ADP_BASE in Table 46.

4.3.2.4.1 PCIe Port

The Adapter capability structure for a PCIe Adapter is shown in Figure 26. The configuration register attributes are defined in Table 52.

Figure 26. PCIe Adapter Capability Structure

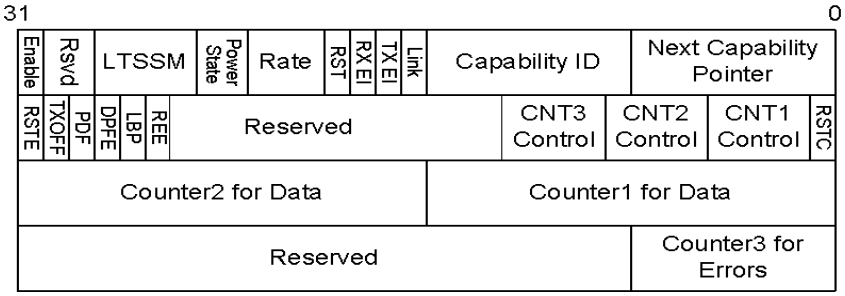


Table 52. PCIe Adapter Configuration Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	ADP_PCIE_CS_0	7:0	Next Capability Pointer This register defines the double word index of the next capability register set in the port configuration space. It is set to 00h if the Adapter capability register set is the final capability set in the linked list of capability register sets in the port configuration space.	RO	0
0	ADP_PCIE_CS_0	15:8	Capability ID This field must contain the value 04h indicating this is the start of the Adapter capability register set.	RO	4
0	ADP_PCIE_CS_0	16	PCIE Link Status PCIE link status of the PCIe core: 0 - Link is down. 1 - Link is up.	RO	0
0	ADP_PCIE_CS_0	17	TX Electrical Idle state 0 - TX is active. 1 - Tx in electrical Idle.	RO	0
0	ADP_PCIE_CS_0	18	RX Electrical Idle state 0 - RX is active. 1 - Rx in Electrical Idle.	RO	0
0	ADP_PCIE_CS_0	19	PCIE Reset state 0 - PCIe domain is active. 1 - PCIE domain in reset.	RO	0
0	ADP_PCIE_CS_0	22:20	PCIE Rate Status PCIE rate status of the core: 1'b0 - Gen1, 1'b1 - Gen2, others – reserved.	RO	0

Table 52. PCIe Adapter Configuration Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	ADP_PCIE_CS_0	24:23	PCIE Power State Status PCIE link power management state status: 2'b00 - P0 (active). 2'b01 - P0s (TX in EI). 2'b10 - P1 (TX/RX in EI). 2'b11 - P2 (TX/RX in EI – lowest power state).	RO	0
0	ADP_PCIE_CS_0	28:25	PCIe LTSSM State 4'h0 – DETECT 4'h1 – POLLING 4'h2 – CONFIG 4'h3 – L0 4'h4 – RECOVERY 4'h5 – DISABLE 4'h6 – LOOPBACK 4'h7 – HOTRESET 4'h8 – L0STX 4'h9 – L0SRX 4'hA – L1 4'hB – L2 4'hC – L0S_TXRX 4'hD – L0S_WAIT_TX_EXIT 4'hE – L0S_WAIT_RX_EXIT	RO	0
0	ADP_PCIE_CS_0	29	Reserved These bits are reserved and must be set to 0.	RO	0
0	ADP_PCIE_CS_0	30	CIO Credit Available	RO	0
0	ADP_PCIE_CS_0	31	Path Enable When set to 1, adapter sends/receives packets. When set to 0, adapter stops sending/receiving packets.	R/W	0
1	ADP_PCIE_CS_1	0	Reset Counters Reset all counters (data counters and error counter).	WO	0
1	ADP_PCIE_CS_1	4:1	Counter1 Control (DFT) Counter 1 Control field (choose which data to count).	R/W	0
1	ADP_PCIE_CS_1	8:5	Counter2 Control (DFT) Counter 2 Control field (choose which data to count).	R/W	0
1	ADP_PCIE_CS_1	11:9	Counter3 Control (DFT) Counter 3 Control field (choose which data to count).	R/W	0
1	ADP_PCIE_CS_1	12	DLLP Plus More Credits Wen set enables to wait more when collecting DLLP and TLP	R/W	0
1	ADP_PCIE_CS_1	14:13	DLLP Plus More Threshold Wen set to wait more when collecting DLLP and TLP	R/W	0
1	ADP_PCIE_CS_1	15	Rx EI Stop Traffic disable	R/W	0

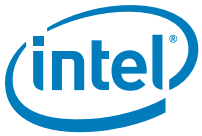


Table 52. PCIe Adapter Configuration Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
1	ADP_PCIE_CS_1	16	Reserved	RO	0
1	ADP_PCIE_CS_1	17	DLLP Plus Enable 1'b0 – No effect (feature disabled) 1'b1 – Enable to collect two packets in one CIO packet.	R/W	0
1	ADP_PCIE_CS_1	18	EIOS EI Assertion Disable 1'b0 – Enable to back pressure PCIE after TxEI Assertion till TxOffline packet is sent to CIO. 1'b1 – No effect (feature disabled)	R/W	0
1	ADP_PCIE_CS_1	19	EIOS EI Assertion Disable 1'b0 – Enable to asser RxEI after receiving EIOS from CIO. 1'b1 – No effect (feature disabled)	R/W	0
1	ADP_PCIE_CS_1	20	TxOffline Stop Read Disable 1'b0 – Enable to back pressure CIO after TxOffline packet to assert RxEI. 1'b1 – No effect (feature disabled)	R/W	0
1	ADP_PCIE_CS_1	21	TS1 to TS2 Transform Disable 1'b0 – Enable to transform TS packets in FIFO to TS2 before L0 state of Tx. 1'b1 – No effect (feature disabled)	R/W	0
1	ADP_PCIE_CS_1	22	TS Fill Disable 1'b0 – Enable to duplicate TS packets without end condition. 1'b1 – No effect (feature disabled)	R/W	0
1	ADP_PCIE_CS_1	23	Logic Idle Add Disable 1'b0 – Enable to add Logic Idle on PIPE Between TS an first non TS packet. 1'b1 – No effect (feature disabled)	R/W	0
1	ADP_PCIE_CS_1	24	Logic Idle Force Disable 1'b0 – Enable to force Logic Idle on PIPE when PCIE Switch goes to L0. 1'b1 – No effect (feature disabled)	R/W	0
1	ADP_PCIE_CS_1	25	Data Path Flush enable 1'b0 – No effect 1'b1 – Enable to perform Ingress Data Path Flush in case of length error.	R/W	0
1	ADP_PCIE_CS_1	26	Reset Endpoint Enable When set enables PCIE Reset to PCIE Endpoint when path is disabled	R/W	1
1	ADP_PCIE_CS_1	27	Lower Back Pressure When set Adapter will assert back-pressure to PCIE IP at lower value	R/W	0
1	ADP_PCIE_CS_1	28	Data Path Flush Enable When set permit to do flush inside PCIE Adapter in case of error	R/W	0

Table 52. PCIe Adapter Configuration Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
1	ADP_PCIE_CS_1	29	Bad PDF Enable When set discard CIO packets with wrong PDF.	R/W	0
1	ADP_PCIE_CS_1	30	TXOff Packet Disable (DFT) When set disable sending TXOffline packets.	R/W	0
1	ADP_PCIE_CS_1	31	PCIe Reset Exit (DFT) When set force the PCIe request signal (from adapter to CAR) to stay high.	R/W	0
2	ADP_PCIE_CS_2	15:0	Counter1 for Data (DFT) Counter for Data (all types of data on Tx/Rx).	RO	NA
2	ADP_PCIE_CS_2	31:16	Counter2 for Data (DFT) Counter for Data (all types of data on Tx/Rx).	RO	NA
3	ADP_PCIE_CS_3	7:0	Counter3 for Errors (DFT) Counter for Rx Errors (all types of errors on Rx).	RO	NA
3	ADP_PCIE_CS_3	8	LTSSM was in Detect status	R/W S	0
3	ADP_PCIE_CS_3	9	LTSSM was in Configuration status	R/W S	0
3	ADP_PCIE_CS_3	10	LTSSM was in Recovery status	R/W S	0
3	ADP_PCIE_CS_3	11	LTSSM was in L2 status	R/W S	0
3	ADP_PCIE_CS_3	15:12	Reserved	R/W	0
3	ADP_PCIE_CS_3	16	COM after end fix dis	R/W	0
3	ADP_PCIE_CS_3	17	RX EI logic idle disable	R/W	0
3	ADP_PCIE_CS_3	18	FIFO Flush in L2 enable	R/W	0
3	ADP_PCIE_CS_3	19	FIFO Flush in L1 enable	R/W	0
3	ADP_PCIE_CS_3	20	TX FIFO delay fix disable	R/W	0
3	ADP_PCIE_CS_3	21	TS duplicate fix disable	R/W	0
3	ADP_PCIE_CS_3	22	Skip insert fix disable	R/W	0
3	ADP_PCIE_CS_3	23	Logic Idle gap fix disable	R/W	0
3	ADP_PCIE_CS_3	24	Reset TxOff counter fix disable	R/W	0
3	ADP_PCIE_CS_3	25	No Rx EI in Polling enable	R/W	0
3	ADP_PCIE_CS_3	26	LTSSM sync fix disable	R/W	0
3	ADP_PCIE_CS_3	27	Higher Back Pressure release	R/W	0
3	ADP_PCIE_CS_3	28	TXOff send fix disable	R/W	0
3	ADP_PCIE_CS_3	29	Rx Valid from Rx EI fix disable	R/W	0
3	ADP_PCIE_CS_3	30	CIO TL Sync Mode enable	R/W	0
3	ADP_PCIE_CS_3	31	PCIE Adapter Wake, Option to cause wake	R/W	0
4	ADP_PCIE_CS_4	29:0	DFT RO Register	RO	0
4	ADP_PCIE_CS_4	31:30	DFT RO Register Control	R/W	0
5	ADP_PCIE_CS_5	0	CIO Back Pressure till Packet Start fix disable	R/W	0
5	ADP_PCIE_CS_5	1	PCIE to CIO TLP/DLLP Back to Back Fix disable	R/W	0
5	ADP_PCIE_CS_5	3:2	CIO to PCIE Aligner Num Select Values 1,2,3 enable to use part of the Aligner	R/W	0
5	ADP_PCIE_CS_5	4	Higher StopTX Threshold When set enables higher back pressure threshold on PIPE	R/W	0
5	ADP_PCIE_CS_5	5	CIO to PCIE Delay Skip insert enable	R/W	0
5	ADP_PCIE_CS_5	31:0	Reserved	R/W	0

4.3.2.4.2 Display Port (DP) IN

The Adapter capability structure for a DisplayPort IN Adapter is shown in Figure 27. The configuration register attributes are defined in Table 53.

Figure 27. DisplayPort IN Adapter Capability Structure

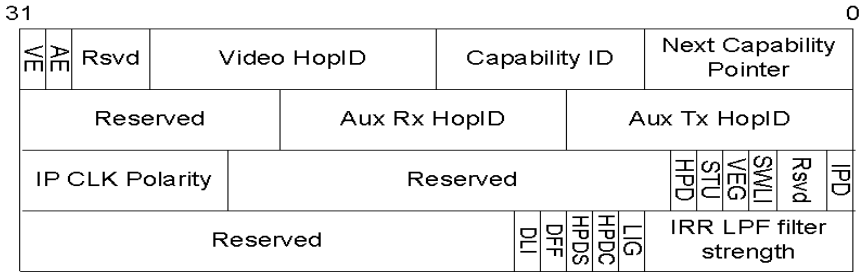


Table 53. DisplayPort Adapter IN Configuration Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	ADP_DP_CS_0	7:0	Next Capability Pointer This register defines the doubleword index of the next capability register set in the port configuration space. It is set to 00h if the Adapter capability register set is the last capability set in the linked list of capability register sets in the port configuration space.	RO	(VSEC)
0	ADP_DP_CS_0	15:8	Capability ID This field must contain the value 04h indicating this is the start of the Adapter capability register set.	RO	4
0	ADP_DP_CS_0	26:16	Video HopID This field specifies the HopID for the path used to transmit Main Link video data.	R/W	0
0	ADP_DP_CS_0	29:27	Reserved These bits are reserved and must be set to 0.	RO	0
0	ADP_DP_CS_0	30	AE – AUX Enable When set to 1, adapter sends/ receives packets on the AUX Rx and AUX Tx HopIDs. When set to 0 no packets are sent/received.	R/W	0
0	ADP_DP_CS_0	31	VE – Video Enable When set to 1, adapter sends packets on the Video HopID. When set to 0, no packets are received.	R/W	0
1	ADP_DP_CS_1	10:0	AUX Tx HopID This field specifies the HopID for the path used to transmit AUX and HPD packets.	R/W	0

Table 53. DisplayPort Adapter IN Configuration Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
1	ADP_DP_CS_1	21:11	AUX Rx HopID This field specifies the HopID for the path used to receive AUX and HPD packets.	R/W	0
1	ADP_DP_CS_1	31:22	Reserved These bits are reserved and must be set to 0.	RO	0
2	ADP_DP_CS_2	0	IP Debug (IPD) This bit enables to connect the DP_IN_IP directly to DP_OUT_IP and vice-versa for debug purpose.	R/W	0
2	ADP_DP_CS_2	2:1	Reserved These bits are reserved and must be set to 0.	RO	0
2	ADP_DP_CS_2	3	SW Link Init to IP (SWLI) When set, a link_init will be sent to the IP. This bit is ORed with all others link_init conditions.	R/W	0
2	ADP_DP_CS_2	4	Video Enable Gating DP IN TMU (VEG) The TMU in the DP IN is gating with video enable (when the bit=1) or by first packet from IP when video is enabled (when the bit=0).	R/W	0
2	ADP_DP_CS_2	5	Single TU Mode (STU) When this bit is set each video TU will be sent in a separate CIO packet.	R/W	0
2	ADP_DP_CS_2	6	HPD status This bit represents the HPD line status.	RO	0
2	ADP_DP_CS_2	31:7	Reserved	R/W	0
3	ADP_DP_CS_3	7:0	IIR LPF filter strength The value of this field sets the strength of IIR LPF filter in DP_IN clock restoration mechanism. The IIR filter's formula: Y = (1-1/A)*Y + X/A. If this parameter is P, then A = 2^P.	R/W	5
3	ADP_DP_CS_3	8	Link Init Gating (LIG) 0 – Link init is enabled. 1 – Link init is disabled.	R/W	0
3	ADP_DP_CS_3	9	HPD Output Clear (HPDC) Write 1 causes a single event of HPD output clear (drive 0) Stays 1 until cleared by writing 0.	R/W	0

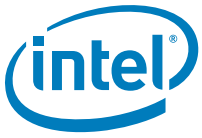


Table 53. DisplayPort Adapter IN Configuration Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
3	ADP_DP_CS_3	10	HPD Output Set (HPDS) Write 1 causes a single event of HPD output set (drive 1) Stays 1 until cleared by writing 0.	R/W	0
3	ADP_DP_CS_3	11	Disable Fifo full protection fix (DFF) When set to 1 will disable the DP IN Fifo full fix.	R/W	0
3	ADP_DP_CS_3	12	Disable Link Init on Fifo full (DLI) When set to 1 will gate link init to be asserted upon Fifo full event in DP IN.	R/W	0
3	ADP_DP_CS_3	31:13	Reserved	RO	0
4	DP_LOCAL_CAP	3:0	Local DP Capability ID: 0: Legacy DP 1,2: DP1.2	RO (loaded from eeprom/flash)	2
4	DP_LOCAL_CAP	7:4	Local Maximal DPCD Rev: 0: DP1.1a 1: DP1.2	RO (loaded from eeprom/flash)	1
4	DP_LOCAL_CAP	11:8	Local Maximal Link Rate: 0: 1.62GHz 1: 2.7GHz 2: 5.4GHz	RO (loaded from eeprom/flash)	2
4	DP_LOCAL_CAP	14:12	Local Maximal Lane Count: 0: 1 lane 1: 2 lanes 2: 4 lanes	RO (loaded from eeprom/flash)	2
4	DP_LOCAL_CAP	15	Local MST Capability 0: Not supported 1: supported	RO (loaded from eeprom/flash)	1
4	DP_LOCAL_CAP	21:16	Reserved	RO	0
4	DP_LOCAL_CAP	22	Local TPS3 supported	RO (loaded from eeprom/flash)	1
4	DP_LOCAL_CAP	23	Local Enhanced framing supported	RO (loaded from eeprom/flash)	1
4	DP_LOCAL_CAP	31:24	Reserved	RO	0
5	DP_REMOTE_CAP	3:0	Remote DP Capability ID: 0: Legacy DP 1,2: DP1.2	R/W	0
5	DP_REMOTE_CAP	7:4	Remote Maximal DPCD Rev: 0: DP1.1a 1: DP1.2	R/W	0
5	DP_REMOTE_CAP	11:8	Remote Maximal Link Rate: 0: 1.62GHz 1: 2.7GHz 2: 5.4GHz	R/W	0
5	DP_REMOTE_CAP	14:12	Remote Maximal Lane Count: 0: 1 lane 1: 2 lanes 2: 4 lanes	R/W	0

Table 53. DisplayPort Adapter IN Configuration Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
5	DP_REMOTE_CAP	15	Remote MST Capability 0: Not supported 1: supported	R/W	0
5	DP_REMOTE_CAP	21:16	Reserved	R/W	0
5	DP_REMOTE_CAP	22	Remote TPS3 supported	R/W	0
5	DP_REMOTE_CAP	23	Remote Enhanced framing supported	R/W	0
5	DP_REMOTE_CAP	31:24	Reserved	R/W	0
6	DP_STATUS	2:0	Lane Count: 0: 1 lane 1: 2 lanes 4: 4 lanes	RO (according to the established link)	0
6	DP_STATUS	7:3	Reserved	RO	0
6	DP_STATUS	9:8	Link Rate: 0: 1.62GHz 1: 2.7GHz 2: 5.4GHz	RO (according to the established link)	0
6	DP_STATUS	16:10	Reserved	RO	0
6	DP_STATUS	31:17	Reserved	R/W	0

4.3.2.4.3 Display Port (DP) OUT

The Adapter capability structure for a DisplayPort OUT Adapter is shown in Figure 28. The configuration register attributes are defined in Table 54.

Figure 28. DisplayPort OUT Adapter Capability Structure

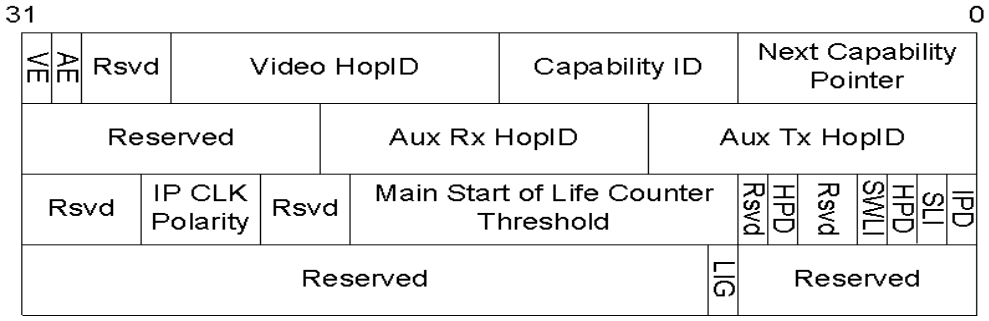


Table 54. DisplayPort OUT Adapter Configuration Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	ADP_DP_CS_0	7:0	Next Capability Pointer This register defines the doubleword index of the next capability register set in the port configuration space. It is set to 00h if the Adapter capability register set is the last capability set in the linked list of capability register sets in the port configuration space.	RO	(VSEC)

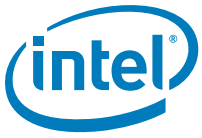


Table 54. DisplayPort OUT Adapter Configuration Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	ADP_DP_CS_0	15:8	Capability ID This field must contain the value 04h indicating this is the start of the Adapter capability register set.	RO	4
0	ADP_DP_CS_0	26:16	Video HopID This field specifies the HopID for path used to transmit Main Link video data.	R/W	0
0	ADP_DP_CS_0	29:27	Reserved These bits are reserved and must be set to 0.	RO	0
0	ADP_DP_CS_0	30	AE – AUX Enable When set to 1, adapter sends/ receives packets on the AUX Rx and AUX Tx HopIDs. When set to 0 no packets are sent/received.	R/W	0
0	ADP_DP_CS_0	31	VE – Video Enable When set to 1, adapter sends packets on the Video HopID. When set to 0, no packets are sent.	R/W	0
1	ADP_DP_CS_1	10:0	AUX Tx HopID This field specifies the HopID for the path used to transmit AUX and HPD packets.	R/W	0
1	ADP_DP_CS_1	21:11	AUX Rx HopID This field specifies the HopID for path used to receive AUX and HPD packets.	R/W	0
1	ADP_DP_CS_1	31:22	Reserved These bits are reserved and must be set to 0.	RO	0
2	ADP_DP_CS_2	0	Reserved These bits are reserved and must be set to 0.	R/W	0
2	ADP_DP_CS_2	1	Reset link on ECC error When set to 1 enables link reset in case of ECC error in memory buffer. When set to 0 will mask ECC errors.	R/W	0
2	ADP_DP_CS_2	2	Disable periodic HDP When set to 1, will disable periodic HDP to DP_IN	R/W	0
2	ADP_DP_CS_2	3	SW Link Init to IP (SWLI) When set, a link_init will be sent to the IP. This bit is ORed with all other link_init conditions.	R/W	0
2	ADP_DP_CS_2	6:4	Reserved These bits are reserved and must be set to 0.	RO	0
2	ADP_DP_CS_2	7	Fast periodic HPD When set to 1: instead of 1Sec - send HPD every 100uSec	RO	0

Table 54. DisplayPort OUT Adapter Configuration Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
2	ADP_DP_CS_2	20:8	Start of Main Threshold Wait number of cycles after receiving first main packet until the main FIFO is being used.	R/W	4095
2	ADP_DP_CS_2	31:21	Reserved These bits are reserved and must be set to 0.	RO	0
3	ADP_DP_CS_3	7:0	IIR LPF filter strength The value of this field sets the strength of IIR LPF filter in DP_IN clock restoration mechanism. The IIR filter's formula: Y = (1-1/A)*Y + X/A. If this parameter is P, then A = 2^P.	R/W	0
3	ADP_DP_CS_3	8	Link Init Gating (LIG) 0 – Link init is enabled. 1 – Link init is disabled.	R/W	0
3	ADP_DP_CS_3	31:9	Reserved These bits are reserved and must be set to 0.	RO	0
4	DP_LOCAL_CAP	3:0	Local DP Capability ID: 0: Legacy DP 1,2: DP1.2	RO (loaded from eeprom/ flash)	2
4	DP_LOCAL_CAP	7:4	Local Maximal DPCD Rev: 0: DP1.1a 1: DP1.2	RO (loaded from eeprom/ flash)	1
4	DP_LOCAL_CAP	11:8	Local Maximal Link Rate: 0: 1.62GHz 1: 2.7GHz 2: 5.4GHz	RO (loaded from eeprom/ flash + updated by Monitor capabilities)	2
4	DP_LOCAL_CAP	14:12	Local Maximal Lane Count: 0: 1 lane 1: 2 lanes 2: 4 lanes	RO (loaded from eeprom/ flash + updated by Monitor capabilities)	2
4	DP_LOCAL_CAP	15	Local MST Capability 0: Not supported 1: supported	RO (loaded from eeprom/ flash)	1
4	DP_LOCAL_CAP	21:16	Reserved	RO	0
4	DP_LOCAL_CAP	22	Local TPS3 supported	RO (loaded from eeprom/ flash + updated by Monitor capabilities)	1
4	DP_LOCAL_CAP	23	Local Enhanced framing supported	RO (loaded from eeprom/ flash + updated by Monitor capabilities)	1
4	DP_LOCAL_CAP	31:24	Reserved	RO	0
5	DP_REMOTE_CAP	3:0	Remote DP Capability ID: 0: Legacy DP 1,2: DP1.2	R/W	0

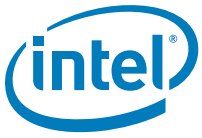


Table 54. DisplayPort OUT Adapter Configuration Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
5	DP_REMOTE_CAP	7:4	Remote Maximal DPCD Rev: 0: DP1.1a 1: DP1.2	R/W	0
5	DP_REMOTE_CAP	11:8	Remote Maximal Link Rate: 0: 1.62GHz 1: 2.7GHz 2: 5.4GHz	R/W	0
5	DP_REMOTE_CAP	14:12	Remote Maximal Lane Count: 0: 1 lane 1: 2 lanes 2: 4 lanes	R/W	0
5	DP_REMOTE_CAP	15	Remote MST Capability 0: Not supported 1: supported	R/W	0
5	DP_REMOTE_CAP	21:16	Reserved	R/W	0
5	DP_REMOTE_CAP	22	Remote TPS3 supported	R/W	0
5	DP_REMOTE_CAP	23	Remote Enhanced framing supported	R/W	0
5	DP_REMOTE_CAP	31:24	Reserved	R/W	0
6	DP_STATUS	2:0	Lane Count: 0: 1 lane 1: 2 lanes 4: 4 lanes	RO (according to the established link)	0
6	DP_STATUS	7:3	Reserved	RO	0
6	DP_STATUS	9:8	Link Rate: 0: 1.62GHz 1: 2.7GHz 2: 5.4GHz	RO (according to the established link)	0
6	DP_STATUS	16:10	Reserved	RO	0
6	DP_STATUS	31:24	Reserved	R/W	0

4.3.2.5 Vendor Specific Configuration

The Vendor-Specific capability structure is an optional capability that is permitted to be implemented by any CIO Switch. This allows the CIO Switch vendors to use the device configuration space to expose vendor-specific registers. Multiple Vendor-Specific capability structures are permitted to exist in the port configuration space. Vendor-Specific capability registers have the same format as the registers described in Table 55.

Note: The register offset is relative to PORT_VSEC_BASE in Table 46.

4.3.2.5.1 Display Port (DP)

The attributes of the DP vendor-specific capability registers are described in Table 55. Those registers related to the 8051.

Having more physical DP ports than DP adapters (because of the SRC ports for re-driver mode), each DP_IN adapter has two Vendor Specific Configuration Spaces assigned to its PortID - VSEC with VSEC_ID=1 contains the registers of redriver SRC DP port, while VSEC with VSEC_ID=0 contains the register of SNK DP port, e.g. VSEC registers of SRC_PA and SNK0 can be accessed through DP_IN PortID of the first DP_IN adapter (while SNK0 VSEC is pointed by Next Capability Pointer of SRC_PA VSEC).

Table 55. DP Vendor Specific Configuration Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	VSEC_DP_CS_0	7:0	Next Capability Pointer This field defines the doubleword index of the next capability register set in the device configuration space. It is set to 00h if the Vendor-Specific capability register set is the final register set in the linked list of capability register sets in the device configuration space.	RO	0 – in case of SNK 0x8F – in case of SRC
0	VSEC_DP_CS_0	15:8	Capability ID This field must contain the value 05h indicating this is the start of Vendor-Specific capability register set.	RO	5
0	VSEC_DP_CS_0	23:16	VSEC ID This field is a vendor-defined ID number that indicates the nature and format of the VSEC structure.	RO	0 – in case of SNK 1 – in case of SRC
0	VSEC_DP_CS_0	31:24	VSEC Length This field indicates the number of double words in the entire VSEC structure including the header and the Vendor-Specific registers.	RO	0x3D
1	IP_CMD	0	IP Valid Command for the IP interface is valid. Self cleared after 8 cycles of 25MHz clock.	R/W	0
1	IP_CMD	1	IP Write1/Read0 Command for the IP interface is Write or Read: WR = 1, RD = 0.	R/W	0
1	IP_CMD	31:2	Reserved These bits are reserved and must be set to 0.	RO	0
2	IP_ADDR	15:0	IP Address Address to be written in the IP (dp_8051 or Host).	WO	0
2	IP_ADDR	31:16	Reserved These bits are reserved and must be set to 0.	RO	0
3	IP_WDATA	31:0	IP Write Data Data to be written to the IP (dp_8051 or Host).	WO	0
4	IP_RDATA	31:0	IP Read Data Data to be read from IP (dp_8051 or Host).	RO	0
The following registers exist only in the first DP VSEC (i.e. the one of the SRC).					
48	VSEC_DP_CS_48	0	Reserved. Writing to this bit will override the EE value.	R/W	0 loaded from FLASH (see FLASH map, byte 0x4A)

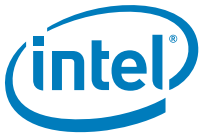


Table 55. DP Vendor Specific Configuration Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
48	VSEC_DP_CS_48	1	DP Capability Loaded from EE (2 separate bits for dp_in and dp_out). Indicates whether DP is supported.	RO	1 loaded from FLASH (see FLASH map, byte 0x4A)
48	VSEC_DP_CS_48	2	Reserved Loaded from EE (2 separate bits for dp_in and dp_out).	RO	1 loaded from FLASH (see FLASH map, byte 0x4A – Section 3.2)
48	VSEC_DP_CS_48	3	DP IN – DP AUX_N Status DP OUT – DP HPD Status	RO	0
48	VSEC_DP_CS_48	4	DP IN – Reserved DP OUT – whenever set, the adapter will not stop reading from its TL, otherwise it might be stopped due to FIFO overflow.	RO R/W	0
48	VSEC_DP_CS_48	31:5	Reserved	RO	0
49	VSEC_DP_CS_49	3:0	DP Sample Time Indicates the time between signal's samples in DP debouncing filter (in ms). A value of 0, disable the filter.	R/W	1
49	VSEC_DP_CS_49	11:4	DP Number of Samples Number of samples in the DP debouncing filter.	R/W	100
49	VSEC_DP_CS_49	15:12	Reserved	RO	0
49	VSEC_DP_CS_49	19:16	Reserved	R/W	1
49	VSEC_DP_CS_49	27:20	Reserved	R/W	100
49	VSEC_DP_CS_49	31:28	Reserved	RO	0
50	VSEC_DP_CS_50	4:0	Reserved	R/W	0
50	VSEC_DP_CS_50	15:5	Reserved	RO	0
50	VSEC_DP_CS_50	23	DP In – GPU present DP Out - Reserved	R/W	0
50	VSEC_DP_CS_50	22:16	DP In – SSC PPM (in resolution of 50 PPM units) DP Out - Reserved	R/W	0
50	VSEC_DP_CS_50	31:24	Reserved	RO	0

4.3.2.5.2 CIO Port

The CIO port vendor-specific capability registers are for internal use only.

The attributes of the CIO port vendor-specific capability registers are described in Table 56.

Table 56. CIO port Vendor Specific Configuration Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	VSEC_CIO_CS_0	7:0	Next Capability Pointer This field defines the doubleword index of the next capability register set in the device configuration space. It is set to 00h if the Vendor-Specific capability register set is the final register set in the linked list of capability register sets in the device configuration space.	RO	0
0	VSEC_CIO_CS_0	15:8	Capability ID This field must contain the value 05h indicating this is the start of the Vendor-Specific capability register set.	RO	5
0	VSEC_CIO_CS_0	23:16	VSEC ID This field is a vendor-defined ID number that indicates the nature and format of the VSEC structure.	RO	
0	VSEC_CIO_CS_0	31:24	VSEC Length This field indicates the number of double words in the entire VSEC structure including the header and the Vendor-Specific registers.	RO	13
1	VSEC_CIO_CS_1	0	Snooper FIFO When 1 – will ensure FIFO behavior when snoop mode – all hopids are merged into one (constant) hopid so there aren't separate queues for each hopid, but one big FIFO for every packet received. When 0 – on snoop mode every hopid will have its own queue. When not in snoop mode – the bit is ignored. Relevant only for CIO adapter.	R/W	0
1	VSEC_CIO_CS_1	1	Reset SLOS Counter On Unplug CB Setting this bit to 1 will cause not to reset the slos counter on unplug event.	R/W	0
1	VSEC_CIO_CS_1	2	Reserved	R/W	0
1	VSEC_CIO_CS_1	3	TS OS Counter CB Setting this bit to 1 will cause not to count few TS before looking the TS attributes.	R/W	0
1	VSEC_CIO_CS_1	4	Retrain On Unknown OS CB Setting this bit to 1 will cause not to retrain when a 15 consecutive unknown OS.	R/W	0
1	VSEC_CIO_CS_1	5	Backpressure upon single retrain CB Setting this bit to 1 will cause not to apply backpressure when retraining in single mode.	R/W	0
1	VSEC_CIO_CS_1	6	Reserved	R/W	0

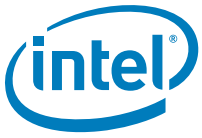


Table 56. CIO port Vendor Specific Configuration Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
1	VSEC_CIO_CS_1	7	Advance Lfsr On Non SCR CB Setting this bit to 1 will cause to advance the scrambler when an OS[9:0] != ~`SCR (fix that was reverted).	R/W	0
1	VSEC_CIO_CS_1	8	Single mode retrain CB This bit has different functionality depending on the lane index. For lane 0 Setting this bit to 1 will prevent dual lane manager fsm to wait for tx buffer to become empty before applying retrain. For lane 1 Setting this bit to 1 will prevent a fix that getting SLOS will cause apply retrain from lcok	R/W	0
1	VSEC_CIO_CS_1	9	Link partner dual able CB Setting this bit to 1 will prevent a fix that report on RX TS dual able only if has been received 3 consecutive times.	R/W	0
1	VSEC_CIO_CS_1	10	Reset elastic buffer max used space Debug only.	R/W	0
1	VSEC_CIO_CS_1	11	Stuck TS1 CB Setting this bit to 1 will prevent a fix that stay in TS1 until rx buffer is empty.	R/W	0
1	VSEC_CIO_CS_1	12	Soft back pressure Setting this bit to 1 will assert manually the back pressure to cio switch	R/W	0
1	VSEC_CIO_CS_1	13	Block link manager backpressure Setting this bit to 1 will block back pressure from TL to cio switch.	R/W	0
1	VSEC_CIO_CS_1	14	TL_tx_st_frd Setting this bit to 1 will cause TL tx fifo to act in store and forward mode	R/W	0
1	VSEC_CIO_CS_1	15	Dis_rs_err_retrain Setting this bit to 1 will prevent RS error cause retrain from lock.	R/W	0
1	VSEC_CIO_CS_1	16	Flip_bit_order Setting this bit to 0 will flip bit order within each byte in both rx and tx 64/128 symbol. Sync bits are not affected by this bit	R/W	1
1	VSEC_CIO_CS_1	17	Sample_hs_cb Setting this bit to 1 will change the sampling order of rx data_h/l from cio ana.	R/W	0
1	VSEC_CIO_CS_1	18	Dis_skip Setting this bit to 1 will disable sending skip OS. can be used in AR to AR connection.	R/W	0
1	VSEC_CIO_CS_1	24:19	Reserved	R/W	0
1	VSEC_CIO_CS_1	29:25	SKIP OS Ratio Skip symbol ratio will be (SKIP_OS_Ratio+1)*64. Default gives skip every 1600 symbols.	R/W	24

Table 56. CIO port Vendor Specific Configuration Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
1	VSEC_CIO_CS_1	30	Soft reset tx path Setting this bit to 1 will reset the tx path for 1 cycle.	R/WClr	0
1	VSEC_CIO_CS_1	31	Target retrain from lock Setting this bit to 1 will cause retrain from lock	R/WClr	0
2	VSEC_CIO_CS_2	11:0	Flow Control Timer Limit TL flow control periodic timer event in us. Allow changing the periodic credit grant period in the TL.	R/W	100
2	VSEC_CIO_CS_2	31:12	Reserved	RO	0
3	VSEC_CIO_CS_3	31:0	HEC Single Errors Counter Number of single hec errors detected. Clear by write.	W/Clr	0
4	VSEC_CIO_CS_4	31:0	Link_Down_Counter Number of link down events. Clear by write.	W/Clr	0
5	VSEC_CIO_CS_5	31:0	Unplug_Event_Counter Number of unplug events. Clear by write.	W/Clr	0
6	VSEC_CIO_CS_6	3:0	Deskew_debug Count cycles between this lane get deskew OS and both lanes has got the deskew OS.	R/W	0
6	VSEC_CIO_CS_6	31:4	Reserved	RO	0
7	VSEC_CIO_CS_7	31:0	Probing Register Probe internal signals.	RO	N/A
8	VSEC_CIO_CS_8	1:0	debug_spare ctrl Select the source of RS frame spare bit. To be used for debug.	R/W	0
8	VSEC_CIO_CS_8	31:2	Reserved	R/W	0
9	VSEC_CIO_CS_9	7:0	RS_err_mask_inject_0 Carry the byte mask for 1st RS error injection. Debug only.	R/W	0
9	VSEC_CIO_CS_9	15:8	RS_err_mask_inject_1 Carry the byte mask for 2nd RS error injection. Debug only.	R/W	0
9	VSEC_CIO_CS_9	23:16	RS_err_mask_inject_2 Carry the byte mask for 3rd RS error injection. Debug only.	R/W	0
9	VSEC_CIO_CS_9	31:24	RS_err_mask_inject_3 Carry the byte mask for 4th RS error injection. Debug only.	R/W	0
10	VSEC_CIO_CS_10	7:0	RS_err index_injection_0 Carry the byte index for 1st RS error injection mechanism.	R/W	0
10	VSEC_CIO_CS_10	15:8	RS_err index_injection_1 Carry the byte index for 2nd RS error injection mechanism.	R/W	0

Table 56. CIO port Vendor Specific Configuration Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
10	VSEC_CIO_CS_10	23:16	RS_err index_injection_2 Carry the byte index for 3rd RS error injection mechanism.	R/W	0
10	VSEC_CIO_CS_10	31:24	RS_err index_injection_3 Carry the byte index for 4th RS error injection mechanism.	R/W	0
11	VSEC_CIO_CS_11	3:0	En_RS_err_injection Setting each bit to 1 will activate 1st-4th RS error injection mechanisms respectively.	R/W	0
11	VSEC_CIO_CS_11	7:4	Inc_RS_err_injection_index 0 Setting these bits to 1 will cause 1st -4th RS error injection mechanism (respectively) to	R/W	0
11	VSEC_CIO_CS_11	23:8	RS_err_injection_frames Carry the amount of RS frames to be injected with RS errors, by all RS error injection	R/W	0
11	VSEC_CIO_CS_11	31:24	Reserved	R/W	0
12	VSEC_CIO_CS_12	15:0	RS uncorrectable errors counter. Carry the amount of uncorrectable RS error detected by RS decoder.	RW/Clr	0
12	VSEC_CIO_CS_12	31:16	RS correctable errors counter. Carry the amount of correctable RS error detected by RS decoder.	RW/Clr	0
13	VSEC_CIO_CS_13	7:0	Soft_HEC_error Carry the down counter amount of hec err dummy indication that will be driven after each	RW	0

4.3.2.5.3 DMA Configuration Based Mailbox Specific Registers

The attributes of the DMA Configuration Based Mailbox vendor-specific capability registers are described in Table 57.

Table 57. Flash Controller Vendor Specific Configuration Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	VSEC_1_DMA_MAILBOX	7:0	Next Capability Pointer This field defines the doubleword index of the next capability register set in the device configuration space. It is set to 00h if the Vendor-Specific capability register set is the final register set in the linked list of capability register sets in the device configuration space.	RO	0x52
0	VSEC_1_DMA_MAILBOX	15:8	Capability ID This field must contain the value 05h indicating this is the start of the Vendor-Specific capability register set.	RO	5

Table 57. Flash Controller Vendor Specific Configuration Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	VSEC_1_DMA_MAILBOX	23:16	VSEC ID This field is a vendor-defined ID number that indicates the nature and format of the VSEC structure.	RO	0x01
0	VSEC_1_DMA_MAILBOX	31:24	VSEC Length This field indicates the number of double words in the entire VSEC structure including the header and the Vendor-Specific registers.	RO	0x13
1	MAIL_DATA_0	31:0	Mail Data 0	RW	0
2	MAIL_DATA_1	31:0	Mail Data 1	RW	0
3	MAIL_DATA_2	31:0	Mail Data 2	RW	0
4	MAIL_DATA_3	31:0	Mail Data 3	RW	0
5	MAIL_DATA_4	31:0	Mail Data 4	RW	0
6	MAIL_DATA_5	31:0	Mail Data 5	RW	0
7	MAIL_DATA_6	31:0	Mail Data 6	RW	0
8	MAIL_DATA_7	31:0	Mail Data 7	RW	0
9	MAIL_DATA_8	31:0	Mail Data 8	RW	0
10	MAIL_DATA_9	31:0	Mail Data 9	RW	0
11	MAIL_DATA_10	31:0	Mail Data 10	RW	0
12	MAIL_DATA_11	31:0	Mail Data 11	RW	0
13	MAIL_DATA_12	31:0	Mail Data 12	RW	0
14	MAIL_DATA_13	31:0	Mail Data 13	RW	0
15	MAIL_DATA_14	31:0	Mail Data 14	RW	0
16	MAIL_DATA_15	31:0	Mail Data 15	RW	0
17	MAIL_IN	31:0	Mail In Writing to this register from any master *except* ARC will generate an interrupt to ARC.	RW	0
18	MAIL_OUT	31:0	Mail Out	RW	0

MAIL_IN Command structures

See Table 58 for Non Active Flash Region Write MAIL_IN outline.

Table 58. Non Active Flash Region Write

Name	Bits	Value	Remarks
Operation Request	0	1b	SW sets this bit to indicate a new operation is requested FW clears the bit when it completes the operation
CSS Header	1	0b	Indicates CSS header write, total of 2 writes initiated by SW by order
Flash Address	23:2	Variable	Flash DW starting address to be written relative to the starting point of the non active region

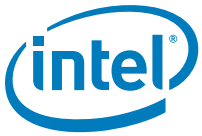


Table 58. Non Active Flash Region Write (Continued)

Name	Bits	Value	Remarks
High DW	27:24	Variable	Number of DW to be written to flash, this value indicated the last MAIL_DATA DW register that should be written to Flash as a result of this command
Command	31:28	0x0	Non Active Flash Region Write

Note: This command doesn't support random write access to the Flash.

See Table 59 for Flash Update Authenticate MAIL_IN outline.

Table 59. Flash Update Authenticate

Name	Bits	Value	Remarks
Operation Request	0	1b	SW sets this bit to indicate a new operation is requested FW clears the bit when it completed the operation
Reserved	27:1	0b	Reserved
Command	31:28	0x1	Flash Update Authenticate

See Table 60 for Active Flash Region Read MAIL_IN outline.

Table 60. Active Flash Region Read

Name	Bits	Value	Remarks
Operation Request	0	1b	SW sets this bit to indicate a new operation is requested FW clears the bit when it completed the operation
Reserved	1	0b	Reserved
Flash Address	2	Variable	Flash DW starting address to read
DW Count	27:24	Variable	Number of DW to read, read data is stored in MAIL_DATA Value of 0x0 indicates 16 DW read
Command	31:28	0x2	Active Flash Region Read

See Table 61 for Power cycle request MAIL_IN outline.

Table 61. Power cycle request

Name	Bits	Value	Remarks
Operation Request	0	1b	SW sets this bit to indicate a new operation is requested FW clears the bit as an indication it is going to start the power cycle
Reserved	27:1	0b	Reserved
Command	31:28	0x4	Power cycle request

MAIL_OUT Command structures

See Table 62 for Status Response MAIL_OUT outline.

Table 62. Status Response

Name	Bits	Value	Remarks
Status	3:0	Variable	Staus: 0x0 Command completed (success) 0x1 Error (authentication failed) 0x2 Error (Access to restricted area) 0x3 Error (other/general) 0x4 Authentication in progress 0x5-0xF Reserved
Status for command	7:4	Variable	Status relevant for command: 0x0 Non Active Flash Region Write 0x1 Flash Update Authenticate 0x2 Active Flash Region Read Reserved 0x4 Power cycle request 0x5-0xE Reserved 0xF Unkown command
Reserved	28:8	0x00	Reserved
Status response	29	1b	Status Response indication FW sets this bit to indicate a new status response SW clears the bit after it reads the response value
Notification indication	30	0b	Notification Indication FW sets to 1 to indicate new notification SW clears after read (FW can push subsequent notification without outstanding notification read conformation)
Operation Request	31	0b	Operation Request FW sets this bit to indicate a new operation is requested SW clears the bit when it completes the operation (FW will not push subsequent request if operation in progress)

4.3.3 Path Configuration Space

Figure 29 shows the path configuration space registers that must be implemented by every CIO Switch. Each path has a set of configuration registers that are described in Table 63. The path configuration registers are indexed based on the HopID contained in the packet header when a packet is received at the ingress side of the port.

Note: Path Config registers for Port#0 (Control Port) initialized by HW defaults and should not be configured by SW.

Figure 29. Path Configuration Space

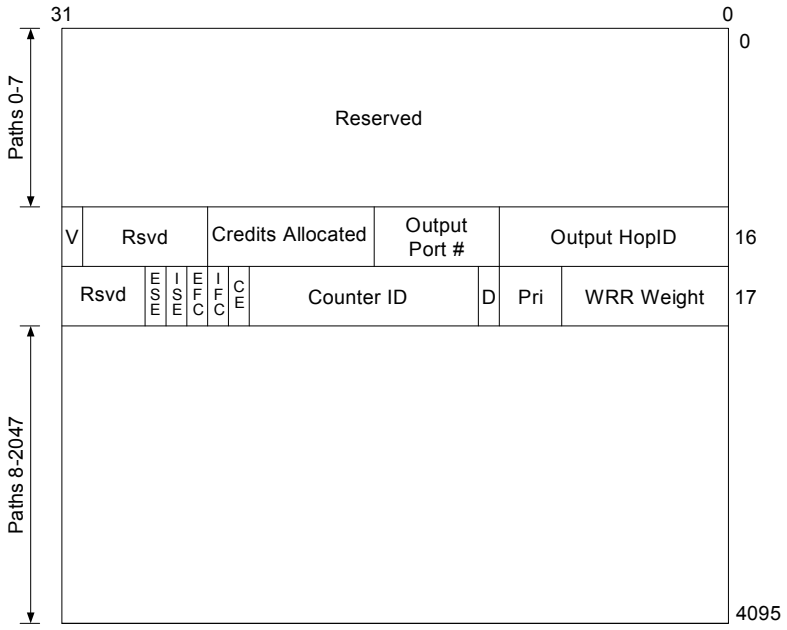


Table 63. Path Configuration Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	PATH_CS_0	10:0	Output HopID This field specifies the output HopID for the path.	R/W	Path 0 – Input port # Else - 0
0	PATH_CS_0	16:11	Output Port # This field specifies the output port number for the path.	R/W	CTRL port paths – path # Else - 0
0	PATH_CS_0	24:17	Path Credits Allocated This field specifies the initial value of the Credits Allocated field to be used by the receiver side of the path.	R/W	Path 0 - 2 PCIe port (1 path) – 7 Else - 0
0	PATH_CS_0	30:25	Reserved Must be set to 0.	RO	0
0	PATH_CS_0	31	Valid flag This flag is set to 1 if the path is enabled and set to 0 otherwise.	R/W	CTRL port paths – 1 Path 0 (CIO/ DMA) - 1 Else - 0
1	PATH_CS_1	7:0	Weight This specifies the WRR scheduler weight for the path. Weight 0 is reserved and must not be used.	R/W	Path 0-7 - 1 Others - 0

Table 63. Path Configuration Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
1	PATH_CS_1	10:8	Priority This specifies the priority level for the path. Priority 0 is the highest priority level and priority 7 is the lowest priority level.	R/W	0
1	PATH_CS_1	11	reserved	RO	0
1	PATH_CS_1	22:12	Counter ID This register specifies the performance counter that is used to collect statistics for the path. The Counter ID must be less than or equal to the maximum number of counters supported at the port.	R/W	0
1	PATH_CS_1	23	Counter Enable (CE) This flag is set to 1 if performance counters are enabled for the path and set to 0 if performance counters are disabled.	R/W	0
1	PATH_CS_1	24	Ingress Flow Control (IFC) Flag This flag must be set to 1 if path credits must be returned to the transmitter as packets are removed from the flow control buffer. If the flag is set to 0, no Credit Grant packets are sent upstream for this path. When set to 0 (path is not flow controlled) and packet should be dropped from the queue (due to lack of space) packet will be dropped from the queue tail.	R/W	CTRL port paths – 0 Path 0 (CIO/ DMA) - 1 PCIe - 1 Else - 0
1	PATH_CS_1	25	Egress Flow Control Flag (EFC) Flag This flag must be set to 1 if the transmitter at the output port must clear the path flow control check before packets are transmitted. If this flag is set to 0, the transmitter does not wait for flow control credits from a downstream receiver to transmit a packet on this path.	R/W	CTRL port paths – NA Path 0 (CIO) - 1 Else - 0
1	PATH_CS_1	26	Ingress Shared Buffering Enable (ISE) Flag This flag must be set to 1 if link credits must be returned to the transmitter as packets are dispatched from this path. If the flag is set to 0, no link Credit Grant packets are sent upstream for this path.	R/W	CTRL port paths – 1 Else-0
1	PATH_CS_1	27	Egress Shared Buffering Enable (ESE) Flag This flag must be set to 1 if the transmitter at the output port must clear the link flow control check before packets are transmitted. If this flag is set to 0, the transmitter does not wait for link flow control credits from a downstream receiver to transmit a packet on this path.	R/W	0
1	PATH_CS_1	28	Pending Requests Pending Requests exist (some Ingress FC buffers contain packets for this path).	RO	0

Table 63. Path Configuration Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
1	PATH_CS_1	29	Block Low Priority Paths (BLPP) This flag instructs the egress arbiter to wait for highest priority path and not to serve low priority. Enabling of this function may result in some utilization loss of egress port, but will ensure the highest priority paths are delivered as soon as egress port is ready. 0 – block low priority paths 1 – do not block low priority path	R/W	CTRL pot paths 1, Else 0
1	PATH_CS_1	31:30	DFT Bits Path(X) internal state for DFT: 31: valid. 30: path_gate_n[7] - result of Path FC gating function. Internal implementation register, not CIO Spec.	RO	0

4.3.4 Counters Configuration Space

Figure 30 shows the Counters configuration space registers that must be implemented by every CIO Switch that supports performance counters. Each performance counter is defined by a set of configuration registers that are described in Table 64. A performance counter may be associated with any HopID on a port and counts the number of received packets on that HopID and the number of packets dropped due to congestion.

Figure 30. Counters Configuration Space

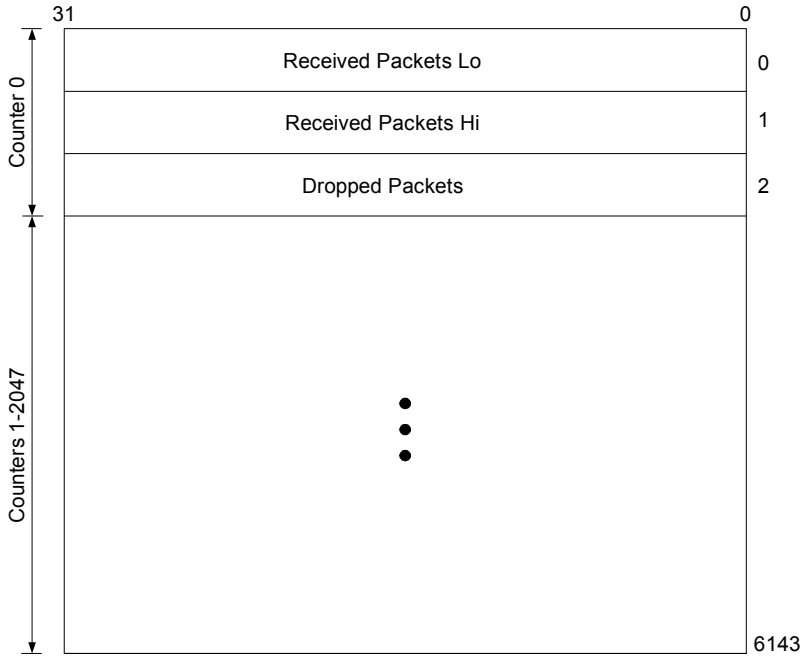


Table 64. Counters Configuration Register Attributes

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0	CNT_CS_0	31:0	Received Packets Low This register specifies the lower 32 bits of a 64-bit counter that is incremented once for every received packet on the path. The counter increments from 0 and saturates at 0xFFFFFFFFFFFFFFFF. Software can write to this counter to clear its value. Software must read the both doublewords of the Received Packets counter in one Read REQUEST. The counter implementation must ensure that the counter is read in an atomic fashion. Software can write to this counter to clear its value.	W/Clr	0
1	CNT_CS_1	31:0	Received Packets High This register specifies the upper 32 bits of a 64-bit counter that is incremented once for every received packet on the path. The counter increments from 0 and saturates at 0xFFFFFFFFFFFFFFFF. Software can write to this counter to clear its value. Software must read the both doublewords of the Received Packets counter in one Read REQUEST. The counter implementation must ensure that the counter is read in an atomic fashion. Software can write to this counter to clear its value.	W/Clr	0

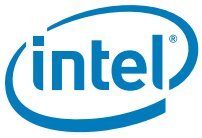


Table 64. Counters Configuration Register Attributes (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
2	CNT_CS_2	31:0	Dropped Packets This register specifies a 32-bit counter that is incremented once for every dropped packet on the path. The counter increments from 0 and saturates at 0xFFFFFFFF. Software can write to this counter to clear its value.	W/Clr	0

4.4 Host Interface

This section describes the software-visible elements of the host interface. The address space of the host interface is mapped into contiguous region of memory using a single PCI Express Base Address Register (BAR). The internal registers and memories may be accessed as direct memory-mapped offsets from the base address register.

Note: All the registers are accessed as whole 32-bit DWords and byte enables are ignored.

4.4.1 Register Summary

Table 165 provides a summary of all the programmer visible registers implemented in the host interface.

Table 65. Host interface Register Summary (N is the number of paths = 12)

Offset	Register Name	R/W	Section #
00000h – 001FCh	Transmit Ring Descriptors	R/W	
08000h – 081FCh	Receive Ring Descriptors	R/W	
18C00h – 18C0Ch	Receive Ring Control	R/W	
19400h	Receive Ring Status	RO	
19800h – 19BFCh	Transmit Table	R/W	
29800h – 29BFCh	Receive Table	R/W	
37800h – 37808h	Interrupt Status	R/Clr	
3780C - 37810	Interrupt cancel register	WO	
37814 - 37818	Interrupt set status	WO	
38200h – 38208h	Interrupt Mask	R/W	
38208 - 3820C	Interrupt Mask Cancel	WO	
38210 - 38214	Interrupt Mask Set	WO	
38C00h – 38C3Ch	Interrupt Throttling Rate	R/W	
38C40h – 0x38C6Ch	Interrupt Vector Allocation	R/W	

Table 65. Host interface Register Summary (N is the number of paths = 12) (Con-

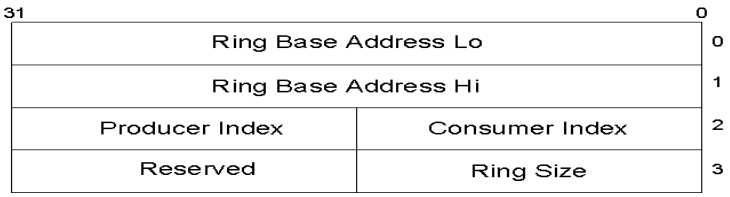
Offset	Register Name	R/W	Section #
39640h	Capabilities	RO	
39644h	Debug Mode Enable	R/W	
39648h	Debug Mode Command	R/W	
3964Ch – 3974Ch	Debug Mode Transmit Packet	R/W	
39750h – 39850h	Debug Mode Receive Packet	R/W	
39854h	PCIe Control Reset Request	R/W	
39858h	Host Interface Reset	R/W	
3985Ch	Snoop Mode Control	R/W	
39860h	DMA Time	RO	
39864h	DMA Miscellaneous	R/W	
39868h	Stop RX per path	R/W	
3986Ch	Thermo Sensor Level	R/W	
39870h	Link Credits State	RO	
39874h	Path Credits Avail	RO	

4.4.2 Register Descriptions

This section contains detailed register descriptions for the ring control and status registers and interrupt registers.

4.4.2.1 Transmit Ring Descriptors

Figure 31. Transmit Ring Descriptor Registers



The transmit ring descriptor shown in Figure 31, is a data structure that resides in the host interface internal registers and defines the circular array used to hold transmit buffer descriptors. The host interface provides one transmit ring per-path. The transmit ring descriptor defines the fields described in Table 66.

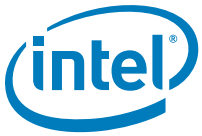


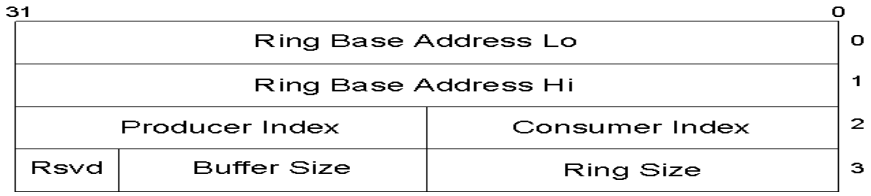
Table 66. Transmit Ring Descriptor Registers Fields[1]

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x00000 + (n * 0x10)	TX_RING_DESC_(n)_0	31:0	Ring Base Address Lo Lower 32 bits of the physical address of the ring in host memory. The ring base address must be aligned to 16 bytes. Therefore, the least significant 4-bits of the Ring Base Address Lo field must be 0. Writing to this register resets the Producer and Consumer indices to 0.	R/W	0
0x00004 + (n * 0x10)	TX_RING_DESC_(n)_1	31:0	Ring Base Address Hi Upper 32 bits of the physical address of the ring in host memory. Writing to this register resets the Producer and Consumer indices to 0.	R/W	0
0x00008 + (n * 0x10)	TX_RING_DESC_(n)_2	15:0	Consumer Index Index into the circular array that points to the next transmit buffer descriptor that must be processed by the segmentation engine. This index is updated by the host interface. Software writes to the consumer index are ignored by the host interface.	RO	0
0x00008 + (n * 0x10)	TX_RING_DESC_(n)_2	31:16	Producer Index Index of the next free location in the circular array into which a transmit buffer descriptor may be written. This index is updated by the host software.	R/W	0
0x0000C + (n * 0x10)	TX_RING_DESC_(n)_3	15:0	Ring Size Size of the ring in number of transmit buffer descriptors. Writing to this register resets the Producer and Consumer indices to 0.	R/W	0
0x0000C + (n * 0x10)	TX_RING_DESC_(n)_3	31:16	Reserved Reserved field that must be set to 0.	R/W	0

1. n = 0 till Total Paths-1

4.4.2.2 Receive Ring Descriptors

Figure 32. Receive Ring Descriptor Registers



The receive ring descriptor, shown in Figure 32, is a data structure that resides in host interface registers and defines the circular array used to hold the receive buffer descriptors. The host interface provides one receive ring per-path. The receive ring descriptor defines the fields described in Table 67.

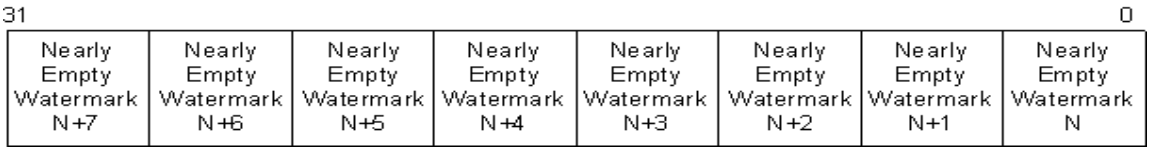
Table 67. Receive Ring Descriptor Registers Fields[1]

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x08000 + (n * 0x10)	RX_RING_DESC_(n)_0	31:0	Ring Base Address Lo Lower 32 bits of the physical address of the ring in host memory. The ring base address must be aligned to 16 bytes. Therefore, the least significant 4-bits of the Ring Base Address Lo field must be 0. Writing to this register resets the Producer and Consumer indices to 0.	R/W	0
0x08004 + (n * 0x10)	RX_RING_DESC_(n)_1	31:0	Ring Base Address Hi Upper 32 bits of the physical address of the ring in host memory. Writing to this register resets the Producer and Consumer indices to 0.	R/W	0
0x08008 + (n * 0x10)	RX_RING_DESC_(n)_2	15:0	Consumer Index Index into the circular array that points to the next receive buffer descriptor that must be processed by the system software. This index is updated by system software.	R/W	0
0x08008 + (n * 0x10)	RX_RING_DESC_(n)_2	31:16	Producer Index Index of the next free location in the circular array into which a receive buffer descriptor may be written. This index is updated by the host interface. Software writes to the producer index are ignored by the host interface.	RO	0
0x0800C + (n * 0x10)	RX_RING_DESC_(n)_3	15:0	Ring Size Size of the ring in number of receive buffer descriptors. Writing to this register resets the Producer and Consumer indices to 0.	R/W	0
0x0800C + (n * 0x10)	RX_RING_DESC_(n)_3	27:16	Buffer Size Size of the host buffers in bytes. The value 0 is assumed to indicate 4096. Therefore, the maximum buffer size is 4096 bytes.	R/W	0
0x0800C + (n * 0x10)	RX_RING_DESC_(n)_3	31:28	Reserved Reserved field that must be set to 0.	R/W	0

1. For this command the TBT2PCIE "Done" bit will not get cleared after the PCIE2TBT Valid bit was cleared as the device and the system are in their Sx entry flow
   n = 0 till Total Paths-1
   n = 0 till Total Paths-1
   n = 0/8/16/24
   n = 0 till Total Paths-1
   n = 0 till Total Paths-1
   m = 0 till 15 (number of interrupt vectors (MSIx)-1)
   # = 1 till 64
   # = 1 till 64
   The values are decided by the no_soft_reset bit which is input to the design

4.4.2.3 Receive Ring Control

Figure 33. Receive Ring Control Register



There are a total of four Receive Ring Control registers (for 32 paths supported by the host interface). As shown in Figure 33, each register specifies the configuration for eight receive rings N+0 to N+7 where N is 0, 8, 16 and 24.

The Receive Ring Control registers specify the Nearly Empty Watermark for the receive rings as shown in Table 68.

Table 68. Receive Ring Control Register Fields[1]

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x18C00 + (n/8 * 0x4)	RX_RING_CTRL_(N)	3:0	Nearly Empty Watermark (N) Specified as the number of entries from the bottom of the ring. The usable range of the Nearly Empty Watermark must be less than ½ the ring size. The encoding of the Nearly Empty Watermark is identical to the encoding of the Nearly Full Watermark specified in Table 69.	R/W	0
0x18C00 + (n/8 * 0x4)	RX_RING_CTRL_(N)	7:4	Nearly Empty Watermark (N + 1)	R/W	0
0x18C00 + (n/8 * 0x4)	RX_RING_CTRL_(N)	11:8	Nearly Empty Watermark (N + 2)	R/W	0
0x18C00 + (n/8 * 0x4)	RX_RING_CTRL_(N)	15:12	Nearly Empty Watermark (N + 3)	R/W	0
0x18C00 + (n/8 * 0x4)	RX_RING_CTRL_(N)	19:16	Nearly Empty Watermark (N + 4)	R/W	0
0x18C00 + (n/8 * 0x4)	RX_RING_CTRL_(N)	23:20	Nearly Empty Watermark (N + 5)	R/W	0

Table 68. Receive Ring Control Register Fields[1] (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x18C00 + (n/8 * 0x4)	RX_RING_CTRL_(N)	27:24	Nearly Empty Watermark (N + 6)	R/W	0
0x18C00 + (n/8 * 0x4)	RX_RING_CTRL_(N)	31:28	Nearly Empty Watermark (N + 7)	R/W	0

1. For this command the TBT2PCIE "Done" bit will not get cleared after the PCIE2TBT Valid bit was cleared as the device and the system are in their Sx entry flow
n = 0 till Total Paths-1
n = 0 till Total Paths-1
n = 0/8/16/24
n = 0 till Total Paths-1
n = 0 till Total Paths-1
m = 0 till 15 (number of interrupt vectors (MSIx)-1)
# = 1 till 64
# = 1 till 64
The values are decided by the no_soft_reset bit which is input to the design

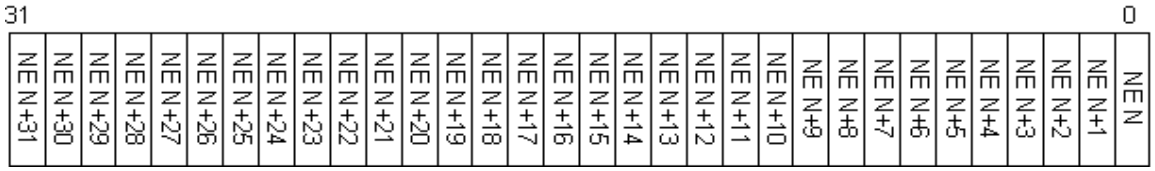
Table 69. Nearly Empty Watermark Encoding

Nearly Full Watermark	Number of Entries
1	1
2	2
3	4
4	8
5	16
6	32
7	64
8	128
9	256
10	512
11	1024
12	2048
13	4096
14	8192
15	16384

4.4.2.4 Receive Ring Status

There is one Receive Ring Status register (32 bits for 32 paths supported by the host interface). As shown in Figure 34, the register contains the nearly-empty status bits for 32 receive rings (N=0).

Figure 34. Receive Ring Status Register



The Status register fields are described in Table 70:

Table 70. Receive Ring Status Register Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x19400	RX_RING_STAT	0	Nearly Empty 0 If a receive ring has less entries than specified by the Nearly Empty Watermark value for that ring, this status bit is set. If the number of entries in the receive ring is greater than the Nearly Empty Watermark, this bit is cleared.	RO	0
0x19400	RX_RING_STAT	1	Nearly Empty 1	RO	0
0x19400	RX_RING_STAT	2	Nearly Empty 2	RO	0
0x19400	RX_RING_STAT	3	Nearly Empty 3	RO	0
0x19400	RX_RING_STAT	4	Nearly Empty 4	RO	0
0x19400	RX_RING_STAT	5	Nearly Empty 5	RO	0
0x19400	RX_RING_STAT	6	Nearly Empty 6	RO	0
0x19400	RX_RING_STAT	7	Nearly Empty 7	RO	0
0x19400	RX_RING_STAT	8	Nearly Empty 8	RO	0
0x19400	RX_RING_STAT	9	Nearly Empty 9	RO	0
0x19400	RX_RING_STAT	10	Nearly Empty 10	RO	0
0x19400	RX_RING_STAT	11	Nearly Empty 11	RO	0
0x19400	RX_RING_STAT	12	Nearly Empty 12	RO	0
0x19400	RX_RING_STAT	13	Nearly Empty 13	RO	0
0x19400	RX_RING_STAT	14	Nearly Empty 14	RO	0
0x19400	RX_RING_STAT	15	Nearly Empty 15	RO	0
0x19400	RX_RING_STAT	16	Nearly Empty 16	RO	0
0x19400	RX_RING_STAT	17	Nearly Empty 17	RO	0
0x19400	RX_RING_STAT	18	Nearly Empty 18	RO	0
0x19400	RX_RING_STAT	19	Nearly Empty 19	RO	0
0x19400	RX_RING_STAT	20	Nearly Empty 20	RO	0
0x19400	RX_RING_STAT	21	Nearly Empty 21	RO	0
0x19400	RX_RING_STAT	22	Nearly Empty 22	RO	0
0x19400	RX_RING_STAT	23	Nearly Empty 23	RO	0
0x19400	RX_RING_STAT	24	Nearly Empty 24	RO	0
0x19400	RX_RING_STAT	25	Nearly Empty 25	RO	0
0x19400	RX_RING_STAT	26	Nearly Empty 26	RO	0
0x19400	RX_RING_STAT	27	Nearly Empty 27	RO	0
0x19400	RX_RING_STAT	28	Nearly Empty 28	RO	0
0x19400	RX_RING_STAT	29	Nearly Empty 29	RO	0
0x19400	RX_RING_STAT	30	Nearly Empty 30	RO	0

Table 70. Receive Ring Status Register Fields (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x19400	RX_RING_STAT	31	Nearly Empty 31	RO	0

4.4.2.5 Transmit Table

The transmit table is a data structure that resides in host interface internal memory and is used by the segmentation engine to segment a Frame into CIO packets. The transmit table contains one entry per path. The format of the transmit table entry is shown in Figure 36. The shaded area represents a working copy of the current transmit buffer descriptor maintained by the segmentation engine during transmit. The non-shaded area contains configuration parameters that must be programmed by software. The description of various fields is given in Table 71.

Figure 35. Transmit Table Entry

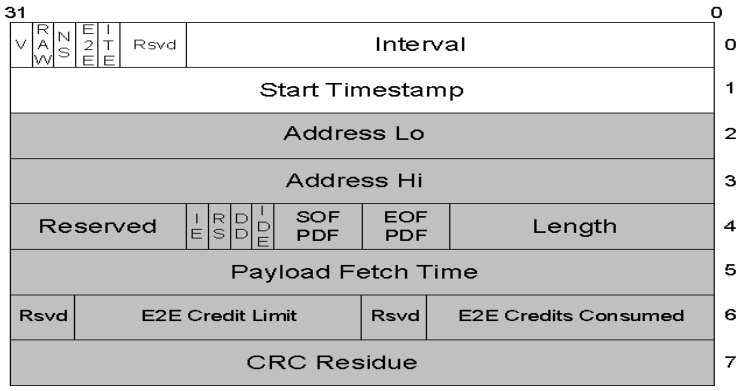


Table 71. Transmit Table Entry Fields[1]

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x19800 + (n * 0x20)	TX_TABLE_(n)_0	23:0	Interval If the Isochronous Transmit Enable (ITE) bit is set to 1, this field specifies the interval between the eligibility times for payload DMA. The resolution of this time is 256ns.	R/W	0
0x19800 + (n * 0x20)	TX_TABLE_(n)_0	26:24	Reserved Must be set to 0.	R/W	0
0x19800 + (n * 0x20)	TX_TABLE_(n)_0	27	Isochronous Transmit Enable (ITE) When set to 1, this bit specifies that the payload eligibility time for isochronous DMA must be calculated using the Start Timestamp and Interval fields. When set to 0, the payload eligibility time is given by the Payload Fetch Time in the transmit buffer descriptor. This bit is only valid when the Isochronous DMA Enable (IDE) bit is set to 1 in the transmit buffer descriptor.	R/W	0

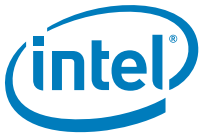


Table 71. Transmit Table Entry Fields[1] (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x19800 + (n * 0x20)	TX_TABLE_(n)_0	28	End-to-End Flow Control Enable (E2E) When set to 1, end-to-end flow control is enabled for the path. When set to 0, end-to-end flow control is disabled.	R/W	0
0x19800 + (n * 0x20)	TX_TABLE_(n)_0	29	No-snoop flag (NS) This flag is set to 1 by software if the PCIe no-snoop attribute must be set for all host-memory accesses resulting from the transmission of a CIO packet on this transmit table entry. This applies to all memory reads and writes to the transmit buffer descriptors and memory reads for the packet payload.	R/W	0
0x19800 + (n * 0x20)	TX_TABLE_(n)_0	30	Raw flag This flag is set to 0 by software if frame mode is used for the path or 1 if raw mode is used. This field is initialized by system software.	R/W	0
0x19800 + (n * 0x20)	TX_TABLE_(n)_0	31	Valid flag (V) This flag is set to 1 if the transmit table entry is enabled. If set to 0, the segmentation engine ignores the transmit table entry.	R/W	0
0x19804 + (n * 0x20)	TX_TABLE_(n)_1	31:0	Start Timestamp If the Isochronous Transmit Enable (ITE) bit is set to 1, this field specifies the absolute time at which the path becomes eligible for isochronous DMA for the first time. The resolution of this time is 256ns.	R/W	0
0x19808 + (n * 0x20)	TX_TABLE_(n)_2	31:0	Address Lo Lower 32 bits of the physical address pointing to a location within the host buffer from which the next CIO packet must be formed for transmission.	RO	NA
0x1980C + (n * 0x20)	TX_TABLE_(n)_3	31:0	Address Hi Upper 32 bits of the physical address pointing to a location within the host buffer from which the next CIO packet must be formed for transmission. The address fields are set to the sum of the address field in the transmit buffer descriptor and the offset field when a new buffer descriptor is removed from the transmit ring. The segmentation engine updates the address fields after every CIO packet transmission.	RO	NA
0x19810 + (n * 0x20)	TX_TABLE_(n)_4	11:0	Length Length of the host buffer payload in bytes that is yet to be transmitted. This field is initialized using the length field in the transmit buffer descriptor and is updated by the segmentation engine after every CIO packet transmission.	RO	NA

Table 71. Transmit Table Entry Fields[1] (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x19810 + (n * 0x20)	TX_TABLE_(n)_4	15:12	EOF Protocol Defined Field (EOF PDF) The value that must be inserted into the PDF field of the CIO packet header for the last packet of the frame. If the frame fits entirely within a single CIO packet, this field is inserted into the PDF field of the CIO packet header. This field is copied from the transmit buffer descriptor of the frame being transmitted.	RO	NA
0x19810 + (n * 0x20)	TX_TABLE_(n)_4	19:16	SOF Protocol Defined Field (SOF PDF) The value that must be inserted into the PDF field of the CIO packet header for the first packet of the frame. If the frame fits entirely within a single CIO packet, this field is ignored. This field is copied from the transmit buffer descriptor of the frame being transmitted.	RO	NA
0x19810 + (n * 0x20)	TX_TABLE_(n)_4	20	Isochronous DMA Enable (IDE) This bit must be set to 1 if the DMA of the buffer payload from host memory must be performed no earlier than the next eligible time. The next eligible time is the Payload Fetch Time if the Isochronous Transmit Enable (ITE) bit is set to 0 in the corresponding transmit table entry. If the ITE bit is set to 1, the next eligible time is determined based on the Start Time and Interval fields in the corresponding transmit table entry. This field is copied from the transmit buffer descriptor of the frame being transmitted.	RO	NA
0x19810 + (n * 0x20)	TX_TABLE_(n)_4	21	Descriptor Done (DD) This bit is set to 1 by the host interface after the transmit buffer descriptor is completely processed. This bit is only valid if the Request Status bit was set. This bit is copied from the transmit buffer descriptor of the frame being transmitted.	RO	NA
0x19810 + (n * 0x20)	TX_TABLE_(n)_4	22	Request Status (RS) This bit must be set to 1 if the host interface must report the transmit status information for this buffer descriptor. The status is reported in the Descriptor Done (DD) bit. This bit is copied from the transmit buffer descriptor of the frame being transmitted.	RO	NA
0x19810 + (n * 0x20)	TX_TABLE_(n)_4	23	Interrupt Enable (IE) This bit must be set to 1 if an interrupt is to be generated when the buffer descriptor is completely processed by the host interface. This bit is copied from the transmit buffer descriptor of the frame being transmitted.	RO	NA
0x19810 + (n * 0x20)	TX_TABLE_(n)_4	31:24	Reserved Must be set to 0.	R/W	0

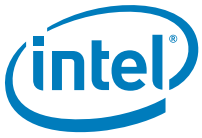


Table 71. Transmit Table Entry Fields[1] (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x19814 + (n * 0x20)	TX_TABLE_(n)_5	31:0	Payload Fetch Time When the IDE bit is set to 1, this field specifies the absolute time at which the payload is eligible for DMA from host memory. This time has a resolution of 256ns. This bit is copied from the transmit buffer descriptor of the frame being transmitted.	RO	NA
0x19818 + (n * 0x20)	TX_TABLE_(n)_6	12:0	E2E Credits Consumed This field specifies the value of the Credits Consumed register for the path's end-to-end credit based flow control. This field is updated by the segmentation engine when a packet is transmitted from this transmit table entry.	RO	NA
0x19818 + (n * 0x20)	TX_TABLE_(n)_6	15:13	Reserved Must be set to 0.	R/W	0
0x19818 + (n * 0x20)	TX_TABLE_(n)_6	28:16	E2E Credit Limit This field specifies the value of the Credit Limit register for the path's end-to-end credit based flow control. This field is updated by the reassembly engine when it receives a end-to-end flow control update for this path.	RO	NA
0x19818 + (n * 0x20)	TX_TABLE_(n)_6	31:29	Reserved Must be set to 0.	R/W	0
0x1981C + (n * 0x20)	TX_TABLE_(n)_7	31:0	CRC Residue Running CRC residue computed over the bytes of the host buffer that have been transmitted. This field is only valid in the frame mode. This field is initialized by the segmentation engine when a new transmit buffer descriptor is removed from the transmit ring and is updated after every CIO packet transmission on this HopID. The final CRC value computed after the last CIO packet is formed is appended to the payload. If there is no space in the CIO packet payload to append the CRC, a new CIO packet is generated that contains the CRC value.	RO	NA

1. For this command the TBT2PCIE "Done" bit will not get cleared after the PCIE2TBT Valid bit was cleared as the device and the system are in their Sx entry flow
   n = 0 till Total Paths-1
   n = 0 till Total Paths-1
   n = 0/8/16/24
   n = 0 till Total Paths-1
   n = 0 till Total Paths-1
   m = 0 till 15 (number of interrupt vectors (MSIx)-1)
   # = 1 till 64
   # = 1 till 64
   The values are decided by the no_soft_reset bit which is input to the design

4.4.2.6 Receive Table

The receive table is a data structure that resides in host interface internal memory and is used by the reassembly engine to assembly a frame from received CIO packets. The receive table contains one entry per path.

The format of the receive table entry is shown in Figure 37. The shaded area represents a working copy of the current receive buffer descriptor maintained by the reassembly engine during receive.

The non-shaded area contains configuration parameters that must be programmed by software. The description of various fields is given in Table 72.

Figure 36. Receive Table Entry

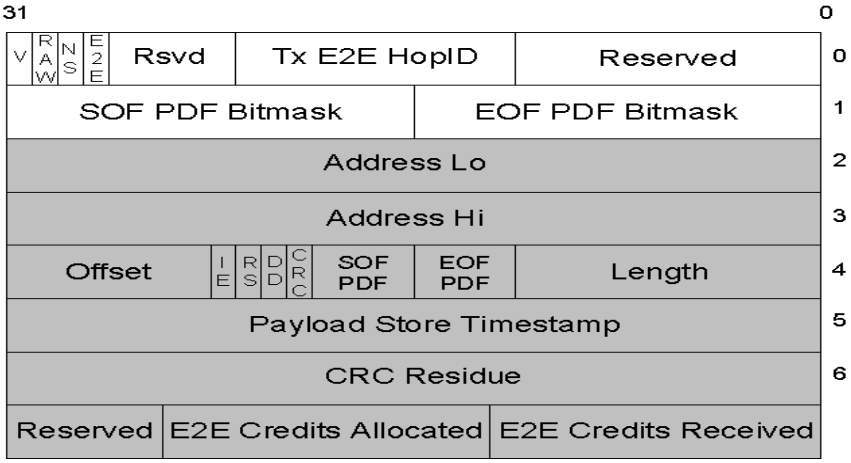


Table 72. Receive Table Entry Fields[1]

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x29800 + (n * 0x20)	RX_TABLE_(n)_0	11:0	Reserved Must be set to 0.	RO	0
0x29800 + (n * 0x20)	RX_TABLE_(n)_0	22:12	Tx E2E HopID This field specifies the HopID of the transmit path that must receive flow control updates received on the HopID associated with the receive table entry. This field is only valid if the E2E bit is set to 1.	R/W	0
0x29800 + (n * 0x20)	RX_TABLE_(n)_0	27:23	Reserved Must be set to 0.	R/W	0
0x29800 + (n * 0x20)	RX_TABLE_(n)_0	28	End-to-End Flow Control Enable (E2E) When set to 1, end-to-end flow control is enabled for the path. When set to 0, end-to-end flow control is disabled.	R/W	0

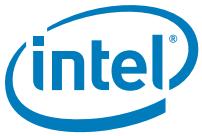


Table 72. Receive Table Entry Fields[1] (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x29800 + (n * 0x20)	RX_TABLE_(n)_0	29	No-snoop flag (NS) This flag is set to 1 by software if the PCIe no-snoop attribute must be set for all host-memory accesses resulting from the reception of a CIO packet on this receive table entry. This applies to all memory reads and writes to the receive buffer descriptors and memory writes for the packet payload.	R/W	0
0x29800 + (n * 0x20)	RX_TABLE_(n)_0	30	Raw flag This flag is set to 0 by software if frame mode is used for the path or 1 if raw mode is used. This field is initialized by system software.	R/W	0
0x29800 + (n * 0x20)	RX_TABLE_(n)_0	31	Valid flag This flag is set to 1 if the receive table entry is enabled. If set to 0, the reassembly engine ignores the receive table entry.	R/W	0
0x29804 + (n * 0x20)	RX_TABLE_(n)_1	15:0	EOF PDF Bitmask This field is initialized by system software. It specifies all the PDF field values that may be interpreted as an End of Frame (EOF) marker. If the bit at the position given by the PDF field value in a received CIO packet is set, then the end of the current frame is indicated and the reassembly engine puts the reassembled frame onto the receive ring.	R/W	0
0x29804 + (n * 0x20)	RX_TABLE_(n)_1	31:16	SOF PDF Bitmask This field is initialized by system software. It specifies all the PDF field values that may be interpreted as a Start of Frame (SOF) marker. If the bit at the position given by the PDF field value in a received CIO packet is set, then the start of a new frame is indicated fetches a new buffer descriptor from the free list.	R/W	0
0x29808 + (n * 0x20)	RX_TABLE_(n)_2	31:0	Address Lo Lower 32 bits of the physical address of the buffer in host memory.	RO	0
0x2980C + (n * 0x20)	RX_TABLE_(n)_3	31:0	Address Hi Upper 32 bits of the physical address of the buffer in host memory. The address fields point to the starting address of the host buffer and are initialized using the values contained in the free buffer descriptor used to reassemble the frame. They are not modified during frame reassembly.	RO	0

Table 72. Receive Table Entry Fields[1] (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x29810 + (n * 0x20)	RX_TABLE_(n)_4	11:0	Length Length of the received packet or frame host in bytes. This field is initialized to 0 when a new receive buffer descriptor is fetched from the receive ring. It is incremented by the length of the received CIO packet. The value of (offset + length) is added to the address fields to obtain the starting address for the DMA transfer when the CIO packet payload is transferred to the receive buffer. At the end of the reassembly process, this field contains the total length of the received frame.	RO	0
0x29810 + (n * 0x20)	RX_TABLE_(n)_4	15:12	EOF PDF This field contains the PDF values of the last packet of the frame. If the received frame fit entirely within a single CIO packet, this field contains the PDF value from that packet.	RO	0
0x29810 + (n * 0x20)	RX_TABLE_(n)_4	19:16	SOF PDF This field contains the PDF value of the first packet of the frame. This field is set to 0 if the frame fits entirely within one CIO packet.	RO	0
0x29810 + (n * 0x20)	RX_TABLE_(n)_4	20	CRC Error In Frame mode, this bit is set to 1 if the CRC check failed for the reassembled frame and set to 0 if the CRC check passed. In Raw mode, this bit is always set to 0.	RO	0
0x29810 + (n * 0x20)	RX_TABLE_(n)_4	21	Descriptor Done (DD) This bit is set to 1 by the host interface after the receive buffer descriptor is completely processed. This bit is only valid if the Request Status bit was set.	RO	0
0x29810 + (n * 0x20)	RX_TABLE_(n)_4	22	Request Status (RS) This bit must be set to 1 if the host interface must report the receive status information for this buffer descriptor. The status is reported in the Descriptor Done (DD) bit.	RO	0
0x29810 + (n * 0x20)	RX_TABLE_(n)_4	23	Interrupt Enable (IE) This bit must be set to 1 if an interrupt is to be generated when the receive buffer descriptor is completely processed by the host interface.	RO	0
0x29810 + (n * 0x20)	RX_TABLE_(n)_4	31:24	Offset The location of the first byte of the CIO packet or Frame from the beginning of the buffer. This field is initialized from the value contained in the receive buffer descriptor and is unmodified by the reassembly engine.	RO	0
0x29814 + (n * 0x20)	RX_TABLE_(n)_5	31:0	Payload Store Timestamp This field specifies the absolute time when the payload of the first CIO packet of a frame was transferred to host memory by the reassembly engine. The resolution of this timestamp is 256ns.	RO	0

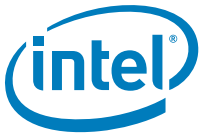


Table 72. Receive Table Entry Fields[1] (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x29818 + (n * 0x20)	RX_TABLE_(n)_6	31:0	CRC Residue Running CRC residue computed over the payload bytes of received CIO packets. This field is initialized by the reassembly engine when a new receive buffer descriptor is fetched and is updated after every CIO packet reception on the associated HopID. The final CRC value computed after the last CIO packet is received is compared to the CRC value appended to the end of the frame payload by the transmitter. If the CRC values do not match, the CRC error flag is set in the receive buffer descriptor.	RO	0
0x2981C + (n * 0x20)	RX_TABLE_(n)_7	12:0	E2E Credits Received This field specifies the value of the Credits Received register for the path's end-to-end credit based flow control. This field is updated by the reassembly engine when the producer index of the receive ring associated with this receive table entry is incremented.	RO	0
0x2981C + (n * 0x20)	RX_TABLE_(n)_7	25:13	E2E Credits Allocated This field specifies the value of the Credits Allocated register for the path's end-to-end credit based flow control. This field is updated by the reassembly engine when the consumer index of the receive ring associated with this receive table entry is incremented.	RO	0
0x2981C + (n * 0x20)	RX_TABLE_(n)_7	31:26	Reserved Must be set to 0.	R/W	0

1. For this command the TBT2PCIE "Done" bit will not get cleared after the PCIE2TBT Valid bit was cleared as the device and the system are in their Sx entry flow
n = 0 till Total Paths-1
n = 0 till Total Paths-1
n = 0/8/16/24
n = 0 till Total Paths-1
n = 0 till Total Paths-1
m = 0 till 15 (number of interrupt vectors (MSIx)-1)
# = 1 till 64
# = 1 till 64
The values are decided by the no_soft_reset bit which is input to the design

4.4.2.7 Interrupt Status

The host interface may be configured to issue interrupts when one or more of the following interrupt events occur.

- Receive ring occupancy is below the nearly-empty watermark.
- Transmit buffer descriptor has been processed and status updated.
- Receive buffer descriptor has been processed and status updated.

The Interrupt Status registers define a bit corresponding to each interrupt event. When an interrupt event occurs, the corresponding bit is set to 1 by the host interface. This may result in an interrupt being issued to the host. System software can determine the source of the interrupt by reading the Interrupt Status registers.

There are two Interrupt Status registers. The number of bit represents the number of path as described in Table 73. Bit 0 is the status bit of ring 0 (path 0) and so on.

Table 73. Interrupt Status Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x37800	ISR_0	11:0	Transmit Buffer Descriptor Processed 0-11 12 status bits for the 12 rings (12 paths).	R/Clr	0
		23:12	Receive Buffer Descriptor Processed 0-11 12 status bits for the 12 rings (12 paths).	R/Clr	0
		31:24	Receive Ring Nearly Empty 0-7 8 status bits for the 8 rings (8 paths).	R/Clr	0
0x37804	ISR_1	3:0	Receive Ring Nearly Empty 8-11 4 status bits for the 4 rings (4 paths).	R/Clr	0

Table 74. Interrupt Cancel Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x3780C	ICS_0	31:0	Setting specific bit in this register will cancel corresponding bit in Interrupt Status register	WO	0
0x37810	ICS_1	3:0	Setting specific bit in this register will cancel corresponding bit in Interrupt Status register	WO	0

Table 75. Interrupt Set Status Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x37914	ISS_0	31:0	Setting specific bit in this register will set corresponding bit in Interrupt Status register	WO	0

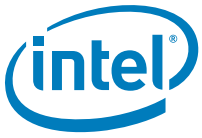


Table 75. Interrupt Set Status Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x37918	ISS_1	3:0	Setting specific bit in this register will set corresponding bit in Interrupt Status register	WO	0

4.4.2.8 Interrupt Mask

Multiple Interrupt Mask registers are provided to correspond to the number of Interrupt Status registers, as described in Table 76. System software may enable/disable interrupts. By writing a value of 1 to the bits of the Interrupt Mask register it will enable the corresponding interrupts.

Table 76. Interrupt Mask Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x38200	IMR_0	11:0	Transmit Buffer Descriptor Processed 0-11 12 status bits for the 12 rings (12 paths).	R/W	0
		23:12	Receive Buffer Descriptor Processed 0-11 12 status bits for the 12 rings (12 paths).	R/W	0
		31:24	Receive Ring Nearly Empty 0-7 8 status bits for the 8 rings (8 paths).	R/W	0
0x38204	IMR_1	3:0	Receive Ring Nearly Empty 8-11 4 status bits for the 4 rings (4 paths).	R/W	0
		31:4	Reserved	R/W	

Table 77. Interrupt Mask Cancel Registers Fields

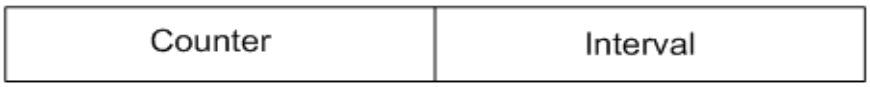
Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x38208	IMC_0	31:0	Setting specific bit in this register, will cancel corresponding bit in Interrupt Mask register	WO	0
0x3820C	IMC_1	3:0	Setting specific bit in this register, will cancel corresponding bit in Interrupt Mask register	WO	0
		31:4	Reserved	WO	0

Table 78. Interrupt Mask Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x38210	IMS_0	31:0	Setting specific bit in this register, will set corresponding bit in Interrupt Mask register	WO	0
0x38214	IMS_1	3:0	Setting specific bit in this register, will set corresponding bit in Interrupt Mask register	WO	0
		31:4	Reserved	WO	0

4.4.2.9 Interrupt Throttling Rate

Figure 37. Interrupt Throttling Rate Register



The Interrupt Throttling Rate (ITR) register (Figure 37) may be used to pace the delivery of interrupts to the host CPU. The format of the ITR is described in Table 79. There are 16 registers, one for each interrupt vector (MSIx).

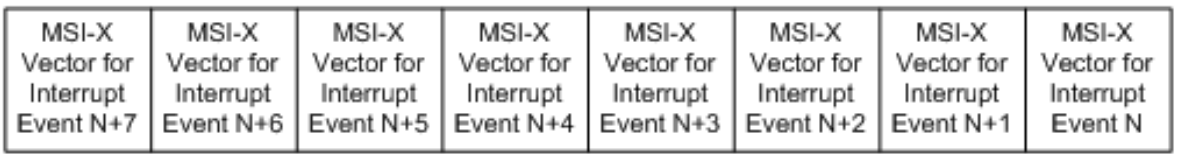
Table 79. Interrupt Throttling Rate Register Fields[1]

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x38C00 + (m * 0x4)	ITR_(m)	15:0	Interval Minimum inter-interrupt interval. The interval is specified in 256ns increments. Setting this bit to 0 disables the interrupt throttling logic. This field has the value 0 on reset.	R/W	0
0x38C00 + (m * 0x4)	ITR_(m)	31:16	Counter Down Counter. Loaded with interval value each time the interrupt is signaled. Counts down to zero and stops. The interrupt is signaled each time this counter is zero and an Interrupt Status register bit is set. This counter can be directly written by software at any time to alter the throttling performance.	R/W S	

1. For this command the TBT2PCIE "Done" bit will not get cleared after the PCIE2TBT Valid bit was cleared as the device and the system are in their Sx entry flow
n = 0 till Total Paths-1
n = 0 till Total Paths-1
n = 0/8/16/24
n = 0 till Total Paths-1
n = 0 till Total Paths-1
m = 0 till 15 (number of interrupt vectors (MSIx)-1)
# = 1 till 64
# = 1 till 64
The values are decided by the no_soft_reset bit which is input to the design

4.4.2.10 Interrupt Vector Allocation

Figure 38. Interrupt Vector Allocation Register



The Interrupt Vector Allocation registers control the assignment of the 16 MSI-X vectors to individual interrupt events.

The total number of IVAR registers is (3*N)/8 where N is the number of paths. As shown in Figure 38, each register specifies the mapping for 8 interrupt events N+0 through N+7 where N is 0, 8, 16, … (3*P - 8).

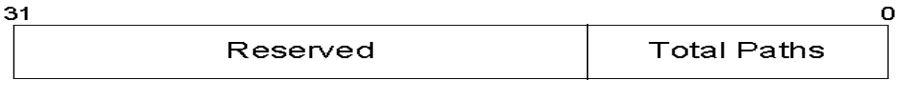
The association of IVAR registers to individual interrupt events is described in Table 80.

Table 80. Interrupt Vector Allocation Register Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x38C40	IVR_0	31:0	Transmit Buffer Descriptor Processed – ring 0-7 Vector Allocation	R/W	0
0x38C44	IVR_1	15:0	Transmit Buffer Descriptor Processed – ring 8-11 Vector Allocation	R/W	0
		31:16	Receive Buffer Descriptor Processed – ring 0-3 Vector Allocation	R/W	0
0x38C48	IVR_2	31:0	Receive Buffer Descriptor Processed – ring 4-11 Vector Allocation	R/W	0
0x38C4C	IVR_3	31:0	Receive Ring Nearly Empty – ring 0-7 Vector Allocation	R/W	0
0x38C50	IVR_4	15:0	Receive Ring Nearly Empty – ring 8-11 Vector Allocation	R/W	0
		31:16	Reserved	R/W	0

4.4.2.11 Host interface Capabilities

Figure 39. Host interface Capabilities Register



The Capabilities register shown in Figure 39, specifies the parameters supported by the host interface. The Capabilities register fields is described in Table 81.

Table 81. Host interface Capabilities Register Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x39640	HOST_ INTERFACE_ CAPABILITIES	10:0	Total Paths The total number of transmit and receive paths supported by the interface.	RO	0x0C
0x39640	HOST_ INTERFACE_ CAPABILITIES	31:11	Reserved Reserved bits. Must be set to 0.	R/W	0

4.4.2.12 Debug Mode Enable

Figure 40. Debug Mode Enable Register

The Debug Mode Enable register, shown in Figure 40, is used to put the host interface into debug mode. If Enable bit (bit 0) of the Debug Mode Enable register is set to 1 the host interface resets and goes into debug mode.

If the Enable bit is set to 0, the host interface resets and resumes normal operation. The default value for the Enable bit is 0 (see Table 78).

Table 82. Debug Mode Enable Register Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x39644	DEBUG_MODE_EN	0	Enable If The Enable bit set to 1 the host interface resets and goes into debug mode. If the Enable bit is set to 0, the host interface resets and resumes normal operation. The default value for the Enable bit is 0.	R/W	0
0x39644	DEBUG_MODE_EN	31:1	Reserved Must be set to 0.	R/W	0

4.4.2.13 Debug Mode Command

Figure 41. Debug Mode Command Register

The Debug Mode Command register shown in Figure 41 is used to issue transmit and receive commands to the host interface in the debug mode. The format of this register is described in Table 83.

Table 83. Debug Mode Command Register Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x39648	DEBUG_MODE_CMD	0	Transmit Ready (TR) This bit is set to 1 by software to initiate the transmission of a CIO packet (specified in the Debug Mode Transmit Packet registers) in the debug mode. After the transmission of the packet completes, the host interface clears the bit. Software must poll and ensure that this bit is clear before it attempts to transmit a packet. Software writes to clear this bit are ignored.	R/W SC	0

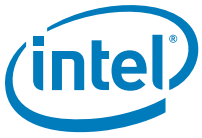
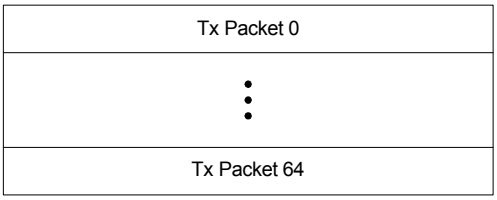


Table 83. Debug Mode Command Register Fields (Continued)

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x39648	DEBUG_MODE_CMD	1	Receive Ready (RR) This bit is set to 1 by software to indicate that it is ready to receive a packet in the debug mode. When this bit is set to 1, the host interface places the next received CIO packet into the Debug Mode Receive Packet registers and clears the bit. Software must poll and ensure that this bit is clear before it attempts to read the packet header and contents from the Debug Mode Receive Packet registers. Software writes to clear this bit are ignored.	R/W SC	0
0x39648	DEBUG_MODE_CMD	31:2	Reserved. Must be set to 0.	R/W	0

4.4.2.14 Debug Mode Transmit Packet

Figure 42. Debug Mode Packet Transmit Registers



The Debug Mode Transmit Packet registers, shown in Figure 42, consist of a set of 65 registers that may be used by software to construct and transmit a CIO packet in the debug mode.

The Tx Packet 0 register specifies the CIO packet header and the Tx Packet 1 through Tx Packet 64 registers specifies the CIO packet payload, as described in Table 84. The actual number of double words transmitted is determined based on the Length field of the CIO packet header.

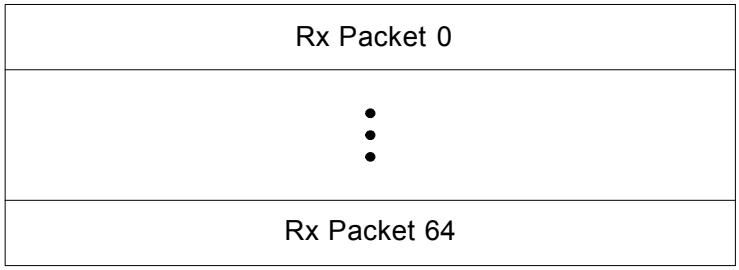
Table 84. Debug Mode Packet Transmit Registers Fields[1]

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x3964C	DEBUG_TX_PKT_0	31:0	CIO packet header	R/W	0
0x39650-0x3974C	DEBUG_TX_PKT_#	31:0	CIO packet payload	R/W	0

1. For this command the TBT2PCIE "Done" bit will not get cleared after the PCIE2TBT Valid bit was cleared as the device and the system are in their Sx entry flow
   n = 0 till Total Paths-1
   n = 0 till Total Paths-1
   n = 0/8/16/24
   n = 0 till Total Paths-1
   n = 0 till Total Paths-1
   m = 0 till 15 (number of interrupt vectors (MSIx)-1)
   # = 1 till 64
   # = 1 till 64
   The values are decided by the no_soft_reset bit which is input to the design

4.4.2.15 Debug Mode Receive Packet

Figure 43. Debug Mode Packet Receive Registers



The Debug Mode Receive Packet registers shown in Figure 43, consist of a set of 65 registers that may be used by software to receive a CIO packet in debug mode. The Rx Packet 0 register contains the CIO packet header and the Rx Packet 1 through Rx Packet 64 registers contains the received CIO packet payload, as described in Table 85. The actual number of double words received must be determined based on the Length field of the CIO packet header.

Table 85. Debug Mode Packet Receive Registers Fields[1]

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x39750	DEBUG_RX_PKT_0	31:0	CIO packet header	R/W S	0
0x39754-0x39850	DEBUG_RX_PKT_#	31:0	CIO packet payload	R/W S	0

1. For this command the TBT2PCIE "Done" bit will not get cleared after the PCIE2TBT Valid bit was cleared as the device and the system are in their Sx entry flow
n = 0 till Total Paths-1
n = 0 till Total Paths-1
n = 0/8/16/24
n = 0 till Total Paths-1
n = 0 till Total Paths-1
m = 0 till 15 (number of interrupt vectors (MSIx)-1)
# = 1 till 64
# = 1 till 64
The values are decided by the no_soft_reset bit which is input to the design

4.4.2.16 Host Interface Reset

Figure 44. Host Interface Reset Register

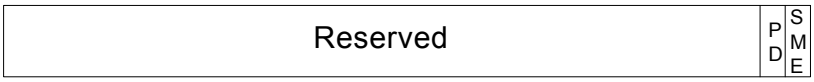
The Host Interface Reset register shown in Figure 44 is used to reset the host interface. The format of this register is described in Table 86.

Table 86. Host Interface Reset Register Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x39858	HOST_RESET	0	RST Software must set the RST bit (bit 0) of the Host Interface Reset register to 1 to reset the host interface. After the reset is complete the RST bit is cleared by the host interface. When the Host Interface is reset, all the internal transmit and receive structures are initialized to their default values. The Host Interface continues to operate in the same mode – debug, snoop or normal mode – after the reset.	R/W SC	0
0x39858	HOST_RESET	31:1	Reserved Must be set to 0.	R/W	0

4.4.2.17 Snoop Mode Control

Figure 45. Snoop Mode Control Register



The Snoop Mode Control register shown in Figure 45 is used to put the host interface into snoop mode. The format of this register is described in Table 87.

Table 87. Snoop Mode Control Register Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x3985C	SNOOP_MODE	0	Snoop Mode Enable (SME) This bit is set to 1 by software to put the Host Interface receive side into snoop mode. To bring the Host Interface out of snoop mode, this bit must be set to 0. The software must reset the Host Interface prior to entering and after exiting snoop mode.	R/W	0
0x3985C	SNOOP_MODE	1	Payload Discard (PD) This bit is set to 1 by software to indicate snooped packets must have their payloads discarded. When this bit is set to 1, only CIO packet headers are transferred to host buffers. When this bit is set to 0, the entire CIO packet (header+payload) is transferred to host buffers.	R/W	0
0x3985C	SNOOP_MODE	31:2	Reserved Must be set to 0.	R/W	0

4.4.2.18 DMA Time

The format of this register is described in Table 88.

Table 88. DMA Time Register Fields

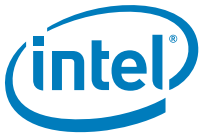
Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x39860	DMA_TIME	31:0	DMA Time TMU time synchronized to DMA clock for isochronous control. Resolution - 250 ns.	RO	0

4.4.2.19 DMA Miscellaneous

The format of this register is described in Table 90.

Table 89. DMA Miscellaneous Register Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x39864	DMA_MISC	0	**DMA Never Idle** When asserted prevents Idle indication to PCIe switch - DMA looked always busy.	R/W	0
0x39864	DMA_MISC	1	**Don’t Discard Control Packet** DMARX doesn't discard PathID 0 packets despite E2E FC disable and descriptors unavailability.	R/W	1
0x39864	DMA_MISC	2	**Auto-Clear Interrupt Status** If asserted to "1" in MSIX mode DMA should clear Interrupt Status Register right after interrupt issuing. Otherwise Interrupt Status Register will be cleared on SW read.	R/W	0
0x39864	DMA_MISC	3	**Disable Credit Sync Packet Sending** If asserted to "1" Credit Sync Packet will never be sent.	R/W	0
0x39864	DMA_MISC	4	**Discard Bad Credit Sync Packet** If asserted to "1" Credit Sync Packet will be discarded in case the sent value is less than current value of CR (credit received) counter.	R/W	1
0x39864	DMA_MISC	5	**dma_fix_tx_wb_hang_disable** Chicken bit - if asserted to “1” disables bug 208397 fix.	R/W	0
0x39864	DMA_MISC	6	**dma_fix_tx_crc_hang_disable** Chicken bit - if asserted to “1” disables bug 208565 fix.	R/W	0
0x39864	DMA_MISC	7	**dma_fix_tx_cio_credit_lost_disable** Chicken bit - if asserted to “1” disables bug 208586 fix.	R/W	0
0x39864	DMA_MISC	8	**dma_fix_tx_pend_corr_disable** Chicken bit - if asserted to “1” disables bug 208588 fix.	RW	0



Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x39864	DMA_MISC	9	**dma_fix_tx_table_busy_disable** Chicken bit - if asserted to "1" disables bug 224211 fix.	RW	0
0x39864	DMA_MISC	10	**dma_fix_read_handler_disable** Chicken bit - if asserted to "1" disables bug 254225 fix	RW	0
0x39864	DMA_MISC	11	**e2e_fc_tx_fix_cb** Chicken bit - if asserted to "1" disables bug 1902168 fix	RW	0
0x39864	DMA_MISC	12	**dma_gather_cb** Chicken bit - if asserted to "1" disables "gather" feature	RW	0
0x39864	DMA_MISC	13	**dma_debug_mode_path0_fix_cb** Chicken bit - if asserted to "1" disables debug mode path0 reliability	RW	1
0x39864	DMA_MISC	14	**dma_debug_mode_pkt_should_be_stopped** This bit configures what should be done with debug packet when DMA is not ready to receive it. "1" : DMA will stop its data path, till debug packet has written into debug registers "0" : DMA will discard debug packet if debug registers are not ready to receive it.	RW	0
0x39864	DMA_MISC	15	**dma_debug_mode_rx_fix_cb** Chicken bit - if asserted to "1" disables fix for RX debug mode. After this fix only "InterDomain" packets considered by DMA as debug packets.	RW	0
0x39864	DMA_MISC	16	E2E flow control packet pended Asserted by HW to "1" if E2E Flow Control packet wait for TX in buffer (debug purposes only).	RO	0
0x39864	DMA_MISC	17	**dma_csr_disable_clear_on_read** Chicken bit - Set this bit to disable interrupt status clear on read capability	RW	0
0x39864	DMA_MISC	18	**stop_cio_when wb_fifo_is_full_cb** Chicken bit - Set this bit to disable stop RX when WB buffer is full	RW	0
0x39864	DMA_MISC	19	**dma_csr_disable_dhost_data_ready_fix** Chicken bit - set this bit to enable fix in DHOST. Default is that this fix disabled	RW	0
0x39864	DMA_MISC	20	**dma_csr_sync_timer_config_bit** Set this bit to configure CS timer to 10s. When this bit unset - CS timer is 1s.	RW	0
0x39864	DMA_MISC	21	**dma_e2e_sync_with_additional_crc_bug_fix** Chicken bit - Set this bit to disable fix for bug 2215376	RW	0
0x39864	DMA_MISC	23:22	Reserved	RW	0

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x39864	DMA_MISC	31:24	**fc_cio_tx_pkt_timeout _cfg** Timeout configuration for DMA FC packet. When expired, internal ACK would be issued for DMA FC packet. This to prevent DMA datapath stuck in case of no CIO credits for FC packet. Part of the fix for 1906956 bug.	RW	0x1

Table 90. ARC and DMA Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x39868	STOP_RX_PER_PATH	0:0	**dont_discard_control_packet** **Equals - dma_csr_misc_reg[1] ^ ee_dont_discard_control_packet**	RO	1
0x39868	STOP_RX_PER_PATH	11:1	**dma_csr_stop_rx_per_path** Set specific bit in this register will cause corresponding DMA RX path to be stopped when no descriptors in both cache and RX table	RW	0x0
0x39868	STOP_RX_PER_PATH	31:12	**Reserved**	RW	0x0
0x3986C	THERMO_SENSOR_LEVEL	6:0	**thermosensor_result**		
0x3986C	THERMO_SENSOR_LEVEL	30:7	**Reserved**		
0x3986C	THERMO_SENSOR_LEVEL	31	**dma_csr_thermo_sensor_level_start** Set this bit to start read thermo sensor level When data ready, HW will unset this bit	RW	0
0x39870	LINK_CREDITS_STATE	7:0	**link_consumed** Visibility for number of consumed link credits by DMA	RO	0
0x39870	LINK_CREDITS_STATE	15:8	**link_limit** Visibility for number of link limit credits advertised to DMA	RO	0
0x39874	PATH_CREDITS_AVAIL	11:0	**cio_fc_credit_avail_per_path** Each bit in this register indicates if there are sufficient number of credits for corresponding path	RO	0
0x39900	INMAILDATA	31:0	**MAILBOX Data from SW** SW -> FW Mailbox Data	R/W	0
0x39904	INMAILCMD	31:0	**MAILBOX Command from SW** SW -> FW Mailbox Command; (SW write accompanied by IRQ#10)	R/W	0
0x39908	OUTMAILDATA	31:0	**MAILBOX Data to SW** FW -> SW Mailbox Data	R/W	0
0x3990C	OUTMAILCMD	31:0	**MAILBOX Command to SW** FW -> SW Mailbox Command; (SW write accompanied by IRQ#9)	R/W	0
0x39910	RSTREQA	31:0	**ARC general purpose register, notin use**	RO	0
0x39914	General Purpose Register	31:0	Reserved	R/W	0
0x39918	EEDATA	31:0	**ARC EE Data** Read data from FLASH	RO	0

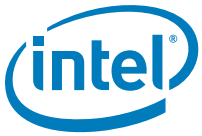


Table 90. ARC and DMA Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x3991C	EECTRL	31:0	**ARC EE Access Control** 23:0 FLASH address for read (in [Bytes]) 31 FLASH read command; FW to set to 1, HW to clear on read completion (accompanied by IRQ#11)	R/W	0
0x39920	EEBASE	31:0	**ARC EE Region base** Byte offset pointing to the beginning of the ARC data area in the FLASH (in [Bytes]) Loaded from FLASH	RO	0
0x39924	EESTRAPS	31:0	**Config bits from FLASH** Loaded from FLASH on initial FLASH load	RW	0
0x39928	WATCHDOG	31:0	**Configurable watchdog timer** 30:0 Watchdog timer – countdown timer @156.25MHz (ARC clk). Written by FW and when gets to 0 causes ARC reset. For example, writing 0xFFFFFFFF will trigger reset after ~13.5sec, unless retriggered. 31 Watchdog Enable – when set, enables watchdog timer	R/W	0
0x3992C	DPIN0CFG	31:0	**DPIN0 parameters** 15:0 SSC PPM shift value. If not 0, this value should be written to respective DPOUT TMU register (DP OUT port, TMU_DP_CS_6). Loaded from FLASH. 30:16 reserved 31 When 0, means this DPIN is connected to GPU Loaded from FLASH(ee_dpi_pwdn_h1)	R/W	0
0x39930	DPIN1CFG	31:0	**DPIN1 parameters** 15:0 SSC PPM shift value. If not 0, this value should be written to respective DPOUT TMU register (DP OUT port, TMU_DP_CS_6). Loaded from FLASH. 30:16 reserved 31 When 0, means this DPIN is connected to GPU Loaded from FLASH(ee_dpi_pwdn_h2)	R/W	0
0x39934	PLUGEVENTCFG	31:0	**plug event configuration** 7:0 Time to keep above GPIO asserted (in [ms]); loaded from FLASH 15:8 Time to wait after HR PCIe reset release till plugevent_gpio toggle (in [ms]); loaded from FLASH 27:16 Reserved 28 GPIO_5__CIO_PLUG_EVENT__HV_OK 29 Polarity (1: active hi, 0: active low) 30 Toggle plugevent_gpio on any CIO [un]plug event 31 Toggle plugevent_gpio on PCIe tunnel creation/teardown	R/W	0

Table 90. ARC and DMA Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x39938	AUX_IENABLE	31:0	**Interrupt Enable** This register masks generation of xirq_n interrupts; 0: disable, 1:enable; Interrupts will not be lost (if there was an interrupt and it was masked out by this register, it will be invoked once re-enabled).	R/W	0x00000007
0x3993C	ARC_LDST_DEBUG	31:0	**LD/ST debug register** 10:0 ldst_addr 11 reserved 12 ldst_ck_en 13 ldst_wren 15:14 reserved 19:16 ldst_mask 31:20 reserved	RO	NA
0x39940	ARC_IFETCH_DEBUG	31:0	**Instruction fetch debug register** 23:0 code_ram_addr 28:24 reserved 29 code_ram_ck_en (active low) 30 code_ram_wr (active low) 31 dccm_code_range (delayed by clk vs. code_ram_addr)	RO	NA
0x39944	ARC_DEBUG	31:0	0 ee_arc_enable (value from FLASH RO) When set, ARC will NOT be halted on reset (arc_start_a) and HopID#0 datapath will be routed to/from ARC subsystem. When cleared, ARC remains in halt (legacy mode) 1 arc_enable invert: XOR'ed with ee_arc_enable and kept on power_good reset. Requires CIO reset after any change! 2 "ctrl_cpu_start": When set, will start the ARC running when it is halted. Thus should be set after using arc_enable_invert, if it was ever halted. 3 "jtag_to_fc":Setting this bit to 1 will switch JTAG to FC (see TSPEC); need to clear in order to be able to set again. 4 ARC Reset 5 car_pcie_dma_rst_n state RO 6 When set, stalls ARC execution pipeline 7 secure_en RO 29:8 Reserved, do not change 30 cio_reset_event_required when set, arc is halted and waits for CIO reset to be performed. When cleared, arc will continue running. 31 CM_ready when set, iCM is fully initialized (at given context) and ready for SW usage.	R/W RO	NA

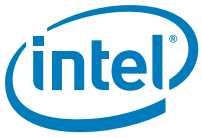


Table 90. ARC and DMA Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x39948	DEBUG_TRAP_RAM_WR_DATA	31:0	**Patch debug register** Patch RAM write data (see DEBUG_TRAP_RAM_CONTROL)	R/W	NA
0x3994C	DEBUG_TRAP_RAM_RD_DATA	31:0	**Patch debug register** Patch RAM read data (see DEBUG_TRAP_RAM_CONTROL)	RO	NA
0x39950	DEBUG_TRAP_RAM_CONTROL	31:0	**Patch debug register** 11:0 debug_trap_ram_addr (in [DW] resolution) 29:12 reserved 30 “debug_trap_ram_access”: set to 1 in order to access Patch RAM thru this debug interface (muxes RAM control from HW to those registers) 31 “debug_trap_ram_write”: writing to 1 performs a write to Patch RAM (need to clear before next write)	R/W	NA
0x39954	DEBUG_TRAP_WR_DATA	31:0	**Patch Trap write data** [16:0]:trap_from address in [DW] [31]:trap_valid	R/W	NA
0x39958	DEBUG_TRAP_RD_DATA	31:0	**Patch debug register** Patch Trap read data (see DEBUG_TRAP_CONTROL)	RO	NA
0x3995C	DEBUG_TRAP_CONTROL	31:0	**Patch debug register** 4:0 “debug_trap_idx”: Trap number (index, 31..0) 30:5 reserved 31 “debug_trap_write”: writing to 1 performs a write to Patch Trap based on index (need to clear before next write)	R/W	NA
0x39960	ee_arc_config	31:0	Straps from FLASH	RO	NA
0x39964	ARC_CACHE_RD_TO	31:0	15:0 Address in RAM to fetch to [Byte] 31:16 reserved	R/W	
0x39968	ARC_CACHE_RD_FROM	31:0	23:0 Address in FLASH to fetch FROM [Byte] 31:24 reserved	R/W	
0x3996C	ARC_CACHE_CONTROL	31:0	15:0 Length of fetch request [Byte] 30:16 reserved 31 Enable bit, on completion the HW unset it and interrupts : cache_req_completed	R/W	
0x39970	ARC_CACHE_MAP1_FROM	31:0	15:0 Absolute address in memory space to map from[DW] 30:24 reserved 31 Enable bit	R/W	
0x39974	ARC_CACHE_MAP_1_TO	31:0	15:0 Address in RAM map to[DW] 31:16 Page length[DW]	R/W	
0x39978	ARC_CACHE_MAP2_FROM	31:0	15:0 Absolute address in memory space to map from[DW] 30:24 reserved 31 Enable bit	R/W	

Table 90. ARC and DMA Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x3997C	ARC_CACHE_MAP_2_TO	31:0	15:0 Address in RAM map to[DW] 31:16 Page length[DW]	R/W	
0x39980	ARC_CACHE_MAP3_FROM	31:0	15:0 Absolute address in memory space to map from[DW] 30:24 reserved 31 Enable bit	R/W	
0x39984	ARC_CACHE_MAP_3_TO	31:0	15:0 Address in RAM map to[DW] 31:16 Page length[DW]	R/W	
0x39988	ARC_CACHE_MAP4_FROM	31:0	15:0 Absolute address in memory space to map from[DW] 30:24 reserved 31 Enable bit	R/W	
0x3998C	ARC_CACHE_MAP_4_TO	31:0	15:0 Address in RAM map to[DW] 31:16 Page length[DW]	R/W	
0x399B0	TAR_CONTROL	31:0	12:0 arc_tar_dw_index 18:13 arc_tar_port 20:19 arc_tar_cs 21 arc_tar_wr1_rd0 22 arc_cio_sw_regs_access 23 arc_pcie_sw_regs_access 29:24 reserved 30 If set, last access completed with timeout 31 arc_tar_valid_toggle: set to 1 by FW, poll for 0 for completion (and then check for timeout)	R/W	
0x399B4	TAR_WR_DATA	31:0	ARC Tar write data	R/W	
0x399B8	TAR_RD_DATA	31:0	Tar ARC read data		
0x399BC	SPWATERMARK	31:0	**Stack Pointer debug** When Stack Pointer (SP/r28) is equal to this value, IRQ6 is fired (if enabled); ignored if uninitialized (=0)	R/W	
0x399C0	reserved	31:0			
0x399C4	INTPENDING	31:0	**Pending Interrupts** When read, returns internal pending interrupts status, including causes that are masked by AUX_IENABLE – Interrupt Enable When written, clears respective internal pending interrupt status.	R/W1C	
0x399C8	CRC_RESULT	31:0	**CRC Result** HW CRC calculation result	R/W	

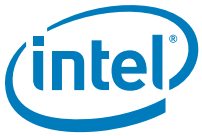


Table 90. ARC and DMA Registers Fields

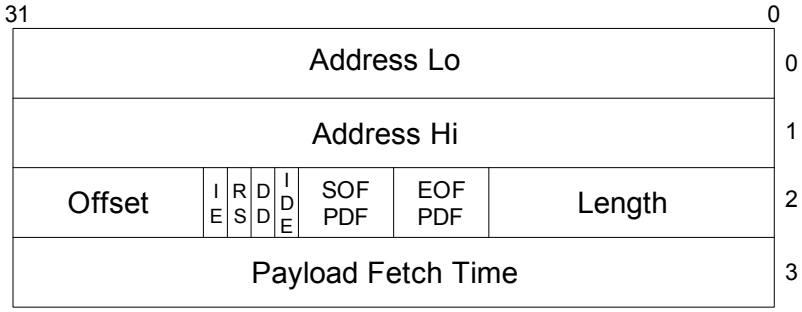
Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x399CC	CRC_CONTROL	31:0	**CRC Control** 0 Calculate on CIO Tx buffer When set to 1 by FW, HW will start calculating CRC, expecting sequential buffer offsets access of the whole packet. CRC can be read from the CRC Result register to be used by FW. HW clears this bit at the end of CRC calculation process. 1 Calculate on CIO Rx buffer 2 Calculate on DMA Tx buffer 3 Calculate on DMA Rx buffer Bits [3:0] are mutually exclusive' don't set more than one of them at a time 31:4 reserved	R/W	
0x399D0	CIOTX	31:0	**CIO Tx Control** 7:0 CIO Packet length in [DW]'s, including CIO Header 31 CIO Tx packet ready; FW to set to 1, HW to clear on packet transmission (accompanied by IRQ#15)	R/W	
0x399D4	CIORX	31:0	**CIO Rx Control** 31 FW ready to receive CIO Rx packet; FW to set to 1, HW to clear on packet reception (accompanied by IRQ#14)	R/W	
0x399D8	DMATX	31:0	**DMATX - DMA Tx Control** 7:0 DMA Packet length in [DW]'s, including CIO Header 31 DMA Tx packet ready; FW to set to 1, HW to clear on packet transmission (accompanied by IRQ#13)	R/W	
0x399DC	DMARX	31:0	**DMA Rx Control** 31 FW ready to receive DMA Rx packet; FW to set to 1, HW to clear on packet reception (accompanied by IRQ#12)	R/W	

4.4.3 Data Structures

4.4.3.1 Transmit

4.4.3.1.1 Transmit Buffer Descriptor

Figure 46. Transmit Buffer Descriptor



The transmit buffer descriptor shown in Figure 46 is a data structure that resides in host memory and describes a host buffer containing a frame that must be transmitted over the CIO link.

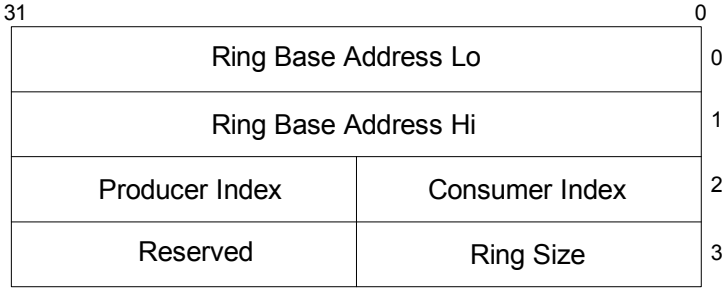
The transmit buffer descriptor defines the following fields:

- Address Lo [DW0 31:0]: Lower 32 bits of the physical address of the buffer in host memory. The buffer address must be doubleword aligned. Therefore, the least significant 2-bits of the Address Lo field must be 0.
- Address Hi [DW1 31:0]: Upper 32 bits of the physical address of the buffer in host memory.
- Length [DW2 11:0]: Length of the frame. It is binary encoded with a value that is equal to the number of bytes in the frame. A length of 0 indicates a frame of 4096 bytes.
- EOF Protocol Defined Field (EOF PDF) [DW2 15:12]: The value that must be inserted into the PDF field of the CIO packet header for the last packet of the frame. If the frame fits entirely within a single CIO packet, this field is inserted into the PDF field of the CIO packet header. If desired to use multiple buffer descriptors in a frame ("gather" feature), set this field to '0' in each buffer descriptor which is not the last one.
- SOF Protocol Defined Field (SOF PDF) [DW2 19:16]: The value that must be inserted into the PDF field of the CIO packet header for the first packet of the frame. If the frame fits entirely within a single CIO packet, this field is ignored. If desired to use multiple buffer descriptors in a frame ("gather" feature), set this field to '0' in each buffer descriptor which is not the first one.
- Isochronous DMA Enable (IDE) [DW2 Bit 20]: This bit must be set to 1 if the DMA of the buffer payload from host memory must be performed no earlier than the next eligible time. The next eligible time is the Payload Fetch Time if the Isochronous Transmit Enable (ITE) bit is set to 0 in the corresponding transmit table entry. If the ITE bit is set to 1, the next eligible time is determined based on the Start Time and Interval fields in the corresponding transmit table entry. If this bit is set to 0, the segmentation engine may DMA the payload from host memory as soon as it fetches the buffer descriptor.
- Descriptor Done (DD) [DW2 Bit 21]: This bit is set to 1 by the host interface after the transmit buffer descriptor is completely processed. This bit is only valid if the Request Status bit was set.
- Request Status (RS) [DW2 Bit 22]: This bit must be set to 1 if the host interface must report the transmit status information for this buffer descriptor. The status is reported in the Descriptor Done (DD) bit.

- Interrupt Enable (IE) [DW2 Bit 23]: This bit must be set to 1 if an interrupt is to be generated when the buffer descriptor is completely processed by the host interface.
- Offset [DW2 31:24]: The location of the first byte of the CIO packet or Frame from the buffer base address defined by the Address Hi/Lo fields.
- Payload Fetch Time [DW3 31:0]: When the IDE bit is set to 1, this field specifies the absolute time at which the payload is eligible for DMA from host memory. This time has a resolution of 250ns.

4.4.3.1.2 Transmit Ring Descriptor

Figure 47. Transmit Ring Descriptor



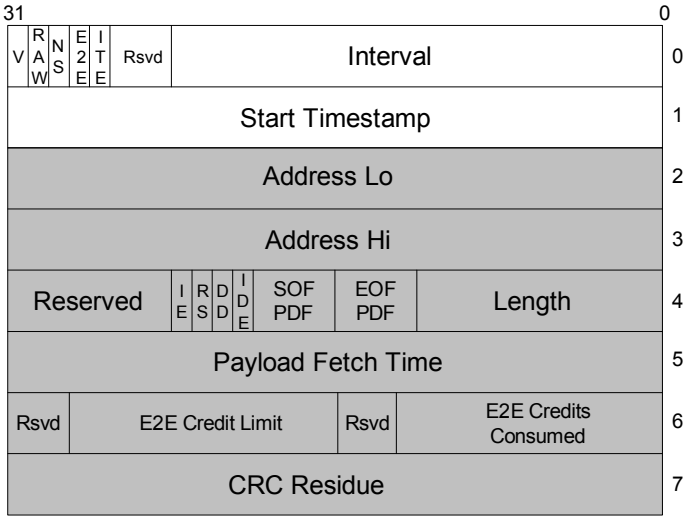
The transmit ring descriptor, shown in Figure 47 is a data structure that resides in the host interface internal registers and defines the circular array used to hold transmit buffer descriptors. The host interface provides one transmit ring per-path. The transmit ring descriptor defines the following fields:

- Ring Base Address Lo [DW0 31:0]: Lower 32 bits of the physical address of the ring in host memory. The ring base address must be aligned to 16 bytes. Therefore, the least significant 4-bits of the Ring Base Address Lo field must be 0. Writing to this register resets the Producer and Consumer indices to 0.
- Ring Base Address Hi [DW1 31:0]: Upper 32 bits of the physical address of the ring in host memory. Writing to this register resets the Producer and Consumer indices to 0.
- Producer Index [DW2 31:16]: Index of the next free location in the circular array into which a transmit buffer descriptor may be written. This index is updated by the host software.
- Consumer Index [DW2 15:0]: Index into the circular array that points to the next transmit buffer descriptor that must be processed by the segmentation engine. This index is updated by the host interface. Software writes to the consumer index are ignored by the host interface.
- Reserved [DW3 31:16]: Reserved field that must be set to 0.
- Ring Size [DW3 15: 0]: Size of the ring in a number of transmit buffer descriptors. Writing to this register resets the Producer and Consumer indices to 0.

4.4.3.1.3 Transmit Table

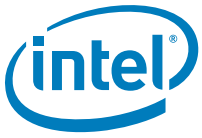
The transmit table is a data structure that resides in the host interface internal memory and is used by the segmentation engine to segment a Frame into CIO packets. The transmit table contains one entry per path.

Figure 48. Transmit Table entry



The format of the transmit table entry is shown in Figure 48. The shaded area represents a working copy of the current transmit buffer descriptor maintained by the segmentation engine during transmit. The non-shaded area contains configuration parameters that must be programmed by software. The description of various fields is given below:

- Interval [DW0 23:0]: If the Isochronous Transmit Enable (ITE) bit is set to 1, this field specifies the interval between the eligibility times for payload DMA. The resolution of this time is 256ns.
- Reserved [DW0 26:24]: Must be set to 0.
- Isochronous Transmit Enable (ITE) [DW0 Bit 27]: When set to 1, this bit specifies that the payload eligibility time for isochronous DMA must be calculated using the Start Timestamp and Interval fields. When set to 0, the payload eligibility time is given by the Payload Fetch Time in the transmit buffer descriptor. This bit is only valid when the Isochronous DMA Enable (IDE) bit is set to 1 in the transmit buffer descriptor.
- End-to-End Flow Control Enable (E2E) [DW0 Bit 28]: When set to 1, end-to-end flow control is enabled for the path. When set to 0, end-to-end flow control is disabled.
- No-snoop flag (NS) [DW0 Bit 29]: This flag is set to 1 by software if the PCIe no-snoop attribute must be set for all host-memory accesses resulting from the transmission of a CIO packet on this transmit table entry. This applies to all memory reads and writes to the transmit buffer descriptors and memory reads for the packet payload.
- Raw flag [DW0 Bit 30]: This flag is set to 0 by software if frame mode is used for the path, or to 1 if raw mode is used. This field is initialized by system software.
- Valid flag [DW0 Bit 31]: This flag is set to 1 if the transmit table entry is enabled. If set to 0, the segmentation engine ignores the transmit table entry.
- Start Timestamp [DW1 31:0]: If the Isochronous Transmit Enable (ITE) bit is set to 1, this field specifies the absolute time at which the path becomes eligible for isochronous DMA for the first time. The resolution of this time is 256ns.
- Address Lo [DW2 31:0]: Lower 32 bits of the physical address pointing to a location within the host buffer from which the next CIO packet must be formed for transmission.
- Address Hi [DW3 31:0]: Upper 32 bits of the physical address pointing to a location within the host buffer from which the next CIO packet must be formed for transmission. The address fields are set to the sum of the address field in the transmit buffer descriptor and the offset field when a new buffer descriptor is removed from the transmit ring. The segmentation engine updates the address fields after every CIO packet transmission.



- Length [DW4 11:0]: Length of the host buffer payload in bytes that is yet to be transmitted. This field is initialized using the length field in the transmit buffer descriptor and is updated by the segmentation engine after every CIO packet transmission.
- EOF Protocol Defined Field (EOF PDF) [DW4 15:12]: The value that must be inserted into the PDF field of the CIO packet header for the last packet of the frame. If the frame fits entirely within a single CIO packet, this field is inserted into the PDF field of the CIO packet header. This field is copied from the transmit buffer descriptor of the frame being transmitted.
- SOF Protocol Defined Field (SOF PDF) [DW4 19:16]: The value that must be inserted into the PDF field of the CIO packet header for the first packet of the frame. If the frame fits entirely within a single CIO packet, this field is ignored. This field is copied from the transmit buffer descriptor of the frame being transmitted.
- Isochronous DMA Enable (IDE) [DW4 Bit 20]: This bit must be set to 1 if the DMA of the buffer payload from host memory must be performed no earlier than the next eligible time. The next eligible time is the Payload Fetch Time if the Isochronous Transmit Enable (ITE) bit is set to 0 in the corresponding transmit table entry. If the ITE bit is set to 1, the next eligible time is determined based on the Start Time and Interval fields in the corresponding transmit table entry. This field is copied from the transmit buffer descriptor of the frame being transmitted.
- Descriptor Done (DD) [DW4 Bit 21]: This bit is set to 1 by the host interface after the transmit buffer descriptor is completely processed. This bit is only valid if the Request Status bit was set. This bit is copied from the transmit buffer descriptor of the frame being transmitted.
- Request Status (RS) [DW4 Bit 22]: This bit must be set to 1 if the host interface must report the transmit status information for this buffer descriptor. The status is reported in the Descriptor Done (DD) bit. This bit is copied from the transmit buffer descriptor of the frame being transmitted.
- Interrupt Enable (IE) [DW4 Bit 23]: This bit must be set to 1 if an interrupt is to be generated when the buffer descriptor is completely processed by the host interface. This bit is copied from the transmit buffer descriptor of the frame being transmitted.
- Reserved [DW4 31:24]: Must be set to 0.
- Payload Fetch Time [DW5 31:0]: When the IDE bit is set to 1, this field specifies the absolute time at which the payload is eligible for DMA from host memory. This time has a resolution of 250ns. This bit is copied from the transmit buffer descriptor of the frame being transmitted.
- E2E Credits Consumed [DW6 12:0]: This field specifies the value of the Credits Consumed register for the path's end-to-end credit based flow control. This field is updated by the segmentation engine when a packet is transmitted from this transmit table entry.
- Reserved [DW6 15:13]: Must be set to 0.
- E2E Credit Limit [DW6 28:16]: This field specifies the value of the Credit Limit register for the path's end-to-end credit based flow control. This field is updated by the reassembly engine when it receives an end-to-end flow control update for this path.
- Reserved [DW6 31:29]: Must be set to 0.
- CRC Residue [DW7 31:0]: Running CRC residue computed over the bytes of the host buffer that have been transmitted. This field is only valid in the frame mode. This field is initialized by the segmentation engine when a new transmit buffer descriptor is removed from the transmit ring and is updated after every CIO packet transmission on this HopID. The final CRC value computed after the last CIO packet is formed, is appended to the payload. If there is no space in the CIO packet payload to append the CRC, a new CIO packet is generated that contains the CRC value.

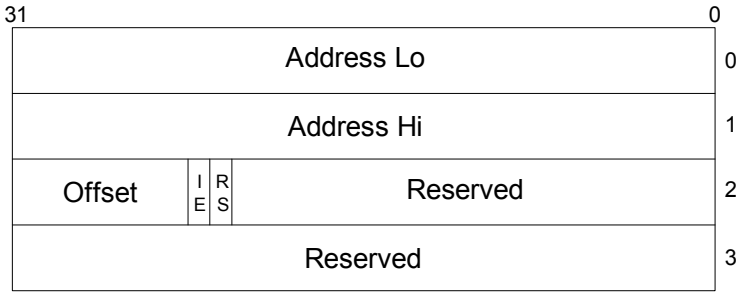
4.4.3.2 Receive

The following data structures are used by the host interface for packet reception and frame reassembly.

4.4.3.2.1 Receive Buffer Descriptor

The receive buffer descriptor is a data structure that resides in host memory and describes a host buffer containing a received frame or packet. The Software creates receive buffer descriptors to point to free receive buffers in host memory, and enqueues it onto the receive ring associated with a HopID. The format of the free receive buffer descriptor is shown in Figure 49.

Figure 49. Receive Buffer Descriptor before Use

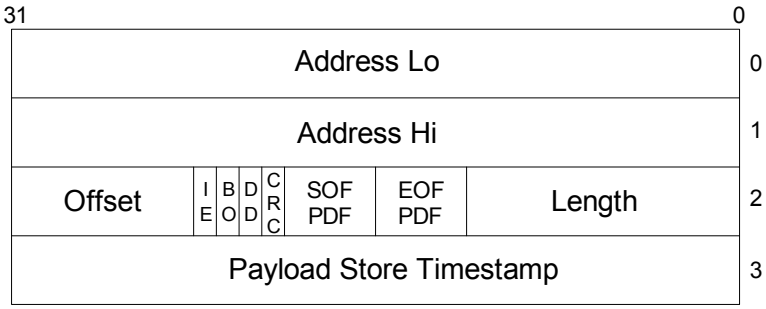


The fields of the receive buffer descriptor are described below:

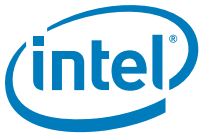
- Address Lo [DW0 31:0]: Lower 32 bits of the physical address of the buffer in host memory. The buffer address must be doubleword aligned. Therefore, the least significant 2-bits of the Address Lo field must be 0.
- Address Hi [DW1 31:0]: Upper 32 bits of the physical address of the buffer in host memory.
- Reserved [DW2 21:0]: Reserved field. Must be set to 0.
- Request Status (RS) [DW2 Bit 22]: This bit must be set to 1 if the host interface must report the receive status information for this buffer descriptor. The status is reported in the Descriptor Done (DD) bit.
- Interrupt Enable (IE) [DW2 Bit 23]: This bit must be set to 1 if an interrupt is to be generated when the buffer descriptor is completely processed by the host interface.
- Offset [DW2 31:24]: The location of the first byte of the CIO packet or Frame from the beginning of the buffer.
- Reserved [DW3 31:0]: Reserved field. Must be set to 0.

When a frame has been fully received and reassembled by the host interface, the receive buffer descriptor is updated. The updated receive buffer descriptor has the format shown in Figure 50.

Figure 50. Receive Buffer Descriptor after Use



The fields of the receive buffer descriptor are described below:

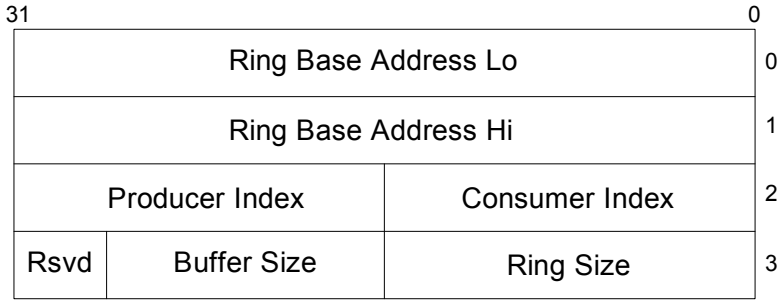


- Address Lo [DW0 31:0]: Lower 32 bits of the physical address of the buffer in host memory. The buffer address must be doubleword aligned. Therefore, the least significant 2-bits of the Address Lo field must be 0.
- Address Hi [DW1 31:0]: Upper 32 bits of the physical address of the buffer in host memory.
- Length [DW2 11:0]: Length of the received packet or frame host, in bytes.
- EOF Protocol Defined Field (EOF PDF) [DW2 15:12]: The value of the PDF field from the last packet of the frame. If the frame fits entirely within a single CIO packet, this field contains the PDF field of the single CIO packet.
- SOF Protocol Defined Field (SOF PDF) [DW2 19:16]: The value of the PDF field from the first packet of the frame. If the frame fits entirely within a single CIO packet, this field is set to 0.
- CRC Error [DW2 Bit 20]: In Frame mode, this bit is set to 1 if the CRC check failed for the reassembled frame, and set to 0 if the CRC check passed. In Raw mode, this bit is always set to 0. The configuration of the Frame mode or Raw mode for a path is specified in the receive table.
- Descriptor Done (DD) [DW2 Bit 21]: This bit is set to 1 by the host interface after the transmit buffer descriptor is completely processed. This bit is only valid if the Request Status bit was set.
- Buffer Overrun Error (BO) [DW2 Bit 22]: This bit must be set to 1 if the received frame exceeded the receive buffer size.
- Interrupt Enable (IE) [DW2 Bit 23]: This bit must be set to 1 if an interrupt is to be generated when the buffer descriptor is completely processed by the host interface.
- Offset [DW2 31:24]: The location of the first byte of the CIO packet or Frame from the beginning of the buffer.

Payload Store Timestamp [DW3 31:0]: This field specifies the absolute time when the payload of the first CIO packet of a frame was transferred to host memory by the reassembly engine. The resolution of this timestamp is 250ns.

4.4.3.2.2 Receive Ring Descriptor

Figure 51. Receive Ring Descriptor



The receive ring descriptor, shown in Figure 51 is a data structure that resides in host interface registers and defines the circular array used to hold the receive buffer descriptors. The receive ring descriptor defines the following fields:

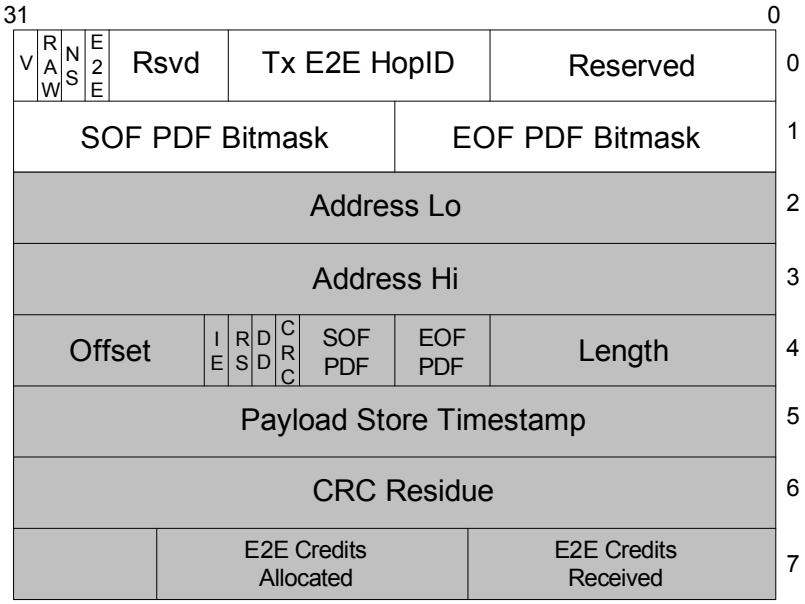
- Ring Base Address Lo [DW0 31:0]: Lower 32 bits of the physical address of the ring in host memory. The ring base address must be aligned to 16 bytes. Therefore, the least significant 4-bits of the Ring Base Address Lo field must be 0. Writing to this register resets the Producer and Consumer indices to 0.
- Ring Base Address Hi [DW1 31:0]: Upper 32 bits of the physical address of the ring in host memory. Writing to this register resets the Producer and Consumer indices to 0.

- Producer Index [DW2 31:16]: Index of the next free location in the circular array into which a receive buffer descriptor may be written. This index is updated by the host interface. Software writes to the producer index are ignored by the host interface.
- Consumer Index [DW2 15:0]: Index into the circular array that points to the next receive buffer descriptor that must be processed by the system software. This index is updated by system software.
- Reserved [DW3 31:28]: Reserved field that must be set to 0.
- Buffer Size [DW3 27:16]: Size of the host buffers in bytes. The value 0 is assumed to indicate 4096. Therefore, the maximum buffer size is 4096 bytes.

Ring Size [DW3 15: 0]: Size of the ring in number of receive buffer descriptors. Writing to this register resets the Producer and Consumer indices to 0.

4.4.3.2.3 Receive Table

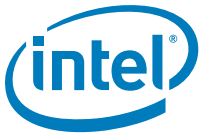
Figure 52. Receive Table Entry



The receive table is a data structure that resides in host interface internal memory and is used by the reassembly engine to assemble a frame from received CIO packets. The receive table contains one entry per path.

The format of the receive table entry is shown in Figure 52. The shaded area represents a working copy of the current receive buffer descriptor maintained by the reassembly engine during receive. The non-shaded area contains configuration parameters that must be programmed by software. The description of various fields is given below:

- Reserved [DW0 11:0]: Must be set to 0.
- Tx E2E HopID [DW0 22:12]: This field specifies the HopID of the transmit path that must receive flow control updates received on the HopID associated with the receive table entry. This field is only valid if the E2E bit is set to 1.
- Reserved [DW0 27:23]: Must be set to 0.
- End-to-End Flow Control Enable (E2E) [DW0 Bit 28]: When set to 1, end-to-end flow control is enabled for the path. When set to 0, end-to-end flow control is disabled.



- No-snoop flag (NS) [DW0 Bit 29]: This flag is set to 1 by software if the PCIe no-snoop attribute must be set for all host-memory accesses resulting from the reception of a CIO packet on this receive table entry. This applies to all memory reads and writes to the receive buffer descriptors, and memory writes for the packet payload.
- Raw flag [DW0 Bit 30]: This flag is set to 0 by software if frame mode is used for the path, or 1 if raw mode is used. This field is initialized by system software.
- Valid flag [DW0 Bit 31]: This flag is set to 1 if the receive table entry is enabled. If set to 0, the reassembly engine ignores the receive table entry.
- EOF PDF Bitmask [DW1 15:0]: This field is initialized by system software. It specifies all the PDF field values that may be interpreted as an End of Frame (EOF) marker. If the bit at the position given by the PDF field value in a received CIO packet is set, then the end of the current frame is indicated, and the reassembly engine puts the reassembled frame onto the receive ring. Bit position 0 (PDF value of 0) may not be set to 1.
- SOF PDF Bitmask [DW1 31:16]: This field is initialized by system software. It specifies all the PDF field values that may be interpreted as a Start of Frame (SOF) marker. If the bit at the position given by the PDF field value in a received CIO packet is set, then the start of a new frame is indicated fetches a new buffer descriptor from the freelist. Bit position 0 (PDF value of 0) may not be set to 1.
- Address Lo [DW2 31:0]: Lower 32 bits of the physical address of the buffer in host memory.
- Address Hi [DW3 31:0]: Upper 32 bits of the physical address of the buffer in host memory. The address fields point to the starting address of the host buffer, and are initialized using the values contained in the free buffer descriptor used to reassemble the frame. They are not modified during frame reassembly.
- Length [DW4 11:0]: Length of the received packet or frame host in bytes. This field is initialized to 0 when a new receive buffer descriptor is fetched from the receive ring. It is incremented by the length of the received CIO packet. The value of (offset + length) is added to the address fields to obtain the starting address for the DMA transfer when the CIO packet payload is transferred to the receive buffer. At the end of the reassembly process, this field contains the total length of the received frame.
- EOF PDF [DW4 15:12]: This field contains the PDF values of the last packet of the frame. If the received frame fits entirely within a single CIO packet, this field contains the PDF value from that packet.
- SOF PDF [DW4 19:16]: This field contains the PDF value of the first packet of the frame. This field is set to 0 if the frame fits entirely within one CIO packet.
- CRC Error [DW4 Bit 20]: In Frame mode, this bit is set to 1 if the CRC check failed for the reassembled frame, and is set to 0 if the CRC check passed. In Raw mode, this bit is always set to 0.
- Descriptor Done (DD) [DW4 Bit 21]: This bit is set to 1 by the host interface after the receive buffer descriptor is completely processed. This bit is only valid if the Request Status bit was set.
- Request Status (RS) [DW4 Bit 22]: This bit must be set to 1 if the host interface must report the receive status information for this buffer descriptor. The status is reported in the Descriptor Done (DD) bit.
- Interrupt Enable (IE) [DW4 Bit 23]: This bit must be set to 1 if an interrupt is to be generated when the receive buffer descriptor is completely processed by the host interface.
- Offset [DW4 31:24]: The location of the first byte of the CIO packet or Frame from the beginning of the buffer. This field is initialized from the value contained in the receive buffer descriptor and is unmodified by the reassembly engine.
- Payload Store Timestamp [DW5 31:0]: This field specifies the absolute time when the payload of the first CIO packet of a frame was transferred to host memory by the reassembly engine. The resolution of this timestamp is 250ns.
- CRC Residue [DW6 31:0]: The running CRC residue computed over the payload bytes of received CIO packets. This field is initialized by the reassembly engine when a new receive buffer

descriptor is fetched, and is updated after every CIO packet reception on the associated HopID. The final CRC value computed after the last CIO packet is received, is compared to the CRC value appended to the end of the frame payload by the transmitter. If the CRC values do not match, the CRC error flag is set in the receive buffer descriptor.

- E2E Credits Received [DW7 12:0]: This field specifies the value of the Credits Received register for the path's end-to-end credit based flow control. This field is updated by the reassembly engine when the producer index of the receive ring associated with this receive table entry is incremented.
- E2E Credits Allocated [DW7 25:13]: This field specifies the value of the Credits Allocated register for the path's end-to-end credit based flow control. This field is updated by the reassembly engine when the consumer index of the receive ring associated with this receive table entry is incremented.

Reserved [DW7 31:26]: Must be set to 0.

4.5 PCI Express Configuration Space

This chapter contains register tables of PCIE Configuration Space of PCIE Bridges/Endpoints in Thunderbolt (PCIE Spec registers and custom registers).

See PCI Express Base 3.0 specification for additional information about PCIE Spec registers.

Thunderbolt contains PCIE Switch: Upstream and five Downstream Ports. The PCIe switch structure is shown in Figure 53 .

In addition it contains two PCIE Embeded Endpoints for DMA and XHC.

PCIE Switch connects to:

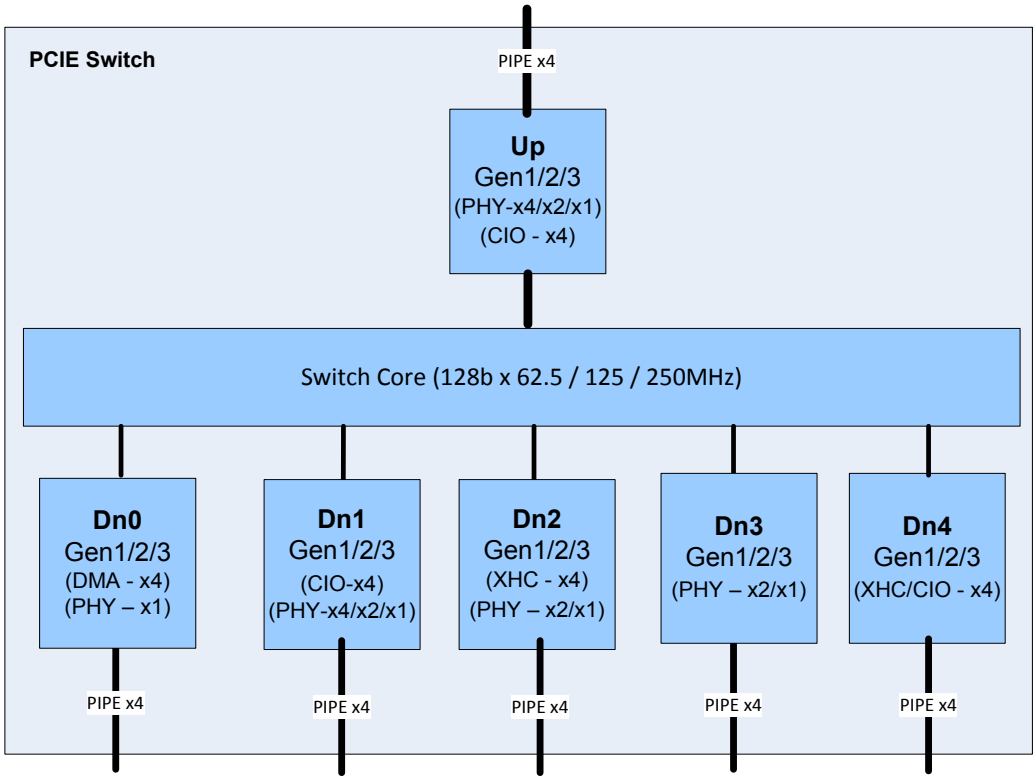
"DMA through Embedded Endpoint.

"XHC through Embedded Endpoint.

"CIO Switch Port through Adapter

"PCIE PHY

Figure 53. PCIe Switch Structure



In each PCIE Port there is PCIE Configuration Space that contains Basic and Extended Capabilities in two seperatelinked linked lists.

List of Basic Capabilities

Upstream / Downstream

"Address 0x34 Capability Pointer with value 0x80 (This is still in the Header)

"Address 0x80 PM Capability with next capability pointer - 0x88

"Address 0x88 MSI Capability with next capability pointer - 0xAC

"Address 0xAC SubSysID Capability with next capability pointer - 0xC0

"Address 0xC0 PCIE Capability with next capability pointer - 0x00 (last))

Downstream

"Address 0x34 Capability Pointer with value 0x80 (This is still in the Header)

"Address 0x80 PM Capability with next capability pointer - 0x88

"Address 0x88 MSI Capability with next capability pointer - 0xAC

"Address 0xAC SubSysID Capability with next capability pointer - 0xC0

"Address 0xC0 PCIE Capability with next capability pointer - 0x00 (last))

DMA EMEP

"Address 0x34 Capability Pointer with value 0x80 (This is still in the Header)

"Address 0x80 PM Capability with next capability pointer - 0x88

"Address 0x88 MSI Capability with next capability pointer - 0xC0

"Address 0xC0 PCIE Capability with next capability pointer - 0xA0

"Address 0xA0 MSI-X Capability with next capability pointer - 0x00 (last)

XHC EMEP

"Address 0x34 Capability Pointer with value 0x80 (This is still in the Header)

"Address 0x80 PM Capability with next capability pointer - 0x88

"Address 0x88 MSI Capability with next capability pointer - 0xC0

"Address 0xC0 PCIE Capability with next capability pointer - 0x00 (last)

List of Extended Capabilities

Upstream

"Address 0x100 - Device Serial Number Capability with next pointer - 0x200

"Address 0x200 - Advanced Error Reporting Capability with next pointer - 0x300

"Address 0x300 - Virtual Channel Capability with next pointer - 0x400

"Address 0x400 - Power Budgeting Capability with next pointer - 0x500

"Address 0x500 - Vendor Specific Enhanced Capability with next pointer - 0x600

"Address 0x600 - Latency Tolerance Reporting Capability with next pointer - 0x700

"Address 0x700 - Secondary PCIE Extended Capability with next pointer - 0x0 (last)

Downstream

"Address 0x100 - Device Serial Number Capability with next pointer - 0x200

"Address 0x200 - Advanced Error Reporting Capability with next pointer - 0x300

"Address 0x300 - Virtual Channel Capability with next pointer - 0x400

"Address 0x400 - Power Budgeting Capability with next pointer - 0x500

"Address 0x500 - Vendor Specific Enhanced Capability with next pointer - 0x700

"Address 0x700 - Secondary PCIE Extended Capability with next pointer - 0x0 (last)

DMA EMEP

"Address 0x100 - Device Serial Number Capability with next pointer - 0x200

"Address 0x200 - Advanced Error Reporting Capability with next pointer - 0x300

"Address 0x300 - Virtual Channel Capability with next pointer - 0x400

"Address 0x400 - Power Budgeting Capability with next pointer - 0x500

"Address 0x500 - Vendor Specific Enhanced Capability with next pointer - 0x600

"Address 0x600 - Latency Tolerance Reporting Capability with next pointer - 0x0

XHC EMEP

"Address 0x100 - Device Serial Number Capability with next pointer - 0x200

"Address 0x200 - Advanced Error Reporting Capability with next pointer - 0x300

"Address 0x300 - Virtual Channel Capability with next pointer - 0x400

"Address 0x400 - Power Budgeting Capability with next pointer - 0x500

"Address 0x500 - Vendor Specific Enhanced Capability with next pointer - 0x600

"Address 0x600 - Latency Tolerance Reporting Capability with next pointer - 0x700

"Address 0x700 - Secondary PCIE Extended Capability with next pointer - 0x0 (last)

4.5.1 Type 0 Configuration Space Header

Thunderbolt contains two PCIE Embedded Endpoints: for DMA and XHC. Each Endpoint has Type 0 Configuration Space Header.

Figure 54 details allocation for register fields of Type 0 Configuration Space header for PCI Express device Functions. Those fields described in Table 91.

Figure 54. Type 0 Configuration Space Header

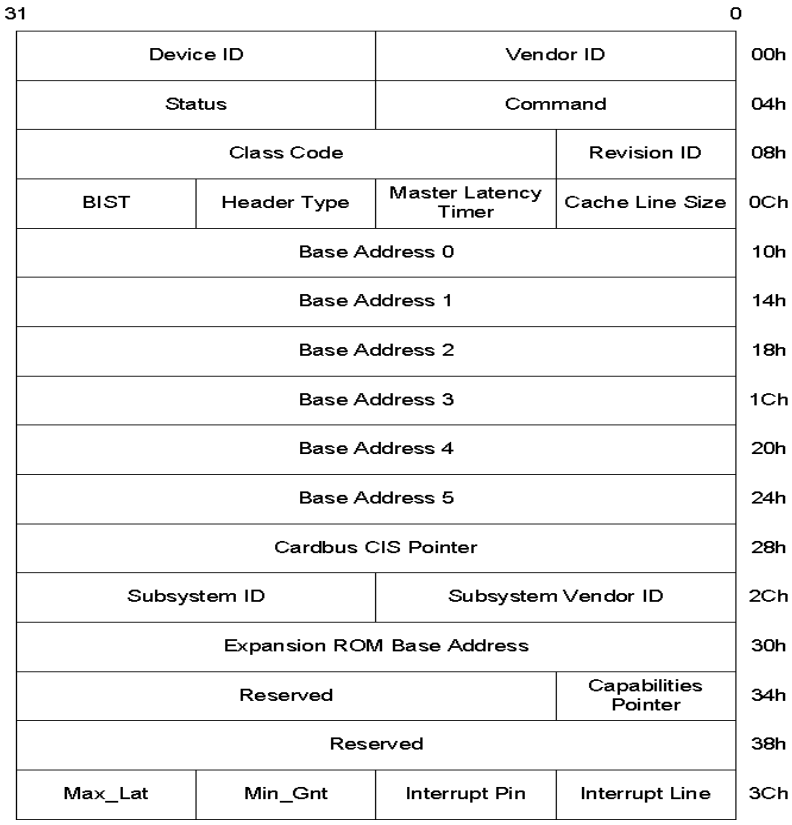


Table 91. Type 0 Configuration Space Header Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x00	PCIE_TYPE0_0	15:0	Vendor ID	RO	0x8086
0x00	PCIE_TYPE0_0	31:16	Device ID	RO	DMA EMEP - 0x1577 XHC EMEP - 0x15B6
0x04	PCIE_TYPE0_1	15:0	Command	See PCIe Spec	0
0x04	PCIE_TYPE0_1	31:16	Status	See PCIe Spec	0x0010
0x08	PCIE_TYPE0_2	7:0	Revision ID	RO	0
0x08	PCIE_TYPE0_2	31:8	Class Code	RO	DMA EMEP - 0x088000 XHC EMEP - 0x0C0330
0x0C	PCIE_TYPE0_3	7:0	Cache Line Size	R/W	0
0x0C	PCIE_TYPE0_3	15:8	Master Latency Timer	RO	0
0x0C	PCIE_TYPE0_3	23:16	Header Type	RO	0
0x0C	PCIE_TYPE0_3	31:24	BIST	See PCIe Spec	0
0x10	PCIE_TYPE0_4	31:0	Base Address 0	See PCIe Spec	See BAR0 in Table 92
0x14	PCIE_TYPE0_5	31:0	Base Address 1	See PCIe Spec	See BAR1 in Table 92
0x18	PCIE_TYPE0_6	31:0	Base Address 2	See PCIe Spec	See BAR2 in Table 92
0x1C	PCIE_TYPE0_7	31:0	Base Address 3	See PCIe Spec	See BAR3 in Table 92
0x20	PCIE_TYPE0_8	31:0	Base Address 4	See PCIe Spec	See BAR4 in Table 92

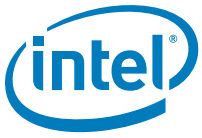


Table 91. Type 0 Configuration Space Header Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x24	PCIE_TYPE0_9	31:0	Base Address 5	See PCIe Spec	See BAR5 in Table 92
0x28	PCIE_TYPE0_10	31:0	Cardbus CIS Pointer	RO	0
0x2C	PCIE_TYPE0_11	15:0	Subsystem Vendor ID	RO	0x2222
0x2C	PCIE_TYPE0_11	31:16	Subsystem ID	RO	0x1111
0x30	PCIE_TYPE0_12	31:0	Expansion ROM Base Address	See PCIe Spec	0
0x34	PCIE_TYPE0_13	7:0	Capabilities Pointer	RO	0x80
0x34	PCIE_TYPE0_13	31:8	Reserved	RO	0
0x38	PCIE_TYPE0_14	31:0	Reserved	RO	0
0x3C	PCIE_TYPE0_15	7:0	Interrupt Line	R/W	0xFF
0x3C	PCIE_TYPE0_15	15:8	Interrupt Pin	RO	0x01
0x3C	PCIE_TYPE0_15	23:16	Min_Gnt	RO	0
0x3C	PCIE_TYPE0_15	31:24	Max_Lat	RO	0

The Subsystem Vendor ID and Subsystem ID fields can be loaded from FLASH during boot to values other than default.

There are two BARs in DMA EMEP with option to configure 32 or 64 bit from EEPROM

"Memory space of 256K that can be 32 or 64 bit BAR

"MSIX of 4K that can be 32 or 64 bit

Table 92. DMA EMEP BAR Values (32bit)

BAR	Value
BAR0 (MEM)	32'b1111_1111_1111_1100_0000_0000_0000_0000
BAR1 (MSIX)	32'b1111_1111_1111_1111_1111_0000_0000_0000
BAR2	32'b0
BAR3	32'b0
BAR4	32'b0
BAR5	32'b0

Table 93. DMA EMEP BAR Values (64bit)

BAR	Value
BAR0 (MEM)	32'b1111_1111_1111_1100_0000_0000_0000_0100
BAR1 (MEM)	32'hFFFFFFFF
BAR2 (MSIX)	32'b1111_1111_1111_1111_1111_0000_0000_0100
BAR3 (MSIX)	32'hFFFFFFFF
BAR4	32'b0
BAR5	32'b0

There is a Memory BAR of 64K in XHC EMEP with option to configure 32 or 64 bit from EEPROM.

Table 94. XHC EMEP BAR Values (32bit)

BAR	Value
BAR0 (MEM)	32'b1111_1111_1111_1111_0000_0000_0000_0000
BAR1	32'b0
BAR2	32'b0
BAR3	32'b0
BAR4	32'b0
BAR5	32'b0

Table 95. XHC EMEP BAR Values (32bit)

BAR	Value
BAR0 (MEM)	32'b1111_1111_1111_1111_0000_0000_0000_0100
BAR1 (MEM)	32'hFFFFFFFF
BAR2 (MSIX)	32'b0
BAR3 (MSIX)	32'b0
BAR4	32'b0
BAR5	32'b0

4.5.2 Type 1 Configuration Space Header

Figure 55 details allocation for register fields of Type 1 Configuration Space header for Switch and Root Complex virtual PCI Bridges (US and DS ports). Those fields are described in Table 96.

Figure 55. Type 1 Configuration Space Header

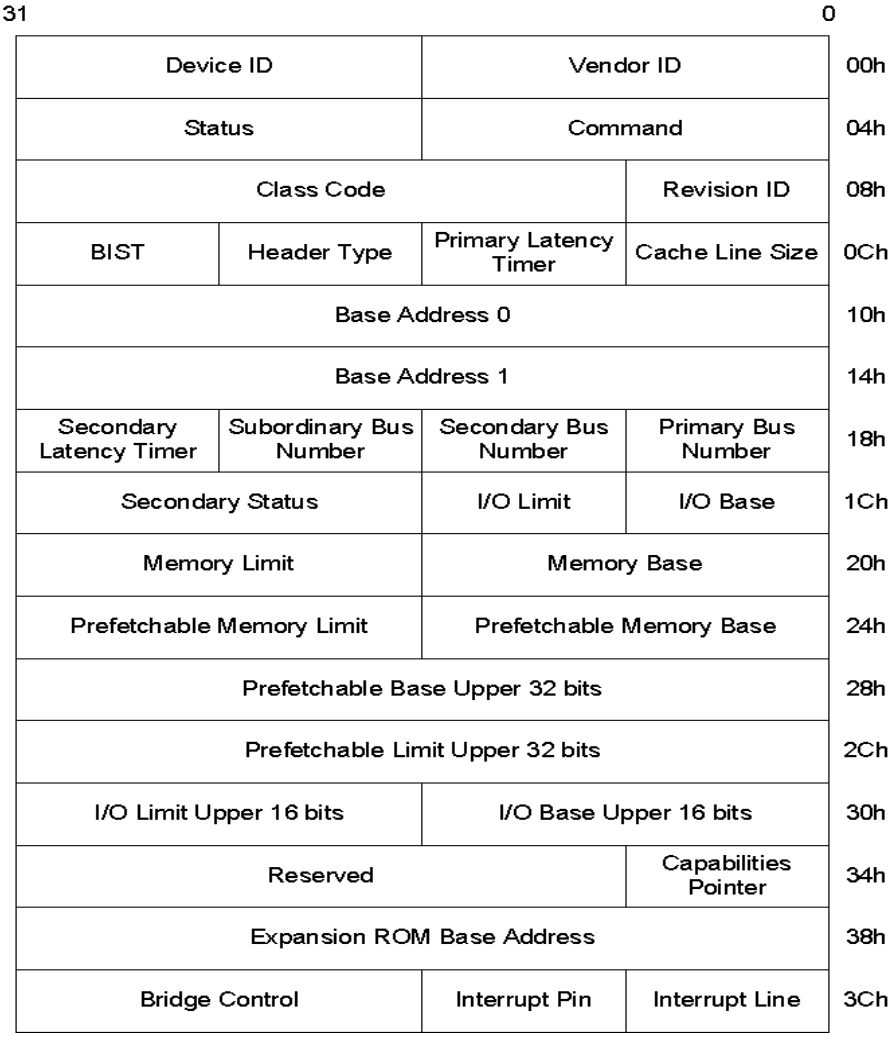


Table 96. Type 1 Configuration Space Header Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x00	PCIE_TYPE0_0	15:0	Vendor ID	RO	0x8086
0x00	PCIE_TYPE0_0	31:16	Device ID	RO	0x1578
0x04	PCIE_TYPE0_1	15:0	Command	See PCIe Spec	0
0x04	PCIE_TYPE0_1	31:16	Status	See PCIe Spec	0x0010
0x08	PCIE_TYPE0_2	7:0	Revision ID	RO	0
0x08	PCIE_TYPE0_2	31:8	Class Code	RO	0x060400
0x0C	PCIE_TYPE0_3	7:0	Cache Line Size	R/W	0
0x0C	PCIE_TYPE0_3	15:8	Primary Latency Timer	RO	0
0x0C	PCIE_TYPE0_3	23:16	Header Type	RO	0x01
0x0C	PCIE_TYPE0_3	31:24	BIST	See PCIe Spec	0

Table 96. Type 1 Configuration Space Header Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x10	PCIE_TYPE0_4	31:0	Base Address 0	See PCIe Spec	0
0x14	PCIE_TYPE0_5	31:0	Base Address 1	See PCIe Spec	0
0x18	PCIE_TYPE0_6	7:0	Primary Bus Number	R/W	0
0x18	PCIE_TYPE0_6	15:8	Secondary Bus Number	R/W	0
0x18	PCIE_TYPE0_6	23:16	Subordinate Bus Number	R/W	0
0x18	PCIE_TYPE0_6	31:24	Secondary Latency Timer	RO	0
0x1C	PCIE_TYPE0_7	7:0	I/O Base	R/W	0x01
0x1C	PCIE_TYPE0_7	15:8	I/O Limit	R/W	0x01
0x1C	PCIE_TYPE0_7	31:16	Secondary Status	See PCIe Spec	0
0x20	PCIE_TYPE0_8	15:0	Memory Base	See PCIe Spec	0
0x20	PCIE_TYPE0_8	31:16	Memory Limit	See PCIe Spec	0
0x24	PCIE_TYPE0_9	15:0	Prefetchable Memory Base	See PCIe Spec	0x0001
0x24	PCIE_TYPE0_9	31:16	Prefetchable Memory Limit	See PCIe Spec	0x0001
0x28	PCIE_TYPE0_10	31:0	Prefetchable Base Upper 32 bits	R/W	0
0x2C	PCIE_TYPE0_11	31:0	Prefetchable Limit Upper 32 bits	R/W	0
0x30	PCIE_TYPE0_12	15:0	I/O Base Upper 16 bits	R/W	0
0x30	PCIE_TYPE0_12	31:16	I/O Limit Upper 16 bits	R/W	0
0x34	PCIE_TYPE0_13	7:0	Capabilities Pointer	RO	0x80
0x34	PCIE_TYPE0_13	31:8	Reserved	RO	0
0x38	PCIE_TYPE0_14	31:0	Expansion ROM Base Address	RO	0
0x3C	PCIE_TYPE0_15	7:0	Interrupt Line	R/W	0xFF
0x3C	PCIE_TYPE0_15	15:8	Interrupt Pin	RO	0x01
0x3C	PCIE_TYPE0_15	31:16	Bridge Control	See PCIe Spec	0

4.5.3 PCI Power Management Capability

Figure 56 details the structure of register fields for Power Management registers and Table 97 describes the register's fields.

Figure 56. Power Management Registers

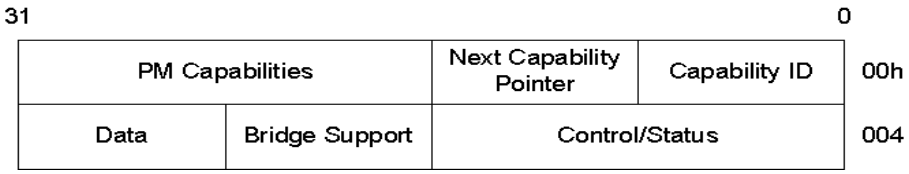


Table 97. Power Management Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x80	PM_CAP_0	7:0	Capability ID	RO	0x01
0x80	PM_CAP_0	15:8	Next Capability Pointer	RO	0x88
0x80	PM_CAP_0	31:16	PM Capabilities	See PCIe Spec	0xFEC3
0x84	PM_CAP_1	15:0	Control and Status	See PCIe Spec	Up/Dn - 0x0008 EMEP - 0x0
0x84	PM_CAP_1	23:16	Bridge Support	See PCIe Spec	0x00
0x84	PM_CAP_1	31:24	Data	See PCIe Spec	0x00

4.5.4 MSI Capability

MSI Capabbilty exists in PCIE Switch Bridges and in Embedded Endpoints

Figure 57 details structure of register fields for MSI registers and Table 98 describes the register's fields.

Figure 57. MSI Registers

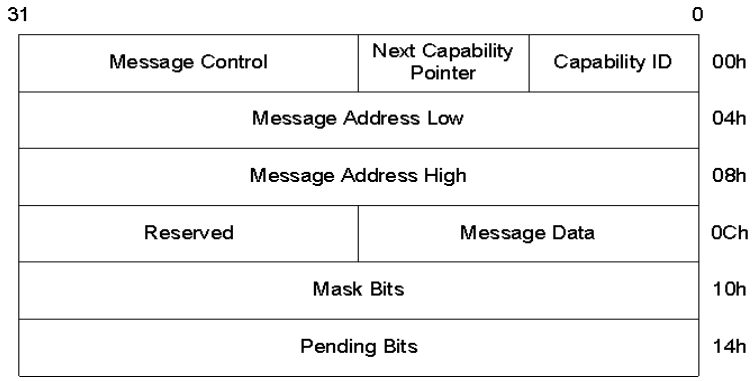


Table 98. MSI Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x88	MSI_CAP_0	7:0	Capability ID	RO	0x05

Table 98. MSI Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x88	MSI_CAP_0	15:8	Next Capability Pointer	RO	Up/Dn - 0xAC EMEP - 0xC0
0x88	MSI_CAP_0	31:16	Message Control	See PCIe Spec	Up/Dn - 0x0080 DMA EP - 0x0080 XHC EP - 0x0086
0x8C	MSI_CAP_1	31:0	Message Address Low	R/W	0
0x90	MSI_CAP_2	31:0	Message Address High	R/W	0
0x94	MSI_CAP_3	15:0	Message Data	R/W	0
0x94	MSI_CAP_3	31:16	Reserved	RO	0
0x98	MSI_CAP_4	31:0	Mask Bits	R/W	0
0x9C	MSI_CAP_5	31:0	Pending Bits	RO	0

4.5.5 Subsystem Vendor ID and Subsystem ID Capability

Standard SubSystem and SubVendor ID Capability that resides in Capability linked list of Upstream and Downstream Bridges. (EMEP contains these fields in Configuration Space Header).

The registers can be loaded from FLASH during boot to values other than default.

Figure 58. Sub System and Sub Vendor ID Registers

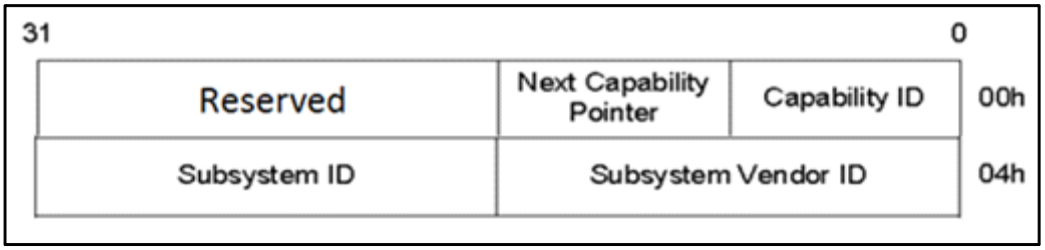


Table 99. Sub System and Sub Vendor ID Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0xAC	SUBSYS_CAP_0	7:0	Capability ID	RO	0x0D
0xAC	SUBSYS _CAP_0	15:8	Next Capability Pointer	RO	0xC0
0xAC	SUBSYS _CAP_0	31:16	Reserved	RO	0x0
0xB0	SUBSYS _CAP_1	15:0	Subsystem Vendor ID	RO	0x2222
0xB0	SUBSYS _CAP_1	31:16	Subsystem ID	RO	0x1111

4.5.6 PCI Express Capability

Figure 59 details the structure of the register fields for PCIe Capabilities registers and Table 100 describes the register's fields (see also Table 101).

Figure 59. PCI Express Registers

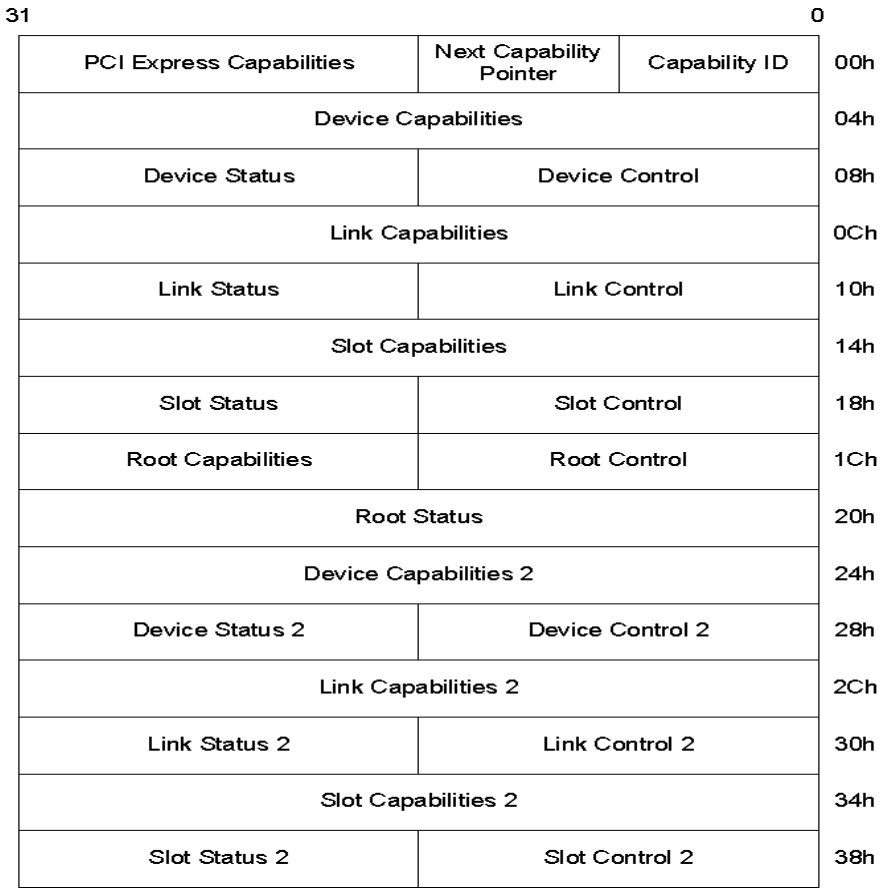


Table 100. PCI Express Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0xC0	PCIE_CAP_0	7:0	Capability ID	RO	0x10
0xC0	PCIE_CAP_0	15:8	Next Capability Pointer	RO	Up/Dn – 0 XHC EMEP - 0 (last) DMA EMEP – 0xA0 (MSIx)
0xC0	PCIE_CAP_0	31:16	PCI Express Capabilities	See PCIe Spec	Up - 0x0052 Dn - 0x0162 EMEP - 0x0002
0xC4	PCIE_CAP_1	31:0	Device Capability	See PCIe Spec	0x00008020
0xC8	PCIE_CAP_2	15:0	Device Control	See PCIe Spec	0x2810
0xC8	PCIE_CAP_2	31:16	Device Status	See PCIe Spec	Up/Dn – 0 EMEP - 0x0010

Table 100. PCI Express Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0xCC	PCIE_CAP_3	31:0	Link Capability	See PCIe Spec	0x0027_FC43 Some fields change according to Port number and Speed / Link Width limit See PCIe Spec
0xD0	PCIE_CAP_4	15:0	Link Control	See PCIe Spec	0
0xD0	PCIE_CAP_4	31:16	Link Status	See PCIe Spec	16'h1041
0xD4	PCIE_CAP_5	31:0	Slot Capability	See PCIe Spec	0x0004_0060 Some fields change according to Port number See PCIe Spec
0xD8	PCIE_CAP_6	15:0	Slot Control	See PCIe Spec	0
0xD8	PCIE_CAP_6	31:16	Slot Status	See PCIe Spec	0
0xDC	PCIE_CAP_7	15:0	Root Control	See PCIe Spec	0
0xDC	PCIE_CAP_7	31:16	Root Capability	See PCIe Spec	0
0xE0	PCIE_CAP_8	31:0	Root Status	See PCIe Spec	0
0xE4	PCIE_CAP_9	31:0	Device Capability 2	See PCIe Spec	32'h0000812
0xE8	PCIE_CAP_10	15:0	Device Control 2	See PCIe Spec	0
0xE8	PCIE_CAP_10	31:16	Device Status 2	See PCIe Spec	0
0xEC	PCIE_CAP_11	31:0	Link Capability 2	See PCIe Spec	0
0xF0	PCIE_CAP_12	15:0	Link Control 2	See PCIe Spec	0x0000_0003 See PCIe Spec
0xF0	PCIE_CAP_12	31:16	Link Status 2	See PCIe Spec	0x0000_0040 See PCIe Spec
0xF4	PCIE_CAP_13	31:0	Slot Capability 2	See PCIe Spec	0
0xF8	PCIE_CAP_14	15:0	Slot Control 2	See PCIe Spec	0
0xF8	PCIE_CAP_14	31:16	Slot Status 2	See PCIe Spec	0

4.5.7 MSIx Capability

MSIx Capability exists only in the DMA Embeded Endpoint.

Figure 60 details the structure of the register fields for MSIx registers. Table 101 describes the register's fields.

Figure 60. MSIx Registers

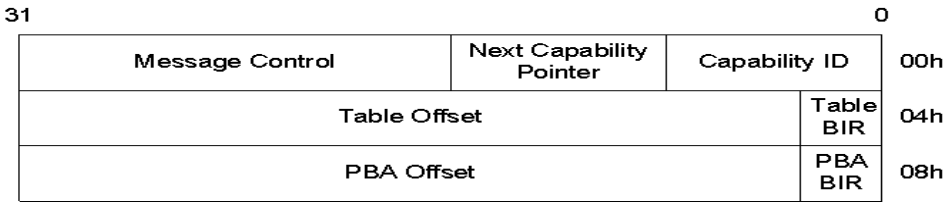


Table 101. MSIx Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0xA0	MSIX_CAP_0	7:0	Capability ID	RO	0x11
0xA0	MSIX_CAP_0	15:8	Next Capability Pointer	RO	0
0xA0	MSIX_CAP_0	31:16	Message Control	See PCIe Spec	0
0xA4	MSIX_CAP_1	2:0	Table BIR	RO	32b - 0x1 64b -0x2
0xA4	MSIX_CAP_1	31:3	Table Offset	RO	0
0xA8	MSIX_CAP_2	2:0	PBA BIR	RO	32b - 0x1 64b -0x2
0xA8	MSIX_CAP_2	31:3	PBA Offset	RO	0x1F4

4.5.8 Device Serial Number Capability

Figure 61 details the structure of the register fields for Device Serial Number registers and Table 102 describes the register's fields.

Figure 61. Device Serial Number Registers

Table 102. Device Serial Number Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x100	DSN_CAP_0	31:0	PCI Express Enhance Capability Header	RO	0x20010003
0x104	DSN_CAP_1	31:0	Serial Number Register (Lower DW)	RO	0x00C9A000
0x108	DSN_CAP_2	31:0	Serial Number Register (Upper DW)	RO	0x01000000

4.5.9 Advanced Error Reporting Capability

Figure 62 details the structure of the register fields for Advanced Error Reporting registers and Table 103 describes the register's fields.

Figure 62. Advanced Error Reporting Registers

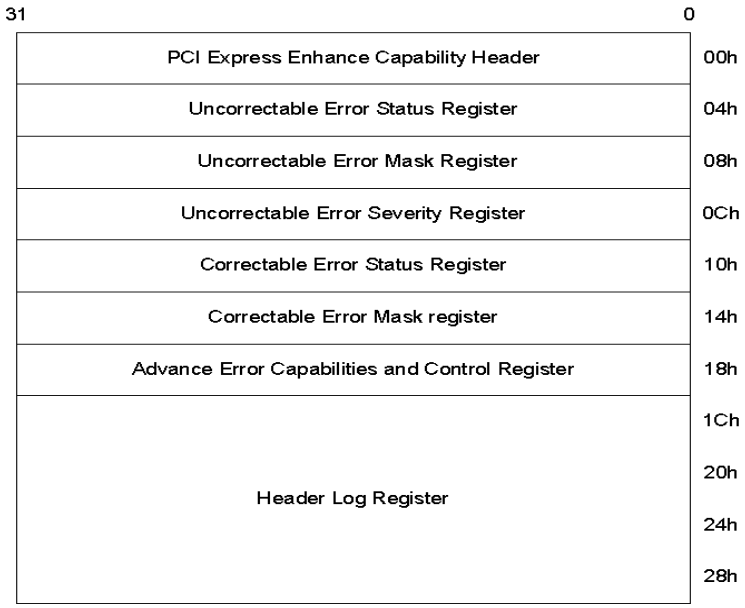


Table 103. Advanced Error Reporting Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x200	AER_CAP_0	31:0	PCI Express Enhanced Capability Header	RO	0x30010001
0x204	AER_CAP_1	31:0	Uncorrectable Error Status Register	See PCIe Spec	0
0x208	AER_CAP_2	31:0	Uncorrectable Error Mask Register	See PCIe Spec	0
0x20C	AER_CAP_3	31:0	Uncorrectable Error Severity Register	See PCIe Spec	Up/Dn0x00462010 DMA EMEP - 0x00062010
0x210	AER_CAP_4	31:0	Correctable Error Status Register	See PCIe Spec	0
0x214	AER_CAP_5	31:0	Correctable Error Mask register	See PCIe Spec	0x00002000
0x218	AER_CAP_6	31:0	Advance Error Capabilities and Control Register	See PCIe Spec	0
0x21C	AER_CAP_7	31:0	Header Log Register 0	ROS	0
0x220	AER_CAP_8	31:0	Header Log Register 1	ROS	0
0x224	AER_CAP_9	31:0	Header Log Register 2	ROS	0
0x228	AER_CAP_10	31:0	Header Log Register 3	ROS	0

4.5.10 Virtual Channel Capability

Figure 63 details the structure of the register fields for Virtual Channel registers and Table 104 describes the register's fields.

Last three registers exists for VC0 and VC1. VC1 part can be configured as part of QoS feature support and also can be hidden in custom QoS support.

Figure 63. Advanced Error Reporting Registers

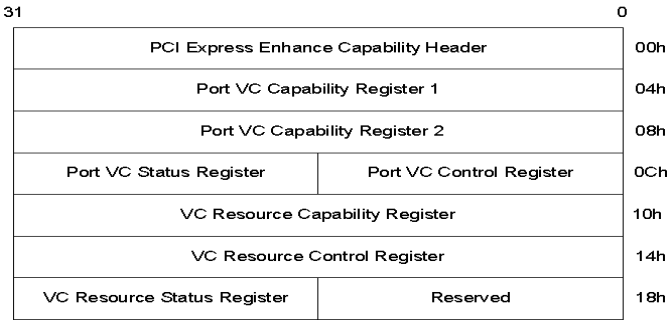


Table 104. Advanced Error Reporting Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x300	VC_CAP_0	31:0	PCI Express Enhance Capability Header	RO	0x40010002
0x304	VC_CAP_1	31:0	Port VC Capability Register 1	RO	0
0x308	VC_CAP_2	31:0	Port VC Capability Register 2	RO	0
0x30C	VC_CAP_3	15:0	Port VC Control Register	3:0 -R/W 15:4 - RsvdP	0
0x30C	VC_CAP_3	31:16	Port VC Status Register	16 - RO 31:17 - RsvdZ	0
0x310	VC_CAP_4	31:0	VC Resource Capability Register	See PCIe Spec	0
0x314	VC_CAP_5	31:0	VC Resource Control Register	R/W *Reserved bits - RsvdP	0x800000FF
0x318	VC_CAP_6	15:0	Reserved	RsvdP	0
0x318	VC_CAP_6	31:16	VC Resource Status Register	17:16 - RO 31:18 - RsvdZ	0x0002
0x31C	VC_CAP_7	31:0	VC1 Resource Capability Register	See PCIe Spec	0
0x320	VC_CAP_8	31:0	VC1 Resource Control Register	R/W *Reserved bits - RsvdP	0
0x324	VC_CAP_9	15:0	Reserved	RsvdP	0
0x324	VC_CAP_9	31:16	VC1 Resource Status Register	17:16 - RO 31:18 - RsvdZ	0

4.5.11 Power Budgeting Capability

Figure 64 details the structure of the register fields for Power Budgeting registers and Table 105 describes the register's fields.

Figure 64. Power Budgeting Registers

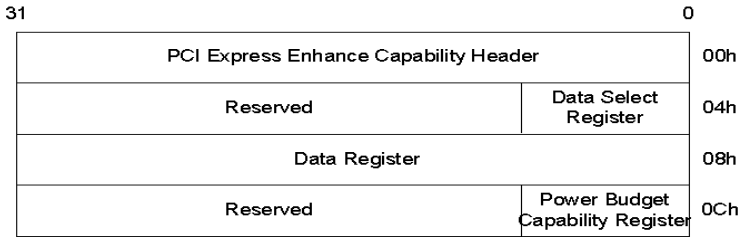


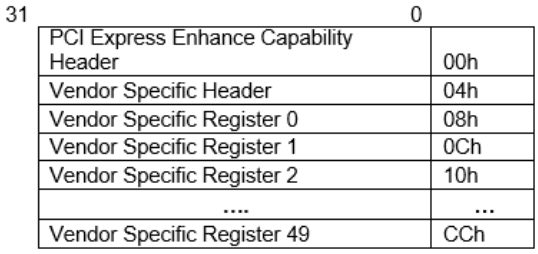
Table 105. Power Budgeting Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x400	PB_CAP_0	31:0	PCI Express Enhance Capability Header	RO	0x50010004
0x404	PB_CAP_1	7:0	Data Select Register	R/W	0
0x404	PB_CAP_1	31:8	Reserved	RsvdP	0
0x408	PB_CAP_2	31:0	Data Register	RO	0x00078200
0x40C	PB_CAP_3	7:0	Power Budget Capability Register	0- HwInit 7:1- RsvdP	0
0x40C	PB_CAP_3	31:8	Reserved	RsvdP	0

4.5.12 Vendor Specific Enhanced Capability

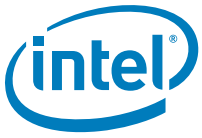
Figure 65 details the structure of register fields for Vendor Specific Enhanced registers and Table 106 describes the register's fields. These registers contain general purpose bits: different modes, dft bits and chicken bits. Vendor Registers might be loaded from FLASH.

Figure 65. Vendor Specific Enhanced Registers



Legacy Vendor Registers (Falcon Ridge):

"Reg 0 (0x8) - General configuration register



"Reg 1 (0xC) - General configuration register

"Reg 2 (0x10) - General configuration register

"Reg3 (0x14) - Power Budget register

"Reg4 (0x18) - Custom Hot Plug / BIOS register

"Reg5 (0x1C) - General configuration register

"Reg6 (0x20) - General configuration register

"Reg7 (0x24) - Custom NVM register

"Reg8 (0x28) - DFT register 1 (RO)

"Reg9 (0x2C) - DFT register 2 (RW)

"Reg10 (0x30) - Custom Reg access (Command Register)

"Reg11 (0x34) - Custom Reg access (Write Data Register)

"Reg12 (0x38) - Custom Reg access (Read Data Register)

"Reg13 (0x3C) - Custom LTR register 1

"Reg14 (0x40) - Custom LTR register 2

"Reg15 (0x44) - Custom LTR register 3

"Reg16 (0x48) - Custom Vendor Register 1 (RO)

"Reg17 (0x4C) - Custom Vendor Register 2 (RW)

"Reg18 (0x50) - CAB VC0 Register

"Reg19 (0x54) - CAB VC1 Register

"Reg20 (0x58) - QoS configuration register (empty)

"Reg21 (0x5C) - QoS Load priority & Custom mode register

"Reg22 (0x60) - QoS Shadow and VC Control Registers

"Reg23 (0x64) - QoS Tx / Rx TC Remapping Register

"Reg24 (0x68) - QoS Rx Remap Table (Entry0)

"Reg25 (0x6C) - QoS Rx Remapping Table (Entry1)

"Reg26 (0x70) - QoS Rx Remapping Table (Entry2)

"Reg27 (0x74) - QoS Rx Remapping Table (Entry3)

"Reg28 (0x78) - QoS Rx Remapping Table (Entry4)

"Reg29 (0x7C) - QoS Rx Remapping Table (Entry5)

"Reg30 (0x80) - QoS Rx Remapping Table (Entry6)

"Reg31 (0x84) - QoS Rx Remapping Table (Entry7)

"Reg32 (0x88) - Custom Port Arbitration register 1

"Reg33 (0x8C) - Custom Port Arbitration register 2

"Reg34 (0x90) - General configuration register

"Reg35 (0x94) - Custom PTM register 1

"Reg36 (0x98) - Custom PTM register 2

"Reg37 (0x9C) - Custom PTM register 3

"Reg38 (0xA0) - Custom L2 feature register

"Reg39 (0xA4) - Custom Compliance Pattern register 1

"Reg40 (0xA8) - Custom Compliance Pattern register 2

"Reg41 (0xAC) - General configuration register

"Reg42 (0xB0) - General configuration register

"Reg43 (0xB4) - General configuration register

"Reg44 (0xB8) - General configuration register

"Reg45 (0xBC) - General configuration register

"Reg46 (0xC0) - General configuration register

"Reg47 (0xC4) - General configuration register

"Reg48 (0xC8) - General configuration register

"Reg49 (0xCC) - General configuration register

Table 106. Vendor Specific Enhanced Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x500	VS_CAP_0	31:0	PCI Express Enhance Capability Header	RO	0x6001000B
0x504	VS_CAP_1	31:0	Vendor Specific Header	RO	0x05011234
0x508	VS_CAP_2	31:0	Vendor Register 0 (VESC_REG0)	R/W	See following tables
…	…	31:0	…	R/W	See following tables
0x5CC	VS_CAP_49	31:0	Vendor Register 0 (VESC_REG0)	R/W	See following tables

Table 107. VESC_REG0 (Offset 08h): General configuration register

Offset	Bits	Description	Value
0x508	vesc_reg0[13:0]	Replay timer value (in units of clocks) Gen1 – 16ns Gen2 – 8ns Gen3 – 4 ns Loaded when bit 31 is written	14'h950 (14'h6000 should be set for Tunneled Link with Clock Request support)
0x508	vesc_reg0[14]	TXSwing control 1'b0: PHY is directed to be in Full swing mode (default). 1'b1: PHY is directed to be in Low swing mode.	1'b0
0x508	vesc_reg0[16:15]	Loopback_control 2'b01: loopback end 2'b10: loopback start	(DFT) 2'b0
0x508	vesc_reg0[17]	Clkreq_p0top2 1'b0: MAC moves the PHY to P1 during clkreq# transition. 1'b1: MAC moves the PHY to P2 during clkreq# transition.	1'b0
0x508	vesc_reg0[18]	enab_urcomp_typ0cfgrd_busnum_mismatch 1'b0: Bus Num is not checked in Type0 CfgRd. 1'b1: Port sends Cmpl with UR status when the destination bus number in Type0 CfgRd doesn't match the actual bus number of the port (This bit is valid only for Up/EP, and reserved for Dn ports)	(Up/EP) 1'b0
0x508	vesc_reg0[19]	Virtual Gen2/Gen3 Enable 1'b0: Ports counters are according to it's rate. 1'b1: Enables indication to the port that it in Gen1 running with Gen2/Gen3 clocks	1'b1
0x508	vesc_reg0[20]	enable_expectValidTLP 1'b0: No Filtering STP 1'b1: Filtering of STP on certain states when no TLP is expected (to prevent error status bits setting)	1'b1
0x508	vesc_reg0[21]	detect_missingEOP_after4K 1'b0: Missing End of Packet is detected after Max Payload Size value programmed by software. 1'b1: Missing End of Packet is detected after 4K bytes	1'b1
0x508	vesc_reg0[22]	Select_gen1_gen2 1'b0: No effect 1'b1: Force Port to stay in Gen1 during Link negotiation	(DFT) 1'b0

Offset	Bits	Description	Value
0x508	vesc_reg0[23]	enable_eidleinfer_dllp 1'b0: L0 Electrical Idle inference lack of SKIP received 1'b1: L0 Electrical Idle inference lack of SKIP/DLLP received Related to other chicken bit (vesc_reg6[31])	1'b1
0x508	vesc_reg0[24]	RxInL0s_L1ASPM_enable 1'b0: L0sRx is not a condition for L1 ASPM entry. 1'b1: Port must be in L0sRx to start L1 ASPM entry. (This bit is valid only for Up/EP, and reserved for Dn ports)	(Up/EP) 1'b0 – Dn 1'b1 – Up/EP
0x508	vesc_reg0[25]	disab_autospdchng_dncomp 1'b0: Up/EP initiates Speed Change after Init FC is completed. 1'b1: Disables auto speed change (This bit is valid only for Up/EP, and reserved for Dn ports)	(Up/EP) 1'b0
0x508	vesc_reg0[26]	L2_Det_Qual 1'b0: the "Detect" state of Downstream Port won't be taken in consideration while entering L2 1'b1: the "Detect" state of Downstream Port will be taken in consideration while entering L2 (This bit is valid only for Up, and reserved for Dn ports)	1'b0 – Dn/EP 1'b1 – Up
0x508	vesc_reg0[27]	L0sL1_Det_Qual 1'b0: the "Detect" state of Downstream Port won't be taken in consideration while entering L1 1'b1: the "Detect" state of Downstream Port will be taken in consideration while entering L1 (This bit is valid only for Up, and reserved for Dn ports)	1'b0 – Dn/EP 1'b1 – Up
0x508	vesc_reg0[28]	Lane negotiation method 1'b0 – dynamic lane negotiation (according to data) 1'b1 – static lane negotiation (according to xmode input)	1'b0
0x508	vesc_reg0[29]	Reserved	1'b0
0x508	vesc_reg0[30]	Endpoint Reset 1'b0: No Effect 1'b1: Endpoint device which connected to this Downstream Port will be reset (static bit) (This bit is valid only for Dn, and reserved for Up/EP ports)	(Dn port) 1'b0
0x508	vesc_reg0[31]	Load replay timer value When software writes 1 to bit 31, the value in bits [13:0] will get loaded into the internal replay timer register.	(Self-Cleared) 1'b0

Table 108. VESC_REG1 (Offset 0Ch): General configuration register

Offset	Bits	Description	Value
0x50C	vesc_reg1[0]	Switch cut-thru disable 1'b0: The decision to use cut-thru or store-forward mode on each port depends on the port rate and width 1'b1: The switch port will use store-forward mode always.	1'b1
0x50C	vesc_reg1[1]	Enable_wake 1'b0: No effect 1'b1: WAKE# is used to wake from L2	1'b0
0x50C	vesc_reg1[2]	Enable_beacon 1'b0: No effect 1'b1: Beacon is used to wake from L2	1'b0
0x50C	vesc_reg1[3]	L1_ASPM override 1'b0: No Effect 1'b1: L1 is disabled if configured by SW	1'b0/1'b1
0x50C	vesc_reg1[4]	L0STX Override 1'b0: No Effect 1'b1: L0STX is disabled if configured by SW	1'b0/1'b1
0x50C	vesc_reg1[5]	ClkReq Override 1'b0: Internal clock request functionality is enabled 1'b1: Disable internal clock request functionality	1'b1
0x50C	vesc_reg1[7:6]	losl1_timer_value L1 entry timer select 2'b00 - 4us 2'b01 - 8us 2'b10 - 12us 2'b11 - 16us (This bit is valid only for Up/EP, and reserved for Dn ports)	2'b11
0x50C	vesc_reg1[8]	Bypass_RxL0sTimer for_L1_disable 1'b0: Port waits some configurable time in L0sRx (bits 7:6), before starting L1 ASPM. 1'b1: Port doesn't waits in L0sRx, before starting L1. (This bit is valid only for Up/EP, and reserved for Dn ports)	1'b0
0x50C	vesc_reg1[9]	L1_RXEleIdle_TO_setting Timeout value for L1ASPM state machine to wait for Rx Electrical Idle condition. 1'b0: Times out after 5 us. 1'b1: Times out after 10 us.	1'b1

Offset	Bits	Description	Value
0x50C	vesc_reg1[10]	nonL0_rxelec_mask 1'b0: No effect 1'b1: Correctible error message generation and setting the correctible error status bit is disabled during the conditions when the link is in a non-L0 state and when Rx EI detected. (to prevent errors near EI transitions)	1'b1
0x50C	vesc_reg1[11]	In L0sTx state Hardware sets this bit when it enters L0sTx. Software can clear it by writing 1 to it.	1'b0
0x50C	vesc_reg1[12]	In L0sRx state Hardware sets this bit when it enters L0sRx. Software can clear it by writing 1 to it.	1'b0
0x50C	vesc_reg1[13]	In L1 state Hardware sets this bit when it enters L1. Software can clear it by writing 1 to it.	1'b0
0x50C	vesc_reg1[14]	In L2 state Hardware sets this bit when it enters L2. Software can clear it by writing 1 to it.	1'b0
0x50C	vesc_reg1[15]	Reserved	1'b0
0x50C	vesc_reg1[16]	disab_vga_routing 1'b0: vga_routing is enabled when vga_en bit is set by SW. 1'b0:vga routing is disabled even if vga_en bit is set by SW.	1'b0
0x50C	vesc_reg1[17]	disab_isa_routing 1'b0: ISA_routing is enabled when isa_en bit is set by SW. 1'b1: ISA routing is disabled even if isa_en bit is set by SW.	1'b0
0x50C	vesc_reg1[18]	RXDetect_Bypass 1'b0: RX Detection logic is NOT bypassed 1'b1: RX Detection logic is bypassed (DFT)	1'b0
0x50C	vesc_reg1[19]	l0srx_ctrbypass_enable 1'b0: Counter not bypassed 1'b1: In L0SRx state machine counter is bypassed when Rx EI condition is detected.	1'b1
0x50C	vesc_reg1[20]	PresenceDet_enable 1'b0: No effect 1'b1: Transitions from L0 to Recovery, and from Recovery to Detect state are accelerated when Presence = 0	1'b1

Offset	Bits	Description	Value
0x50C	vesc_reg1[21]	bypass_inl1 1'b0: Port condition to be in L1 will NOT be bypassed 1'b1: Port condition to be in L1 will be bypassed	1'b0/1'b1
0x50C	vesc_reg1[22]	bypass_inl0srx 0: Port condition to be in L0SRX will NOT be bypassed. 1: Port condition to be in L0SRX will be bypassed.	1'b0/1'b1
0x50C	vesc_reg1[23]	losl1_timer_value_inms L1 entry timer unit control 1'b0: bits[7:6] unit is in us 1'b1: bits[7:6] unit is in ms (DFT) (This bit is valid only for Up/EP, and reserved for Dn ports)	(Up/Ep) 1'b0
0x50C	vesc_reg1[24]	WAKE_pinB_qual 1'b0: WAKE_pinB is not used to exit from L2 1'b1: WAKE_pinB is used to exit from L2. (This bit is valid only for Dn, and reserved for Up/EP ports)	1'b0
0x50C	vesc_reg1[25]	Vendor_IOSpace_dis 1'b0: IO space is enabled. 1'b1: IO space is disabled. Following registers will return zero when accessed by software.	1'b0
0x50C	vesc_reg1[26]	l2eidlewait_en 1'b0: During L2 entry Port wait for partner to enter electrical idle before sending EIOS and entering EI. 1'b1: During L2 entry Port doesn't wait for partner and enters electrical idle on its own timing. (This bit is valid only for Dn, and reserved for Up/EP ports)	(Dn) 1'b1
0x50C	vesc_reg1[27]	hotrstexit_timer_en 1'b0: Waits for Rx electrical idle to make a transition from Hot Reset to Detect (Bug) 1'b1: exit to DETECT after 2ms timer expired and no Electrical Idle detected within that period (Bug Fix) (This bit is valid only for Dn, and reserved for Up/EP ports)	(Dn) 1'b1
0x50C	vesc_reg1[28]	LinkWidthCap_selection Link Width in Link Capabilty register selection control 1'b0: Set according to xmode input 1'b1: Set according to EEPORM load	1'b0

Offset	Bits	Description	Value
0x50C	vesc_reg1[29]	rcvrcfgtoidle_send32tsx_en Number of Tx TS2 during Recover.Config to Recovery.Idle transition. 34 TSx instead of 18. 1'b0: 18 TS2 are sent (default – according to Spec (16)) 1'b1: 34 TS2 are sent (DFT)	1'b0
0x50C	vesc_reg1[30]	rcvrcfgtoidle_rcv4tsx_en Expected Number of Rx TS2 during Recover.Config to Recovery.Idle transition. 1'b0: 8 TS2 expected (default – according to the Spec) 1'b1: 4 TS2 expected (DFT)	1'b0
0x50C	vesc_reg1[31]	cb_pme_err_message_dis 1'b0: PostReqProcVC0 block is blocked from sending extra credit update for PM_PME message (Bug fix) 1'b1: PostReqProcVC0 sends extra credit update for PM_PME message (Bug)	1'b0

Table 109. VESC_REG2 (Offset 10h): General configuration register

Offset	Bits	Description	Value
0x510	vesc_reg2[0]	Disable constant Clock Request Ack 1'b0: Clock request Ack is constant high. 1'b1: Clock request Ack is generated from delayed request.	1'b0
0x510	vesc_reg2[1]	Reserved	1'b0
0x510	vesc_reg2[2]	Power Down Delay Enable Delay of Power Down signal in case of Lane Reversal 1'b0: No effect 1'b1: Internal PIPE PowerDown signal delay of one cycle.	1'b0
0x510	vesc_reg2[3]	Reserved	1'b0
0x510	vesc_reg2[7:4]	L1 Entry Delay Counter Delays entry to L1 for configurable time: 4'h0 – No Delay, 4'h1 - ~1ms, 4'h2 - ~2ms, 4'h3 - ~4ms 4'h4 – ~8ms, 4'h5 – ~16ms, 4'h6 – ~64ms, 4'h7 – ~128ms 4'h8 – ~256ms, 4'h9 – ~0.5 sec, 4'hA – ~1 sec, 4'hB – ~2sec 4'hC – ~4 sec, 4'hD – ~8 sec, 4'hE – ~16 sec, 4'hF - ~32 sec	4'h0
0x510	vesc_reg2[8]	DFT PME generation 1'b0: No effect 1'b1: Sends PM_PME message till SW clears PME_Status	1'b0

Offset	Bits	Description	Value
0x510	vesc_reg2[9]	Disable Bus Capture from Host Interface 1'b0: Capture Bus and Dev Num only from PHY access 1'b1: Capture Bus and Dev Num from PHY / Host access. (This bit is valid only for Dn and reserved for Up/EP ports)	(Dn) 1'b0
0x510	vesc_reg2[10]	Host_datataken_datavalid chicken bit 1'b0: Backdoor register access bug is fixed. 1'b1: Backdoor register access bug fix is disabled.	1'b0
0x510	vesc_reg2[11]	cb_Ltr_value _maxlimit (LTR) 1'b0: Max LTR register doesn't limit the LTR final value. 1'b1: Max LTR register limits the LTR final value. (This bit is valid only for Up/EP and reserved for Dn ports)	(Up/EP) 1'b1
0x510	vesc_reg2[12]	cb_rxexit_duetorecov 1'b0: Port waits for periodic FC update to exit L0sRx before it can initiate Link Retrain. 1'b1: Port immediately exits from L0Srx and initiate Link Recovery (This bit is valid only for Dn and reserved for Up/EP ports)	(Dn) 1'b1
0x510	vesc_reg2[13]	cb_dynltr_sel (LTR) Selects between static and dynamic LTR value for Switch down ports that are connected with non-LTR capable EPs 1'b0: Dynamic LTR value 1'b1: Static LTR value	1'b0
0x510	vesc_reg2[16:14]	cb_prog_cons8count_value (DFT) Number of consecutive TS to be considered as 8. 3'h1 – two TS … 3'h7 – eight TS (Valid if bit 17 is set)	3'h0
0x510	vesc_reg2[17]	cb_prog_cons8count_enable 1'b0: Eight consecutive TS indication is set upon 8 TS. 1'b1: Enables Eight consecutive TS indication to be programmable (bits 16:14)	1'b0
0x510	vesc_reg2[19:18]	cb_replay_numlimit_sel (DFT) Selects the number of Replays till Recovery 2'b00: 16 2'b01: 32 2'b10: 64 2'b11: 256 (Valid if bit 21 is set)	2'b0

Offset	Bits	Description	Value
0x510	vesc_reg2[20]	cb_replay_norecov (DFT) 1'b0: Port goes to Recovery after 4 Replays (Spec) 1'b1: Port never goes to Recovery as a result of Replays (Valid if bit 21 is set)	1'b0
0x510	vesc_reg2[21]	cb_master_replay(DFT) 1'b0: No effect 1'b1: Enable for Replay manipulations (bits 20:18)	1'b0
0x510	vesc_reg2[22]	cb_extrenal_pme disable 1'b0: No effect 1'b1: Disables PME generation	1'b0
0x510	vesc_reg2[23]	cb_false_linkdown 1'b0: No effect 1'b1: Forces a Port to report link down condition (This bit is valid only for Dn, and reserved for Up/EP ports)	(Dn) 1'b0
0x510	vesc_reg2[24]	cb_disable_l1soft 1'b0: L1 Software is active (according to D-state) 1'b1: L1 Software is disabled (DFT) (This bit is valid only for Up/Ep and reserved for EP ports)	(Up/Ep) 1'b0
0x510	vesc_reg2[25]	cb_regacc_disable 1'b0: Configuration Space can be accessed through backdoor interface. 1'b1: Disables alternate backdoor register access feature	1'b0
0x510	vesc_reg2[26]	cb_ltr_disable (LTR) 1'b0: LTR is controlled by Software. 1'b1: Disables LTR feature (hide Capability).	1'b0
0x510	vesc_reg2[27]	cb_disab_redunrecov 1'b0: Redundant recovery fix is enabled. 1'b1: Redundant recovery fix is disabled.	1'b0
0x510	vesc_reg2[28]	cb_bypass_creditchk (QoS) 1'b0: default behavior when there is no QoS custom modes 1'b1: Bypass credit check when ingress port has VC1 enabled and egress port is custom VC0 only mode.	1'b0/1'b1
0x510	vesc_reg2[29]	disable_ecrc_fix 1'b0: ECRC fix of FC loss is enabled 1'b1: ECRC fix is disabled	1'b0

Offset	Bits	Description	Value
0x510	vesc_reg2[30]	cb_enable_vc1 (QoS) 1'b0: VC1 is disabled in PCIE Switch. 1'b1: VC1 in enabled in PCIE Switch. (This bit is valid only for Up and reserved for Dn/EP ports)	(Up) 1'b0/1'b1
0x510	vesc_reg2[31]	compbuff_perport enable (CAB) 1'b0: Completion Allocation Buffer is disabled 1'b1: Completion Allocation Buffer is enabled (This bit is valid only for Dn, and reserved for Up/EP ports)	(Dn) 1'b0/1'b1

Table 110. VESC_REG 3 (Offset 14h): General configuration register

Offset	Bits	Description	Value
0x510	vesc_reg3[7:0]	D0_MAX_3P3V_BASE_PWR Provides the max power consumption in D0 state from 3.3V power supply. Total power consumption is this value times scale (0.01)	8'h0
0x510	vesc_reg3[15:8]	D0_SUSTAINED_3P3V_BASE_PWR Provides the sustained power consumption in D0 state from 3.3V power supply. Total power consumption is this value times scale (0.01)	8'h0
0x510	vesc_reg3[23:16]	D3_MAX_3P3V_BASE_PWR Provides the max power consumption in D3 state from 3.3V power supply. Total power consumption is this value times scale (0.01)	8'h0
0x510	vesc_reg3[31:24]	D3_SUSTAINED_3P3V_BASE_PWR Provides the sustained power consumption in D3 state from 3.3V power supply. Total power consumption is this value times scale (0.01)	8'h0

Table 111. VESC_REG 4: (Offset 18h): Custom Hot Plug / BIOS register

Offset	Bits	Description	Value
0x518	vesc_reg4[31:0]	Custom use	32'h0

Table 112. VESC_REG 5: (Offset 1Ch): General configuration register

Offset	Bits	Description	Value
0x51C	vesc_reg5[0]	Reserved	1'b0
0x51C	vesc_reg5[1]	d0u_hot_plug_fix_en 1'b0: D0U is not considered in Hot Plug PM PME generation 1'b1: D0U is considered during Hot Plug PM PME generation (This bit is valid only for Dn and reserved for Up/EP ports)	(Dn) 1'b1

Offset	Bits	Description	Value
0x51C	vesc_reg5[2]	LTR close msg fix disable (LTR) 1'b0 – close ltr Message handling enabled 1'b1 – close ltr Message handling disabled	1'b0
0x51C	vesc_reg5[3]	LTR extra msg fix disable (LTR) 1'b0 – Does not send duplicate ltr message 1'b1 – sends duplicate ltr message	1'b0
0x51C	vesc_reg5[4]	cb_l2_rate_fix_en 1'b0 – During L2, does speed change only at Detect (bug) 1'b1 – Does speed change in L2.	1'b1
0x51C	vesc_reg5[5]	Exit from L2 on PERST# 1'b0 – Do not exit from L2 when PCIRST is there. 1'b1 – Exit from L2 when PCIRST is there. (This bit is valid only for Up/EP and reserved for Dn ports)	(Up/Ep) 1'b1
0x51C	vesc_reg5[6]	L1 entry during L2 fix disable 1'b0 – Port doesn't erter L1 ASPM if L2L3 is in progress 1'b1 – Port enter L1 ASPM if L2L3 is in progress (bug) (This bit is valid only for Up/EP and reserved for Dn ports)	(Up/Ep) 1'b0
0x51C	vesc_reg5[7]	L0s entry during L1/L2 fix disable 1'b0 – Port doesn't enter L0sTx if L2L3 or L1 is in progress 1'b1 – Port enter L0sTx ASPM if L2L3 or L1 in progress (bug)	1'b0
0x51C	vesc_reg5[8]	L1 Soft exit timer fix disable 1'b0: Dn Port does not wait for 1.5 ms during L1 soft exit 1'b1: Dn Port waits for 1.5 ms during L1 soft exit (bug) (This bit is valid only for Dn and reserved for Up/EP ports)	(Dn) 1'b0
0x51C	vesc_reg5[9]	LTR dependency on Dn fix 1'b0: LTR message will be sent only if at least one downstream port received LTR message from Endpoint device 1'b1: Fix that doesn’t check if LTR message was received once (This bit is valid only for Up and reserved for Dn/EP ports)	(Up) 1'b1

Offset	Bits	Description	Value
0x51C	vesc_reg5[10]	LTR dependency on Dn fix 1'b0: if any of downstream ports is locked there is no need to receive at least one LTR message to send one (default) 1'b1: LTR message will be sent only if at least one downstream port received LTR message from Endpoint device (This bit is valid only for Up and reserved for Dn/EP ports)	1'b0
0x51C	vesc_reg5[11]	Disable TLP Event in Fifo 1'b0 : New TLP event is done through FIFO for rate change. 1'b1 : Previous method of transferring the New TLP Event.	1'b0
0x51C	vesc_reg5[12]	Disable peer to peer ordering fix 1'b0 : Peer to Peer ordering issue is fixed 1'b1 : Peer to Peer Ordering issue is not fixed (This bit is valid only for Dn and reserved for Up/EP ports)	(Dn) 1'b0
0x51C	vesc_reg5[13]	EMEP L2 Seq Wake 1'b0 : Do not exit from TRANSIT_P1 state of L2SeqWake FSM. 1'b1 : Exit from TRANSIT_P1 state of L2SeqWake FSM. (This bit is valid only for Dn and reserved for Up/EP ports)	(Ep) 1'b1
0x51C	vesc_reg5[14]	cb_LTR_nonzeroTC_dis 1'b0: Flags a Malformed TLP upon LTR Msg with non-zero TC. 1'b1: Port does not flag a Malformed TLP upon LTR Msg with non-zero TC.	(Dn) 1'b0
0x51C	vesc_reg5[15]	cb_LTR_notexpected_dis 1'b0 : Port flags a Malformed TLP upon LTR Msg. 1'b1 : Port does not flag a Malformed TLP upon LTR Msg. (This bit is valid only for Up/EP and reserved for Dn ports)	(Up/Ep) 1'b0
0x51C	vesc_reg5[16]	cb_nonzro_TC_msg_acpt 1'b0: Do not Accept Msg TLP's with non zero TC.Flag it as Malformed TLP. 1'b1: Accept TLP's with non zero TC.Do not Flag it as Malformed TLP.	1'b0
0x51C	vesc_reg5[17]	cb_idle_to_rlock_disable_invert 1'b0: Cfg.Idle to Recovery transition is fixed 1'b1: Bug in transition from Cfg.Idle to recovery	1'b0

Offset	Bits	Description	Value
0x51C	vesc_reg5[18]	cb_low_addr_fix_disable 1'b0: Lower address and byte count of UR CPL is fixed 1'b1: Bad Lower address and byte count of UR CPL is fixed	1'b0
0x51C	vesc_reg5[19]	cb_disable_swdn_rcvd_beacon 1'b0: Detection Beacon during L2 is active 1'b1: Disables Beacon Detection (This bit is valid only for Dn and reserved for Up/EP ports)	(Dn) 1'b0
0x51C	vesc_reg5[20]	cb_fts_ext_sync_3k_or_4k Selects the number of transmitted FTS extended sync bit 1'b0: 4095 1'b1: 3000	1'b1
0x51C	vesc_reg5[21]	cb_update_fc_maltlp_en 1'b0: Port doesn't update FC credits for malformed TLP's 1'b1: Port updates FC credits for malformed TLP's	1'b0
0x51C	vesc_reg5[22]	cb_obff_enable_wr_en 1'b0: OBFF enable is not writable when 1'b1: OBFF enable is still writable Note: OBFF is not supported	1'b0
0x51C	vesc_reg5[23]	cb_aspm_speed_chg_disable 1'b0: Speed Change fix during ASPM Prep is enabled 1'b1: Speed Change fix during ASPM Prep is disabled	1'b0
0x51C	vesc_reg5[24]	cb_tcvc_mapping_shadow_disable (QoS) 1'b0: TC/VC mapping is done with shadow VC1 register 1'b1: TC VC mapping is done with spec VC1 register	1'b0/1'b1
0x51C	vesc_reg5[25]	cb_eidle_infer_disable 1'b0: The issue of Eidle inferrence is fixed. 1'b1: The issue of Eidle inferrence is not fixed.	1'b0
0x51C	vesc_reg5[26]	cb_eidle_infer_anylane_disable 1'b0: The issue of Eidle inferrence for anylane is fixed. 1'b1: The issue of Eidle inferrence for anylane is not fixed.	1'b0
0x51C	vesc_reg5[27]	cb_crdtchk_hdr_arb_fix_disable_chan0 1'b0: The hdr threshold on channel 0 is 'd1 1'b1: The hdr threshold on channel 0 is 'd2	1'b0
0x51C	vesc_reg5[28]	cb_crdtchk_hdr_arb_fix_disable_chan1 1'b0: The hdr threshold on channel 1 is 'd1 1'b1: The hdr threshold on channel 1 is 'd2	1'b0

Offset	Bits	Description	Value
0x51C	vesc_reg5[29]	cb_crdtchk_data_arb_fix_disable_chan1 1'b0: The hdr threshold on channel 1 is ‘d8 1'b1: The the hdr threshold on channel 1 is ‘d16	1'b0
0x51C	vesc_reg5[30]	cb_crdtchk_hdr_arb_fix_disable_chan2 1'b0: The hdr threshold on channel 2 is ‘d1 1'b1: The hdr threshold on channel 2 is ‘d2	1'b0
0x51C	vesc_reg5[31]	cb_crdtchk_data_arb_fix_disable_chan2 1'b1: The hdr threshold on channel 2 is ‘d16 1'b0: The hdr threshold on channel 2 is ‘d8	1'b0

Table 113. VESC_REG 6: (Offset 20h): General configuration register

Offset	Bits	Description	Value
0x520	vesc_reg6[0]	cb_eieos_32_rcvrcfglock_enable – Default 1’b0 1'b0: EIEOE in RCVR.CFG is sent after every 33 TS in (non Gen1) 1'b1: EIEOS in RCVR.CFG is sent after every 32 TS in (non Gen1)	1'b1
0x520	vesc_reg6[1]	cb_eieos_32_rcvrlock_enable – Default 1’b0 1'b0: EIEOE in RCVR.CFG is sent after every 31 TS in (non Gen1) 1'b1: EIEOS in RCVR.CFG is sent after every 32 TS in (non Gen1)	1'b1
0x520	vesc_reg6[2]	cb_eieos_cfg_first_TS_enable – Default 1’b0 1'b1: EIEOS in is not sent CFG.LINKWIDTHSTART before first TS. 1'b1: EIEOS in CFG.LINKWIDTHSTART is sent before first TS.	1'b1
0x520	vesc_reg6[3]	cb_eidle_pulse_fix_enable – Default 1’b0 1'b0: Tx Elec Idle pulse occurs when in Detect state 1'b1: Fix to eliminate Tx Elec Idle pulse when in Detect state.	1'b1
0x520	vesc_reg6[4]	cb_ln0_LinkNum_fix_enable– Default 1’b0 1'b0: Rcved TS Link Number is checked only on Ln0 (Bug) 1'b1: Rcved TS Link Number is checked on all lanes (Spec)	1'b1
0x520	vesc_reg6[5]	cb_updtltr1_lockmask_unset_enable (LTR) 1'b0: LTR1 register in Downstream ports is not updated when LTR1 lock or mask bits are unset. 1'b1: LTR1 register in Downstream ports is updated when LTR1 lock or mask bits are unset.	1'b1
0x520	vesc_reg6[6]	cb_max_val_chg_sndltr_enable (LTR) 1'b0: Doesn't send LTR Message from EndPoint (EMEP) if max ltr register change causes a change in the latency value. (This bit is valid only for Ep and reserved for Up/Dn ports) 1'b1: Send LTR Message from if max ltr register change causes a change in the latency value.	(Ep) 1'b1

Offset	Bits	Description	Value
0x520	vesc_reg6[7]	cb_notlimit_lswitch_enable (LTR) 1'b0: Lswitch value is limited to 20% (25%) of LTR Dn min (Bug) 1'b1: Lswitch value is not limited to 20% (25%) of LTR Dn min (This bit is valid only for Up and reserved for Dn/Ep ports)	(Up) 1'b1
0x520	vesc_reg6[8]	cb_noreq_bit_ltr1_nonD0_enable (LTR) 1'b0: The LTR requirement stays high upon entry to non-D0 state high if Port in locked (Bug) 1'b0: The LTR requirement get reset upon entry to non-D0 state high if Port in locked (Bug) (This bit is valid only for Dn and reserved for up/Ep ports)	(Dn) 1'b1
0x520	vesc_reg6[9]	cb_allanylane_lpback_fix_enable 1'b0: In Cfg port checks on loopback bit set on any lane. 1'b0: In Cfg port checks on loopback bit set on all lane. on all lanes.	1'b0
0x520	vesc_reg6[10]	cb_DstateSM_reset_noDLDown_enable –Default 1’b0 1'b0: DstateSM reset is on Link Down (DL Down). 1'b1: DstateSM doesn’t reset on Link Down (DL Down).	1'b0
0x520	vesc_reg6[11]	cb_ur_err_msg_status_enable 1'b0: Error Msg is not sent and error status bit is not set for non-active SWDN ports. 1'b1: Error Msg are sent and error status bit is set for non-active SWDN ports. (This bit is valid only for Up and reserved for Dn/Ep ports)	(Up) 1'b1
0x520	vesc_reg6[12]	cb_ur_dnport_id_enable 1'b0: UR CPL because of non-active downstream port have the Completer ID (B:D:F) of the upstream port. 1'b1: UR CPL because of non-active downstream port have the Completer ID (B:D:F) of the downstream port. (This bit is valid only for Up and reserved for Dn/Ep ports)	(Up) 1'b1
0x520	vesc_reg6[13]	cb_sig_sys_err_enable 1'b1: Signal System Error bit (Status Reg Offset 0x06) is set upon ERR_FATAL/NONFATAL Message and SERR# is 1’b1. 1'b1: Signal System Error bit (Status Reg Offset 0x06) is not set upon ERR_FATAL/NONFATAL Message and SERR# is 1’b1. (This bit is valid only for Dn and reserved for Up/Ep ports)	(Dn) 1'b1
0x520	vesc_reg6[14]	cb_mask_adv_err_cor_enable 1'b0: Advisory Error Correctable status is set upon FATAL error 1'b1: Advisory Error Correctable status is not set upon FATAL error	1'b1

Offset	Bits	Description	Value
0x520	vesc_reg6[15]	Reserved	1'b0
0x520	vesc_reg6[16]	cb_disable_MsgdestVC_byrouteID 1'b0: destVC for ID routed Messages is correctly computed (using the ID (B:D:F) information) 1'b1: destVC for ID routed Messages are incorrectly computed in (without using the ID (B:D:F) information)	1'b0
0x520	vesc_reg6[17]	cb_devnum_fix_disable 1'b0: Dev Num in the UR CPL's sent by Dn ports is 'correctly set to the Dn ports device number. 1'b1: Dev Num in the UR CPL's sent by Dn ports is 'd0. (This bit is valid only for Dn and reserved for Up/Ep ports)	1'b0
0x520	vesc_reg6[18]	cb_MRD_Lk_fix_disable 1'b0: UR CPL's Lock for MrdLk 32/64 are returned 1'b1: UR CPL's for MrdLk 32/64 are not returned	1'b0
0x520	vesc_reg6[20:19]	cb_room_avail_margin_select 2'b00 – Margin is 5'd8 2'b 01 – Margin is 5'd12 2'b 10 – Margin is 5'd16 2'b 11 – Not applicable but if programmed Margin is 5'd8	2'b00
0x520	vesc_reg6[22:21]	cb_min_idle_transmit_count While in Configuration : 2'b00 – Margin is 4'd2 2'b01 – Margin is 4'd3 2'b10 – Margin is 4'd6 2'b11 – Margin is 4'd7 While in Recovery : 2'b00 – Margin is 4'd4 2'b01 – Margin is 4'd5 2'b10 – Margin is 4'd8 2'b11 – Margin is 4'd9	2'b00
0x520	vesc_reg6[23]	cb_lane_reversal_disable 1'b0 : Lane reversal exists according to define 1'b1 : Lane reversal is disabled (even if defined)	1'b0
0x520	vesc_reg6[24]	cb_lane_reversal_x2_mode_disable : Default 1'b0 1'b0: Lane 0 is compared with 1 and Lane 1 with 0. 1'b1: Lane 0 is compared with 3 and Lane 1 with 2.	1'b0
0x520	vesc_reg6[26:25]	cb_update_fcq_wait_count : Default 1'b0 1'b0 : At gen1 speed wait for 5 cycles. 1'b1 : at gen1 speed wait for 4 cycles.	1'b0

Offset	Bits	Description	Value
0x520	vesc_reg6[27]	cb_sw_mode_err_cfgwr0_msgd_disab 1'b0: For poisoned TLP advisory error, CfgWr0 and MsgD are taken into account. 1'b1 : For poisoned TLP advisory error, CfgWr0 and MsgD are not taken into account.	1'b0
0x520	vesc_reg6[28]	Reserved	1'b0
0x520	vesc_reg6[29]	cb_prog_cons2_sel : Defaut 1'b0 1'b0: Counter value in TSXDet is set to 1 1'b1: Counter value in TSXDet is set to 2 (DFT)	1'b0
0x520	vesc_reg6[30]	cb_goto_quiet_rcvr_notdet: Defaut 1'b0 1'b0: Wait 12 ms before going to DETECT.QUIET when Rcvr is not detected on all lanes. 1'b1: Do not wait 12 ms and immediately go to DETECT.QUIET when Rcvr is not detected on all lanes.	1'b1
0x520	vesc_reg6[31]	cb_disable_eidleinfer_skip: Defaut 1'b0 1'b0: inferring eidle by skip absence is enabled 1'b1: inferring eidle by skip absence is disabled Related to other chicken bit (vesc_reg0[23])	1'b0

Table 114. VESC_REG 7: (Offset 24h): Custom NVM register

Offset	Bits	Description	Value
0x524	vesc_reg7[31:0]	Custom use	32'h0

Table 115. VESC_REG 8: (Offset 28h): DFT register 1 (RO)

Offset	Bits	Description	Value
0x528	vesc_reg8[31:0]	Read Only register that collects several internal Hardware indication for Debug Bit 31 – Data Link is Active Bit 30 – Link Up Other bits changes according to configuration. 4 options controlled by vesc_reg9[31:30]	32'h0

Table 116. VESC_REG 9: (Offset 2Ch): DFT register 2

Offset	Bits	Description	Value
0x52C	vesc_reg9[9:0]	Recovery cause Entry to Recovery sticky Bit9 – Received TS Bit8 – Presence change (Unplug) Bit7 – TLP Replay (several times) Bit6 – DLLP Absence Bit5 – Retrain Link (only Dn) Bit4 – Hot Reset (only Dn) Bit3 – Disabled (only Dn) Bit2 – Loopback Bit1 – Rx EI without EIOS Bit0 – Speed Change Note: Bits that can be reset by writing 1	10'h0
0x52C	vesc_reg9[10]	Recovery to Detect Indicates transition from Recovery to Detect happened Note: Bits that can be reset by writing 1	1'b0
0x52C	vesc_reg9[11]	Configuration to Detect Indicates transition from Configuration to Detect happened Note: Bits that can be reset by writing 1	1'b0
0x52C	vesc_reg9[12]	Polling to Detect Indicates transition from Polling to Detect happened Note: Bits that can be reset by writing 1	1'b0
0x52C	vesc_reg9[15:13]	Reserved	1'b0
0x52C	vesc_reg9[20:16]	LTSSM Sub-State Read Only Hardware status of Sub-state of LTSSM state (bits 24:21)	

Offset	Bits	Description	Value
0x52C	vesc_reg9[24:21]	LTSSM State Read Only LTSSM state status 4'h0 – Detect 4'h1 – Polling 4'h2 – Configuration 4'h3 – L0 4'h4 – Recovery 4'h5 – Disable 4'h6 – Loopback 4'h7 – Hot Reset 4'h8 – L0sTx 4'h9 – L0sRx 4'hA – L1 4'hB - L2 4'hC – L0sTxRx 4'hD – Transition state in L0s (wait Tx exit) 4'hE – Transition State in L0s (wit Rx exit) 4'hF – Transition state to Recovery	
0x52C	vesc_reg9[31:25]	Reserved	6'b0
0x52C	vesc_reg9[31:30]	Read Only vesc_reg8 control Four options to control the Hardware indication for vesc_reg8	2'b00

Table 117. VESC_REG 10: (Offset 30h): Custom Reg access (Command Register)

(See TBT Trgister access through PCIE chapter)

Offset	Bits	Description	Value
0x530	vesc_reg10[12:0]	DW Index Sets DW Index Target bus value	13'h0
0x530	vesc_reg10[18:13]	Port Sets Port# Target bus value	6'h0
0x530	vesc_reg10[20:19]	CS Sets CS Target bus value 2'b00 – Path Configuration Space 2'b01 – Port Configuration Space 2'b10 – Device Configuration Space 2'b11 – Counters Configuration Space	2'h0
0x530	vesc_reg10[21]	CMD[0] 1'b0 – Read 1'b1 – Write	1'b0

Offset	Bits	Description	Value
0x530	vesc_reg10[22]	CMD[1] 1'b0: Regular Target bus access 1'b1: Access to CIO Switch registers	1'b0
0x530	vesc_reg10[23]	CMD[2] 1'b0: Regular Target bus access 1'b1: Access to PCIe Switch registers	1'b0
0x530	vesc_reg10[29:24]	Reserved	6'h0
0x530	vesc_reg10[30]	Comand in progress Set by Software to start wr/rd command and cleared by Hardware when command is finished or timeouts	1'b0
0x530	vesc_reg10[31]	Timeout Set by Hardware in case of timeout	1'b0

Table 118. VESC_REG 11: (Offset 34h): Custom Reg access (Write Data Register)

(See TBT rgister access through PCIE chapter)

Offset	Bits	Description	Value
0x534	vesc_reg11[31:0]	Write Data Software puts required data before perfoming wr command	32'h0

Table 119. VESC_REG 12: (Offset 38h): Custom Reg access (Read Data Register)

(See TBT Trgister access through PCIE chapter)

Offset	Bits	Description	Value
0x538	vesc_reg12[31:0]	Read Data Data is loaded by Harware at the end of command	32'h0

Table 120. VESC_REG 13 (Offset 3Ch): Custom LTR register 1

(see Custom LTR Registers Usage chapter)

Offset	Bits	Description	Value
0x53C	vesc_reg13[31:0]	See Custom LTR Registers chapter	32'h0

Table 121. VESC_REG 14 (Offset 40h): Custom LTR register 2

(See Custom LTR Registers Usage chapter)

Offset	Bits	Description	Value
0x540	vesc_reg14[31:0]	See Custom LTR Registers chapter	32'h0

Table 122. VESC_REG 15 (Offset 44h): Custom LTR register 3

(See Custom LTR Registers Usage chapter)

Offset	Bits	Description	Value
0x544	vesc_reg15[31:0]	See Custom LTR Registers chapter	32'h0

Custom PCIE-TBT Mailbox Registers

Table 123. VESC_REG 16 (Offset 48h): Custom Vendor Register 1

Offset	Bits	Description	Value
0x548	vesc_reg16[31:0]	See Custom PCIE-TBT Mailbox Registers chapter	32'h0

Table 124. VESC_REG 17 (Offset 4Ch): Custom Vendor register 2

Offset	Bits	Description	Value
0x54C	vesc_reg17[31:0]	See Custom PCIE-TBT Mailbox Registers chapter	32'h0

Table 125. VESC_REG 18 (Offset 50h): CAB VC0 register

(See Custom CAB Registers Usage chapter)

Offset	Bits	Description	Value
0x550	vesc_reg18[0]	VC0 CAB enable 1'b0: VC0 CAB is disabled 1'b1: VC0 CAB is enabled (This bits is valid only for Dn port)	(Dn) 1'b0
0x550	vesc_reg18[1]	VC0 MemRd Admission Enable 1'b0: VC0 MemRd Admission is disabled 1'b1: VC0 MemRd Admission is enabled	1'b0
0x550	vesc_reg18[2]	Load Threshold value 1'b0: No effect 1'b1: Load MemRd admission threshold for VC0	1'b0
0x550	vesc_reg18[3]	VC0 CAB capable Read Only bit to indicate Downstream Port supports VC0 CAB (This bits is valid only for Dn port)	Up/Ep – 1'b0 Dn – 1'b1
0x550	vesc_reg18[4]	rd_cmpl_same_cycle_fix_dis 1'b0: Port handles the case of Rd and Cmpl at the same cycle. 1'b1: Bug is not fixed	1'b0
0x550	vesc_reg18[5]	check_cab_calculation_en 1'b0: Port doesn't check over/underflow of counters 1'b1: Port checks over/underflow of counters	1'b1
0x550	vesc_reg18[7:6]	Reserved	2'b0
0x550	vesc_reg18[12:8]	VC0 CAB Size Read only field to indicate CAB size in units of 512 Bytes	Up/Ep – 4'h0 Dn - 4'h8
0x550	vesc_reg18[15:12]	Reserved	4'h0
0x550	vesc_reg18[31:16]	VC0 Threshold Threshold value in dwords (32 bits) for VC0	16'h0

Table 126. VESC_REG 19 (Offset 54h): CAB VC1 register

(See Custom CAB Registers Usage chapter)

Offset	Bits	Description	Value
0x554	vesc_reg19[0]	VC1 CAB enable 1'b0: VC1 CAB is disabled 1'b1: VC1 CAB is enabled (This bits is valid only for Dn port)	(Dn) 1'b0/1'b1
0x554	vesc_reg19[1]	VC1 MemRd Admission Enable 1'b0: VC1 MemRd Admission is disabled 1'b1: VC1 MemRd Admission is enabled	1'b0/1'b1
0x554	vesc_reg19[2]	Load Threshold value 1'b0: No effect 1'b1: Load MemRd admisson threshold for VC1	1'b0/1'b1
0x554	vesc_reg19[3]	VC1 CAB capable Read Only bit to indicate Downstream Port supports VC1 CAB (This bits is valid only for Dn port)	Up/Ep – 1'b0 Dn – 1'b1
0x554	vesc_reg19[4]	rd_cmpl_same_cycle_fix_dis 1'b0: Port handles the case of Rd and Cmpl at the same cycle. 1'b1: Bug is not fixed	1'b0
0x554	vesc_reg19[5]	check_cab_calculation_en 1'b0: Port doesn't check over/underflow of counters 1'b1: Port checks over/underflow of counters	1'b1
0x554	vesc_reg19[7:6]	Reserved	2'b0
0x554	vesc_reg19[12:8]	VC1 CAB Size Read only field to indicate CAB size in units of 512 Bytes	Up/Ep – 4'h0 Dn - 4'h8
0x554	vesc_reg19[15:12]	Reserved	4'h0
0x554	vesc_reg19[31:16]	VC1 Threshold Threshold value in dwords (32 bits) for VC1	16'h0

Table 127. VESC_REG 20 (Offset 'h58): Reserved register

Offset	Bits	Description	Value
0x558	vesc_reg20[0]	Reserved	32'h0

Table 128. VESC_REG 21 (Offset 'h5C) - QoS - Load priority & Custom mode register

(See Custom QoS Registers Usage chapter)

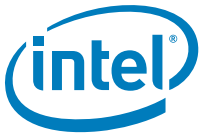
Offset	Bits	Description	Value
0x55C	vesc_reg21[7:0]	Priority value VC arbiter (per transaction type) Used in per transaction type (Post / Non-Post / Cmpl) VC arbiter(Loaded when bit 16 is set)	8'd0
0x55C	vesc_reg21[15:8]	Priority value VC arbitration (over all transaction types) Used in in VC arbiter over all transaction types (Loaded when bit 17 is set)	8'd0

Offset	Bits	Description	Value
0x55C	vesc_reg21[16]	Load priority value VC arbiter (per transaction type) 1'b0: No effect 1'b1: Loads Priority value VC arbiter per transaction type.	1'b0
0x55C	vesc_reg21[17]	Strict priority VC arbiter (per transaction type) 1'b0: No effect 1'b1: Strict Priority in VC arbiter per transaction type (DFT)	1'b0
0x55C	vesc_reg21[18]	Load priority value VC arbitrer (over all type of transactions) 1'b0: No effect 1'b1: Loads Priority value VC arbiter over all transaction type.	1'b0
0x55C	vesc_reg21[19]	Strict priority vc1 VC arbiter (over all type of transactions) 1'b0: No effect 1'b1: Strict Priority in VC arbiter over all transaction type (DFT)	1'b0
0x55C	vesc_reg21[20]	cb_disable_priority_arb 1'b0: 1'b1: Disable priority arbitration over transaction types	1'b0
0x55C	vesc_reg21[21]	cb_disable_lookahead_buffer 1'b0: Look ahead to Rx buffers to keep the VC request channel for VC Arbiter. 1'b1: Disable looking ahead to buffer (Bug)	1'b0
0x55C	vesc_reg21[23:22]	Reserved	2'h0
0x55C	vesc_reg21[24]	Custom VC mode enable 1'b0: No Effect 1'b1: Custom VC mode	1'b0
0x55C	vesc_reg21[25]	VC0 link only enable 1'b0: 1'b1:	1'b0
0x55C	vesc_reg21[26]	Map according to Source TC/VC map 1'b0: Send packet according to TC/VC map of destination. 1'b1: Send packet according to TC/VC map of source.	1'b0
0x55C	vesc_reg21[27]	Enable VC0 CPL push VC0 and VC1 Posted. 1'b0: 1'b1:	1'b0
0x55C	vesc_reg21[28]	Enable VC1 CPL push VC0 and VC1 Posted 1'b0: 1'b1:	1'b0

Table 129. VESC_REG 22 (Offset 'h60) - Shadow port VC Capability and VC Resource Control

(See Custom QoS Registers Usage chapter)

Bits [15:0] are used as shadow for Port VC Capability Register 1.



Bits [31:16] are used as shadow VC Resource Control Register for VC1.

Offset	Bits	Description	Value
0x560	vesc_reg22[2:0]	Extended VC Count Extended VC count to be loaded with value 1	3'h0
0x560	vesc_reg22[3]	Reserved	1'b0
0x560	vesc_reg22[6:4]	Low Priority Extended VC Count Low Priority Extended VC count to be loaded with value 1	3'h0
0x560	vesc_reg22[15:7]	Reserved	9'h0
0x560	vesc_reg22[23:16]	TC/VC1 Map Field to be lowed with TC mapping for VC1	8'h0
0x560	vesc_reg22[26:24]	VC1 ID VC ID to be loaded with value 1	3'h0
0x560	vesc_reg22[30:27]	Reserved	4'h0
0x560	vesc_reg22[31]	VC1 enable 1'b0: No 1'b1: Custom VC1 is enabled	1'b0

Table 130. VESC_REG 23 (Offset 'h64) - TX and Rx TC remapping register

(See Custom QoS Registers Usage chapter)

Offset	Bits	Description	Value
0x564	vesc_reg23[0]	Remap TC Tx Post Map all Tx Posted traffic to TC0	1'b0
0x564	vesc_reg23[1]	Remap TC Tx Non-Post Map all Tx NonPosted traffic to TC0	1'b0
0x564	vesc_reg23[2]	Remap TC Tx Cmpl Map all Tx CPL traffic to TC0	1'b0
0x564	vesc_reg23[3]	Remap TC Tx Msg Map all Tx Msg traffic to TC0	1'b0
0x564	vesc_reg23[4]	Remap one TC Tx Post Map Tx Posted with TC == vesc_reg23 [10:8] to TC0	1'b0
0x564	vesc_reg23[5]	Remap one TC Tx Non-Post Map Tx NonPosted with TC == vesc_reg23 [10:8] to TC0	1'b0
0x564	vesc_reg23[6]	Remap one TC Tx Cmpl Map Tx CPL with TC == vesc_reg23 [10:8] to TC0	1'b0
0x564	vesc_reg23[7]	Remap one TC Tx Msg Map Tx Msg with TC == vesc_reg23 [10:8] to TC0	1'b0
0x564	vesc_reg23[10:8]	TC for Tx Remap TC value with which the TLP TC is to be matched for remapping.	3'h0
0x564	vesc_reg23[15:11]	Reserved	5'h0
0x564	vesc_reg23[16]	Remap TC Rx Post Map Rx Posted to TC 22:20	1'b0
0x564	vesc_reg23[17]	Remap TC Rx Non-Post Map Rx NonPosted to TC 22:20	1'b0

Offset	Bits	Description	Value
0x564	vesc_reg23[18]	Remap TC Rx Cmpl Map Rx CPL to TC 22:20	1'b0
0x564	vesc_reg23[19]	Remap TC Rx Msg Map Rx Msg to TC 22:20	1'b0
0x564	vesc_reg23[22:20]	TC RX Remap Remap to this TC incoming traffic	3'h0
0x564	vesc_reg23[23]	Remap TC Rx Non-Match Post Map Rx Posted when it does not have a match in the bdf table entry to TC 29:27	1'b0
0x564	vesc_reg23[24]	Remap TC Rx Non-Match Non-Post Map Rx NonPosted when it does not have a match in the bdf table entry to TC 29:27	1'b0
0x564	vesc_reg23[25]	Remap TC Rx Non-Match Cmpl Map Rx CPL when it does not have a match in the bdf table entry to TC 29:27	1'b0
0x564	vesc_reg23[26]	Remap TC Rx Non-Match Msg Map Rx Msg when it does not have a match in the bdf table entry to TC 29:27	1'b0
0x564	vesc_reg23[29:27]	Non-Match TC Rx Remap Remap is to this TC when Non Match to bdf entry.	3'h0
0x564	vesc_reg23[30]	Reserved	1'b0
0x564	vesc_reg23[31]	Upstream Traffic RX TC remapping 1'b0: RX TC remapping is done for all RX traffic 1'b1: RX TC remapping is done only for Traffic whose destination is Upstream (This bit valid for Dn and reserved forUp/Dn)	1'b0

Table 131. VESC_REG 24-31 (Offset 'h68 – 'h84) - Rx Remap (Bus:Device:Function) tables.

(See Custom QoS Registers Usage chapter)

Note: vesc_reg24 to vesc_reg31 have the same structure

Offset	Bits	Description	Value
0x5*	vesc_reg*[0]	Post Rx TC Map Map Rx Posted (MemWr) to TC 6:4 if bdf [31:16] matches	1'b0
0x5*	vesc_reg*[1]	NonPost Rx TC Map Map Rx NonPosted to TC 6:4 if bdf [31:16] matches	1'b0
0x5*	vesc_reg*[2]	Cmpl Rx TC Map Map Rx CPL to TC 6:4 if bdf [31:16] matches	1'b0
0x5*	vesc_reg*[3]	Msg Rx TC Map Map Rx Msg to TC 6:4 if bdf [31:16] matches	1'b0
0x5*	vesc_reg*[6:4]	Remap to this TC Remapping will be done to TC specified in this field (0 to 7)	3'h0
0x5*	vesc_reg*[7]	Ignore Function Number Wild Card option to include all functions under same line	1'b0
0x5*	vesc_reg*[15:8]	Reserved	8'h0

Offset	Bits	Description	Value
0x5*	vesc_reg*[31:16]	BDF Bus : 8 bits [31:24] Device : 5 bits [23:19] Function : 3 bits [18:16]	16'h0

Table 132. VESC_REG 32 (Offset 'h88): Custom Port Arbitration registers 1

Offset	Bits	Description	Value
0x588	vesc_reg32[31:0]	Reserved	32'h0

Table 133. VESC_REG 33 (Offset 'h8C): Custom Port Arbitration registers 2

Offset	Bits	Description	Value
0x58C	vesc_reg33[31:0]	Reserved	32'h0

Table 134. VESC_REG 34: (Offset 90h): General configuration register

Offset	Bits	Description	Value
0x590	vesc_reg34[1:0]	cb_eidle_to_eidleset_upbnd_sel Time to wait from Rx EI to EIOS 2'b00 : Upper bound for eidle to eidleset == 7'd40 2'b01 : Upper bound for eidle to eidleset == 7'd20 2'b10 : Upper bound for eidle to eidleset == 7'd60 2'b11 : Upper bound for eidle to eidleset == 7'd80	2'b0
0x590	vesc_reg34[2]	cb_mask_txdata_vld_disable– Default 1'b0 1'b0 : Mask TxDataValid and TxStartBlock during Tx El 1'b1 : Do not mask TxDataValid and TxStartBlock during Tx El	1'b0
0x590	vesc_reg34[4:3]	cb_ctrl_retry_buf_thrshold Considering Retry Buffer available room at Tx channel 2'b00 : Current behavior No blocking of VC0 packets. 2'b01 : Block if Retry Buffer is 3/4 full 2'b10 : Block if Retry Buffer half full 2'b11 : Block if Retry Buffer is 1/4 full	(Dn Port) 2b10
0x590	vesc_reg34[5]	cb_pipedemux_strobe_reset_dis 1'b0 : Reset of PipeDemux address count strobe at De-Skew. 1'b1 : Disable reset of PipeDemux address count strobe.	1'b0

Offset	Bits	Description	Value
0x590	vesc_reg34[6]	cb_gen3_block_dllp 1'b0 : For Dn port doesn't block Init FC DLLP till Equalization completes. For Up/Ep port block Init FC DLLP till good DLLP Pkt is received 1 : For Dn ports (when Upcomp = 1) block Init FC DLLP till Equalization completes. For Up/Ep port doesn't block Init FC DLLP till good DLLP Pkt is received	1'b0
0x590	vesc_reg34[7]	cb_recov_speed_to_detect 1'b0: Recovery.Speed to Detect timeout after 48 ms. 1'b1: No Timeout from Recovery.Speed to Detect (Bug)	1'b0
0x590	vesc_reg34[12:8]	cb_down_port_DevNum (for custom use) Device number that will be used for DownStream Ports (instead of default) if bit 13 is set. (This field is valid for Dn port and reserved for Up/Ep ports)	(Dn) 3'b0
0x590	vesc_reg34[13]	cb_use_down_port_DevNum 1'b0: No effect 1'b1: Use the cb_down_port_DevNum as the device number for Downstream Port. (This bit is valid for Dn port and reserved for Up/Ep ports)	(Dn) 1'b0
0x590	vesc_reg34[14]	cb_disable_tlp_formater 1'b0 : Use new TLP formatter (TLP's are always written to retry buffer in gen3 format and read according to data rate). 1'b1 : Do not use TLP formatter. TLP's are always written to retry buffer in format of the current data rate.	1'b0
0x590	vesc_reg34[15]	cb_disable_anylane_eios 1'b0: Detected EIOS on anylane 1'b1: Detected EIOS on all lanes	1'b0
0x590	vesc_reg34[16]	cb_disable_extra_skip 1'b0: Fix issue of sending Skip from SkipReq during L0 (PHY) 1'b1: SkipReq in PhyLayer tries to sends Skip during L0 (bug)	1'b0
0x590	vesc_reg34[18:17]	cb_en_wteios_config_L1[1:0] X0 : Do not wait for eios before entering L1 01 : Wait for eios before entering L1 11 : Wait for eios for configurable time before entering L1	Up - 2'b11 Dn - 2'b00 Ep - 2'b11
0x590	vesc_reg34[19]	cb_en_wteios_config_L1[2] 1'b0 : Wait 2xTTX-IDLE-MIN for eios before entering L1 1'b1 : Wait 4xTTX-IDLE-MIN for eios before entering L1	1'b1

Offset	Bits	Description	Value
0x590	vesc_reg34[20]	cb_en_wteios_config_L2[0] 1'b0 : Do not wait for eios before entering L2 1'b1 : Wait for eios before entering L2	Up - 1'b1 Dn - 1'b0 Ep - 1b1
0x590	vesc_reg34[21]	cb_en_wteios_config_L2[1] 0 : Wait 2xTTX-IDLE-MIN for eios before entering L2 1 : Wait 4xTTX-IDLE-MIN for eios before entering L2	1'b1
0x590	vesc_reg34[22]	cb_ bypass_equalization 1'b0 : Do not bypass gen3 equalization 1'b1 : Completely Bypass gen3 equalization (DFT - Simulation)	1'b0
0x590	vesc_reg34[25]	cb_bypass_rx_detect 1'b0 :Do not Bypass Rx Detection in DETECT.QUIET_PRE state 1'b1 :Bypass Rx Detection in DETECT.QUIET_PRE state (DFT)	1'b0
0x590	vesc_reg34[26]	cb_bypass_scram_descram 1'b0 : Do not Bypass Scrambler/DeScrambler. 1'b1 : Bypass Scrambler/DeScrambler (DFT)	1'b0
0x590	vesc_reg34[27]	cb_TXStoreForward_enable 1'b0 : Core operates in cut-thru mode (Retry Buffer) 1'b1 : Core operates in Store forward mode	1'b0
0x590	vesc_reg34[28]	cb_ByPassCreditChk 1'b0 :Do not by pass credit check 1'b1 : Bypass credit check (DFT)	1'b0
0x590	vesc_reg34[29]	cb_CoreHasInfCredits 1'b0:Core has finite credits 1'b1: Core has infinite credits (DFT)	1'b0
0x590	vesc_reg34[30]	cb_LBMode_one 1'b0 : No loopback 1'b1 : Tx looped back to Rx within the port (DFT)	1'b0
0x590	vesc_reg34[31]	cb_ForceToCompliance 1'b0 : Port is not forced to compliance 1'b1 : Port is forced to compliance (DFT)	1'b0

Table 135. VESC_REG 35 (Offset 'h94): Custom PTM registers 1

Offset	Bits	Description	Value
0x594	vesc_reg35[31:0]	Not Used	32'h0

Table 136. VESC_REG 36 (Offset 'h98): Custom PTM registers 2

Offset	Bits	Description	Value
0x598	vesc_reg36[31:0]	Not Used	32'h0

Table 137. VESC_REG 37 (Offset 'h9C): Custom PTM registers 3

Offset	Bits	Description	Value
0x59C	vesc_reg37[31:0]	Not Used	32'h0

Table 138. VESC_REG 38 (Offset 'hA0): Custom L2 feature register

(See Custom L2 Register Usage chapter)

Note: This register is valued only at Downstream Port.

Offset	Bits	Description	Value
0x5A0	vesc_reg38[7:0]	PTA timeout Timeout value in half ms for PTA handshake	8'h0
0x5A0	vesc_reg38[15:8]	L2 timeout Timeout value in half ms for L2 handshake	8'h0
0x5A0	vesc_reg38[16]	PTA timeout enable Enable use of timeout value for PTA handshake	8'h0
0x5A0	vesc_reg38[15:8]	L2 timeout enable Enable use of timeout value for L2 handshake	8'h0
0x5A0	vesc_reg38[21:18]	Reserved	4'h0
0x5A0	vesc_reg38[22]	Reserved	1'b0
0x5A0	vesc_reg38[23]	Core in L2 Read only insdication of L2 FSM	1'b0
0x5A0	vesc_reg38[24]	Auto reset disable Disable default partner reset during custom L2	1'b0
0x5A0	vesc_reg38[25]	Static reset Software reset partner (statically from bit)	1'b0
0x5A0	vesc_reg38[26]	Reserved	1'b0
0x5A0	vesc_reg38[27]	Wake finished Status bit that wake ended and Port is in L0	1'b0
0x5A0	vesc_reg38[28]	Wake Wake trigger from custom L2	1'b0
0x5A0	vesc_reg38[29]	Handshake completed (timeout) Status bit that the handshake is completed after timeout	1'b0
0x5A0	vesc_reg38[30]	Handshake completed Status bit that the handshake is completed	1'b0
0x5A0	vesc_reg38[31]	Custom L2 trigger Trigger custom Turnoff/L2 in Downstream	1'b0

Table 139. VESC_REG 39 (Offset 'hA4): Custom Compliance Pattern register 1

(See Custom Compliance Pattern Registers Usage chapter)

Offset	Bits	Description	Value
0x5A4	vesc_reg39[3:0]	K-char value Used to force K-Char in Gen1/2 Pattern along with register 40	4'h0

Offset	Bits	Description	Value
0x5A4	vesc_reg39[9:4]	FSM state Used with bit 30 or bit 29 to force required state Values are from 6'd0 to 6'd34	6'b0
0x5A4	vesc_reg39[10]	Disable Load Board Compliance Entry 1'b0: No effect 1'b1: Prevents from Port to enter Polling.Compliance due to Rx Electrical Idle signal being high	1'b0
0x5A4	vesc_reg39[11]	Reserved	1'b0
0x5A4	vesc_reg39[12]	LFSR advance disable output Don’t Advance LFSR output value (valid if bit 26 is set)	1'b0
0x5A4	vesc_reg39[13]	Scrambler reset output Reset Scrambler output value (valid if bit 26 is set)	
0x5A4	vesc_reg39[14]	Drive Compliance output Drive Compliance output value (valid if bit 26 is set)	1'b0
0x5A4	vesc_reg39[15]	Exit Compliance output Exit Compliance output value (valid if bit 26 is set)	1'b0
0x5A4	vesc_reg39[16]	Rx EI input Rx Electrical Idle input value (valid if bit 27)	1'b0
0x5A4	vesc_reg39[17]	Compliance entry method input Compliance entry method (valid if bit 27 and 25 are set)	1'b0
0x5A4	vesc_reg39[18]	Send Compliance input Send Compliance input value (valid if bit 27 is set)	1'b0
0x5A4	vesc_reg39[19]	Modified Compliance input Modified Compliance input value (valid if bit 27 is set)	1'b0
0x5A4	vesc_reg39[20]	Custom value lane 0 enable 1'b0: No effect 1'b1: Enable to force the custom pattern on lane 0	1'b0
0x5A4	vesc_reg39[21]	Custom value lane 1 enable 1'b0: No effect 1'b1: Enable to force the custom pattern on lane 1	1'b0
0x5A4	vesc_reg39[22]	Custom value lane 2 enable 1'b0: No effect 1'b1: Enable to force the custom pattern on lane 2	1'b0
0x5A4	vesc_reg39[23]	Custom value lane 3 enable 1'b0: No effect 1'b1: Enable to force the custom pattern on lane 3	1'b0
0x5A4	vesc_reg39[24]	Compliance Entry Method enable 1'b0: No effect 1'b1: Enables to force Compliance Entry Method	1'b0
0x5A4	vesc_reg39[25]	Overwrite FSM ouputs from FSM 1'b0: No effect 1'b1: Enables to force several control outputs of FSM	1'b0

Offset	Bits	Description	Value
0x5A4	vesc_reg39[26]	Overwrite FSM Inputs to FSM 1'b0: No effect 1'b1: Enables to force several control inputs of FSM	1'b0
0x5A4	vesc_reg39[27]	Jump to Gen3 specific sate enable 1'b0: No effect 1'b1: Enables to jump states in order to repeat 4 consecutive states for full Gen3 block (bits 9:4)	1'b0
0x5A4	vesc_reg39[28]	Stop Compliance FSM at specific sate enable 1'b0: No effect 1'b1: Indicates to stop at specific state of FSM (bits 9:4)	1'b0
0x5A4	vesc_reg39[29]	Force Compliance FSM specific state enable 1'b0: No effect 1'b1: Forces specific state of FSM (bits 9:4)	1'b0
0x5A4	vesc_reg39[30]	Custom Pattern from Register Enable 1'b0: No effect 1'b1: Enables to force custom pattern from register instead of regular compliance pattern.	1'b0
0x5A4	vesc_reg39[31]	Custom Compliance Enable 1'b0: No effect 1'b1: Master Bit that enables to use other bits and register 40 to force custom pattern or perform several manipulation to Compliance FSM.	1'b0

Table 140. VESC_REG 40 (Offset 'hA8): Custom Compliance Pattern register 2

Offset	Bits	Description	Value
0x5A8	vesc_reg40[31:0]	Data from Register Constant 4 symbols that will be forced on PIPE for custom Compliance Pattern (when bits 31 and 30 are set)	32'h0

Table 141. VESC_REG 41: (Offset ACh): General configuration register

Offset	Bits	Description	Value
0x5AC	vesc_reg41[0]	cb_gen3_valid_flag_sel 1'b0 : RxDataValid de-assertion is per lane 1'b1 : RxDataValid de-assertion is common	1'b0
0x5AC	vesc_reg41[1]	cb_detetect_rxei_exit_by_eieos_gen2_dis 1'b0 : Rx EI exit in Gen2 by EIEOS 1'b1 : Rx EI exit in Gen2 by Rx EI signal	1'b0
0x5AC	vesc_reg41[2]	cb_detetect_rxei_exit_by_eieos_gen3_dis 1'b0 : Rx EI exit in Gen3 by EIEOS 1'b1 : Rx EI exit in Gen3 by Rx EI signal	1'b0
0x5AC	vesc_reg41[3]	cb_any_lane_rx_ei_exit_det_sel 1'b0 : no effect 1'b1 : Any Lane RxEI is done by EIEOS and by Rx EI signal	1'b1

Offset	Bits	Description	Value
0x5AC	vesc_reg41[4]	cb_all_lane_rx_ei_exit_det_sel 1'b0 : no effect 1'b1 : All Lane RxEI is done by EIEOS and by Rx EI signal	1'b0
0x5AC	vesc_reg41[5]	cb_disable_frmerr_data_sds 1'b0: When recovering from framing error receiver stops processing data until SDS is received 1'b1: When recovering from framing error receiver does not stop processing data until SDS is received	1'b0
0x5AC	vesc_reg41[6]	cb_rxvalid_deassert_disable 1'b0: No effect 1'b1: RxValid de-assertion of PIPDemux is delayed for 1 cycle	1'b0
0x5AC	vesc_reg41[7]	cb_gen2_eieos_detect_cut_dis 1'b0 : Detects Gen2 EIEOS even without first two Bytes 1'b1 : Detects Gen2 EIEOS only if first two Bytes exist	1'b0
0x5AC	vesc_reg41[8]	cb_gen2_eieos_detect_shift_dis 1'b0 : Detects Gen2 EIEOS even if shifted by 2 Bytes. 1'b1 : Detects Gen2 EIEOS only if it is aligned correctly.	1'b0
0x5AC	vesc_reg41[9]	cb_easy_gen2_eieos_detection 1'b0 : no effect 1'b1 : Enables to Detects Gen2 EIEOS without last 8 bytes.	1'b1
0x5AC	vesc_reg41[10]	cb_easy_gen3_eieos_detection 1'b0 : no effect 1'b1 : Enables to Detects Gen3 EIEOS without last 4 bytes.	1'b0
0x5AC	vesc_reg41[11]	cb_rst_eieos_flag_in_recov_speed_dis 1'b0 : EIEOS flag is reset during entry to Recovery.Speed 1'b1 :Fix of EIEOS flag reset is disabled	1'b0
0x5AC	vesc_reg41[12]	cb_no_first_chanbond_dis 1'b0 : First Channel Bonding pulse is disabled (pulse is masked in order not to ruin first EIEOS) 1'b1 : First Channel Bonding pulse is enabled	1'b0
0x5AC	vesc_reg41[13]	cb_gen2_eios_detect_2nd_byte_dis 1'b0 : Gen2 EIOS is detected by only first 3 bytes (Spec) 1'b1 : Gen2 EIOS is detected by only first 2 bytes	1'b0
0x5AC	vesc_reg41[14]	cb_gen2_eios_detect_3rd_byte_en 1'b0 : Gen2 EIOS is detected without last byte (Spec) 1'b1 : Gen2 EIOS is detected by all 4 bytes	1'b0
0x5AC	vesc_reg41[15]	cb_ignore_rx_data_in_ei_en (not used)	1'b0
0x5AC	vesc_reg41[16]	cb_clr_dat_strm_valid_with_rx_ei 1'b0 :no effect 1'b1 : Enable to clear Data Stream Valid in Rx EI	1'b1

Offset	Bits	Description	Value
0x5AC	vesc_reg41[17]	cb_lnrev_rx_ei_early 1’b0 : no effect 1’b1 : Selects Rx EI one cycle earlier	1'b0
0x5AC	vesc_reg41[18]	cb_blk_align_deassertion_dis 1’b0 : Block Align is 1 when Data Stream is no valid 1’b1 : Force Block Align control signal high	1'b0
0x5AC	vesc_reg41[19]	cb_adv_less_nph_credits 1’b0 : No Action 1’b1 : Advertise less Non-Post Header credits	1'b0
0x5AC	vesc_reg41[22:20]	cb_adv_less_nph_value 1’b0 : No effect 1’b1 : Less credits in steps of 4 (0 - 4, 1- 8, … 7 - 28)	3'b0
0x5AC	vesc_reg41[23]	cb_adv_less_ph_credits 1’b0 : No Action 1’b1 : Advertise one credit less for Post Header	1'b0
0x5AC	vesc_reg41[24]	cb_adv_less_pd_credits 1’b0 : No Action 1’b1 : Advertise 1 credits less for Post Data	1'b0
0x5AC	vesc_reg41[25]	cb_adv_less_cplh_credits 1’b0 : No Action 1’b1 : Advertise one credit less for Cmpl Header	1'b0
0x5AC	vesc_reg41[26]	cb_adv_less_cpld_credits 1’b0 : No Action 1’b1 : Advertise 1 credit less for Cmpl Data	1'b0
0x5AC	vesc_reg41[27]	cb_dllp_seq_burst_dis 1’b0 : Back to Back DLLP can be sent 1’b1 : Disables the option to send back to back DLLP	1'b0
0x5AC	vesc_reg41[28]	cb_dlssm_arb_fast_ack_grant_dis 1’b0 : Early Grant ACK for BW improvement 1’b1 : Early Grant ACK is disabled	1'b0
0x5AC	vesc_reg41[29]	cb_dlssm_arb_fast_fc_grant_dis 1’b0 : Early Grant FC for BW improvement 1’b1 : Early Grant FC is disabled	1'b0
0x5AC	vesc_reg41[30]	cb_dlssm_arb_fast_tlp_grant_dis 1’b0 : Early Grant TLP for BW improvement 1’b1 : Early Grant TLP is disabled	1'b0

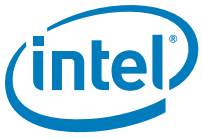
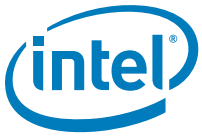


Table 142. VESC_REG 42: (Offset B0h): General configuration register

Offset	Bits	Description	Value
0x5B0	vesc_reg42[0]	cb_det_pwr_down_delay_en 1'b0 : no effect 1'b1 : delay Power Down in Detect, relatively to Tx EI	1'b0
0x5B0	vesc_reg42[1]	cb_dis_pwr_down_delay_en 1'b0: no effect 1'b1: Delay Power Down in Disabled, relatively to Tx EI	1'b0
0x5B0	vesc_reg42[2]	cb_combine_phy_status_static 1'b0: no effect 1'b1: PhyStatus de-assertion combined according to xmode	1'b0
0x5B0	vesc_reg42[4:3]	cb_sel_time_from_rst_to_rx_detect Select timer value after Reset till Rx Detection 2'b00 : 1ms 2'b01 : 5ms 2'b10 : 13ms 2'b11 : 15ms	2'b00
0x5B0	vesc_reg42[6:5]	cb_sel_time_in_detect_quite Select timer value in Detect Quite 0 : 13ms 1 : 11ms 2 : 12ms 3 : 14ms	2'b00
0x5B0	vesc_reg42[7]	cb_disable_snd_eios 1'b0 : Port sends EIOS before asserting Tx EI while reducing xmode to x1 in Configuration.LaneNumAccept 1'b1 : Port doesn't send EIOS before asserting Tx EI while reducing xmode to x1 in Configuration.LaneNumAccept	1'b0
0x5B0	vesc_reg42[8]	cb_eidle_inferred_recov_disable 1'b0 : Infer EI is checked in Recovery.Speed entry 1'b1 : Infer EI isn't checked in Recovery.Speed entry	1'b0
0x5B0	vesc_reg42[9]	cb_idle_before_sds_fix_dis 1'b0 – Fix to prolong last TS to prevent Logical Idle before Transmission of SDS 1'b1 – Disable the fix of Logical Idle before SDS	1'b0
0x5B0	vesc_reg42[10]	cb_l0stx_fsm_rst_in_recov_dis 1'b0 – Entry to Recovery Reset L0sTx FSM 1'b1 – Disable the L0sTx FSM reset	1'b0
0x5B0	vesc_reg42[11]	cb_l1aspm_fsm_rst_in_recov_dis 1'b0 – Entry to Recovery Reset L1 ASPM FSM 1'b1 – Disable the L1 ASPM FSM reset	1'b0

Offset	Bits	Description	Value
0x5B0	vesc_reg42[12]	cb_l1soft_fsm_rst_in_recov_dis 1’b0 – Entry to Recovery Reset L1 Soft FSM 1’b1 – Disable the L1 Soft FSM reset	1'b0
0x5B0	vesc_reg42[13]	cb_backdoor_d0_l1_exit_dis 1’b0 – Exit L1Soft when Port exits non D0 state (Host i/f) 1’b1 – Exit from non D0 state (Host i/f) doesn’t effect L1	1'b0
0x5B0	vesc_reg42[14]	cb_ei_time_during_rate_change_sel Selects the time to be in Tx EI 1’b0 – 8us 1’b1 – 60us	1'b0
0x5B0	vesc_reg42[15]	cb_exit_elec_idle_for_l0s_idle_sel 1’b0 – L0sRx exit upon any lane exit from Rx EI 1’b1 – L0sRx exit upon all lane exit from Rx EI	1'b0
0x5B0	vesc_reg42[16]	cb_exit_elec_idle_for_l1_idle_sel 1’b0 – L1 exit upon any lane exit from Rx EI 1’b1 – L1 exit upon all lane exit from Rx EI	1'b0
0x5B0	vesc_reg42[17]	cb_send_one_eios_in_poll_comp 1'b0: No Effect 1'b1: In cases of 2 EIOS disables the second EIOS	1'b0
0x5B0	vesc_reg42[18]	cb_bond_rx_valid_fix_dis 1’b0 – RxDataValid is delayed with same delay of Rx Data. 1’b1 – RxDataValid delay is fixed.	1'b0
0x5B0	vesc_reg42[20:19]	cb_l0s_entry_time_sel Select the time to wait during L0s entry (in PCLK div2) 2’b00 – 12 cycles 2’b01 – 24 cycles 2’b10 – 36 cycles 2’b11 – 48 cycles	2’b00
0x5B0	vesc_reg42[21]	cb_lcrc_gap_fix_dis 1’b0: Fix the issue of LCRC calculation when TxDataValid is throttled. 1'b1: Issue of LCRC calculation when TxDataValid is throttled is not fixed.	1'b0
0x5B0	vesc_reg42[22]	cb_fast_grant_ext_dis 1’b0 : Grant for external channels is returned immediately 1’b1 : Grant for external channels is delayed for one cycle	1'b0
0x5B0	vesc_reg42[23]	cb_fast_grant_int_dis 1’b0 : Grant for internal channels is returned immediately 1’b1 : Grant for internal channels is delayed for one cycle	1'b0



Offset	Bits	Description	Value
0x5B0	vesc_reg42[24]	cb_early_vc_sel_forreq_ext_dis 1'b0 : VC select for external channels comes earlier 1'b1 : VC select for external channels comes later	1'b0
0x5B0	vesc_reg42[25]	cb_early_vc_sel_forreq_int_dis 1'b0 : VC select for internal channels comes earlier 1'b1 : VC select for internal channels comes later	1'b0
0x5B0	vesc_reg42[26]	cb_return_ur_in_non_d0_state_en 1'b0 : no effect 1'b0 : When Port in non D0 UR is returned upon MemRd	1'b1
0x5B0	vesc_reg42[27]	cb_vdm_type1_fc_sel - (in EMEP) 1'b0 : Port doesn't returns FC on VDM type 1 (from User) 1'b1 : Port returns FC on VDM type 1	Up/Dn – 1'b0 EMEP - 1'b1
0x5B0	vesc_reg42[28]	cb_vdm_type0_fc_sel -(in EMEP) 1'b0 : Port doesn't returns FC on VDM type 0 (from User) 1'b1 : Port returns FC on VDM type 0	1'b0
0x5B0	vesc_reg42[29]	cb_dis_invld_tlp_lenchk 1'b0: Port checks TLP length and Parity. Assert a framing error if check does not pass. 1'b1 : Port doesn't check TLP length and Parity.	1'b0
0x5B0	vesc_reg42[30]	cb_gen2_early_rx_valid_dis 1'b0 : RxValid is asserted one cycle earlier in PIPEDemux in order not to miss first Gen2 EIEOS 1'b1 : Issue is not fixed (first EIEOS is missed)	1'b0
0x5B0	vesc_reg42[31]	cb_gen3_early_rx_valid_dis 1'b0 : RxValid is asserted one cycle earlier in PIPEDemux in order not to miss first Gen3 EIEOS 1'b1 : Issue is not fixed (first EIEOS is missed)	1'b0

Table 143. VESC_REG 43: (Offset B4h): General configuration register

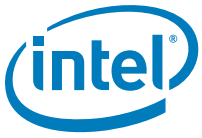
Offset	Bits	Description	Value
0x5B4	vesc_reg43[3:0]	cb_preset_to_use_ln0 Value of the preset to use during the master phase on lane0 (Valid values are 0 to A)	4'h0
0x5B4	vesc_reg43[7:4]	cb_preset_to_use_ln1: Value of the preset to use during the master phase on lane1 (Valid values are 0 to A)	4'h0
0x5B4	vesc_reg43[11:8]	cb_preset_to_use_ln2 Value of the preset to use during the master phase on lane2 (Valid values are 0 to A)	4'h0
0x5B4	vesc_reg43[15:12]	cb_preset_to_use_ln3 Value of the preset to use during the master phase on lane3 (Valid values are 0 to A)	4'h0

Offset	Bits	Description	Value
0x5B4	vesc_reg43[19:16]	cb_preset_to_request Value of the preset to request during the master phase (Valid values are 0 to A)	4'h0
0x5B4	vesc_reg43[20]	cb_drive_master_preset_fix_dis 1'b0 : During Master Phase asks specific preset (from reg) 1'b1 : Captures values on Rx and aks the same values	1'b0
0x5B4	vesc_reg43[21]	cb_force_constant_preset 1'b0 : no effect 1'b1 : Option to force on PIPE preset values from register (Value is taken from bits [19:16])	1'b0
0x5B4	vesc_reg43[22]	cb_eq_use_rx_preset_dis 1'b0 : Port reacts on "Use Preset" from Partner 1'b1 : Port ignores "Use Preset" from Partner	1'b0
0x5B4	vesc_reg43[23]	cb_check_valid_rx_preset_dis 1'b0 : Port checks if Rx Preset is valid 1'b1 : Port doesn't check if Rx Preset is valid	1'b0
0x5B4	vesc_reg43[24]	cb_only_one_good_eq 1'b0 : no effect 1'b1 : Only one Equalization Evaluation	1'b0
0x5B4	vesc_reg43[25]	cb_reverse_coff_order 1'b0 : Coeff order according to Spec 1'b1 : Reverse the order for custom use (bug)	1'b0
0x5B4	vesc_reg43[26]	cb_optimal_setting_reached_sel 1'b0 : "optimal" condition based on "coff tmp" parameters 1'b1 : "optimal" condition based on "coff" parameters	1'b0
0x5B4	vesc_reg43[27]	cb_force_optimal_setiing_reached 1'b0 : no effect 1'b1 : DFT option to force "optimal" condition	1'b0
0x5B4	vesc_reg43[28]	cb_force_all_checks_satisfied 1'b0 : no effect 1'b1 : DFT option to force "coeff check" condition	1'b0
0x5B4	vesc_reg43[29]	cb_toggle_invalid_request_dis 1'b0 : no effect 1'b1 : DFT option to disabled toggle of invalid request	1'b0
0x5B4	vesc_reg43[30]	cb_bypass_master_phase 1'b0 : Do not Bypass the master phase of Equalization 1'b1 : Bypass the master phase of Equalization.	1'b0
0x5B4	vesc_reg43[31]	cb_usepreset_on_rjct_coeff 1'b0: Assert Use preset when coefficients are rejected. 1'b1: Do not assert Use preset when coefficients are rejected.	1'b0

Table 144. VESC_REG 44: (Offset B8h): General configuration register

Offset	Bits	Description	Value
0x5B8	vesc_reg44[0]	cb_slave_capture_value_sel 1’b0 : During Slave phase checking Stored parameters 1’b1 : During Slave phase checking Rx parameters	1'b0
0x5B8	vesc_reg44[1]	cb_another_try_after_reject 1’b0 : Port finish Master Phase in case of reject. 1’b1 : Port tries different Preset/Coeff in case of reject.	1'b1
0x5B8	vesc_reg44[2]	cb_finish_after_reject_sel 1’b0 : In case of reject Equalization fails 1’b1 : In case of reject Port goes to next step	1'b1
0x5B8	vesc_reg44[3]	cb_slave_capture_value_fix_dis 1’b0 : In Slave mode returns the values from FSM parameters (sync with FSM updates) 1’b1 : In Slave mode returns the values directly from previously capture values from TS	1'b0
0x5B8	vesc_reg44[5:4]	cb_eq_counter_value_sel Select counter value during Equalization Master Phase 2'b00 600ns 2'b01 700ns 2'b10 800ns 2'b11 1us	2'b00
0x5B8	vesc_reg44[7:6]	cb_num_of_good_rx_eval_sel Selects number good Rx Evalueation 2'b00 : 2 2'b01 : 4 2'b10 : 6 2'b11 : 8	2'b01
0x5B8	vesc_reg44[9:8]	cb_num_of_bad_rx_eval_sel 2’d0 : 64 2’d1 : 128 2’d2 : 196 2’d3 : 255	2'b00
0x5B8	vesc_reg44[13:10]	cb_reserved_eco Reserved extra bits for ECO	4'h0
0x5B8	vesc_reg44[14]	cb_gen1_tx_ei_later_rise 1’b0 : no effect 1’b1 : Tx EI assertion happens one cycle later (in Gen1)	1'b0
0x5B8	vesc_reg44[15]	cb_gen2_tx_ei_later_rise 1’b0 : no effect 1’b1 : Tx EI assertion happens one cycle later (in Gen2)	1'b0

Offset	Bits	Description	Value
0x5B8	vesc_reg44[16]	cb_gen3_tx_ei_later_rise 1'b0 : no effect 1'b1 : Tx EI assertion happens one cycle later (in Gen3)	1'b0
0x5B8	vesc_reg44[17]	cb_gen1_tx_ei_later_fall 1'b0 : no effect 1'b1 : Tx EI de-assertion happens one cycle later (in Gen1)	1'b0
0x5B8	vesc_reg44[18]	cb_gen2_tx_ei_later_fall 1'b0 : no effect 1'b1 : Tx EI de-assertion happens one cycle later (in Gen2)	1'b0
0x5B8	vesc_reg44[19]	cb_gen3_tx_ei_later_fall 1'b0 : no effect 1'b1 : Tx EI de-assertion happens one cycle later (in Gen3)	1'b0
0x5B8	vesc_reg44[20]	cb_tx_elec_idle_delay_sel Fix to prevent SyncHdr of during TxEI entry or exit Selects the Tx EI that wil be used to force SynHdr to 2'b01 1'b0 : Tx EI in PHYTX uses early version 1'b1 : Tx EI in PHYTX uses late version	1'b0
0x5B8	vesc_reg44[21]	cb_sync_hdr_tx_ei_sel Selects the Tx EI that wil be used to force SynHdr to 2'b01 1'b0 : Uses long version (early assertion / later de-assertion) 1'b1 : one version is used (controlled by previous bit)	1'b0
0x5B8	vesc_reg44[22]	cb_gen3_tx_data_valid_gap_fix_dis 1'b0 : Fix to hold Tx Data Valid after Tx EI de-assertion. 1'b1 : Tx Data Valid is de-asserted after Tx EI de-assertion.	1'b0
0x5B8	vesc_reg44[23]	cb_recov_speed_all_ei_det_fix_en 1'b0 : Rx EI is done either by EIOS + infer or by Rx signal. 1'b1 : Rx EI is done by all three means.	1'b1
0x5B8	vesc_reg44[24]	cb_later_eios_done_en 1'b0 : no effect 1'b1 : Enables one cycle delay on EIOS sent indication	1'b0
0x5B8	vesc_reg44[25]	cb_poll_eios_send_fix_dis 1'b0 : Fix to change speed only after EIOS was sent 1'b1 : Disable the fix (This bit should be set for Compliance testing)	1'b0
0x5B8	vesc_reg44[26]	cb_capture_gen3_value_fix 1'b0 : Capture Gen3 value if ConsecTS >= 2 1'b1 : Capture Gen3 value if ConsecTS = 2	1'b0
0x5B8	vesc_reg44[27]	cb_exit_elec_idle_for_infer_idle_sel 1'b0 –Exit from Rx EI for EI infer FSM based on all lanes 1'b1 – Exit from Rx EI for EI infer FSM based on any lanes	1'b0

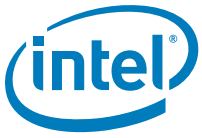


Offset	Bits	Description	Value
0x5B8	vesc_reg44[28]	cb_poll_active_continue_to_detect_ts 1'b0 : no effect 1'b1 : Continue to detect TS during Polling Active	1'b1
0x5B8	vesc_reg44[29]	cb_cfg_start_continue_to_detect_ts 1'b0 : no effect 1'b1 : Continue to detect TS during Configuration Start	1'b1
0x5B8	vesc_reg44[30]	cb_cfg_complete_continue_to_detect_ts 1'b0 : no effect 1'b1 : Continue to detect TS during Configuration Complete	1'b0
0x5B8	vesc_reg44[31]	cb_eidle_recov_enable 1'b0 : no effect 1'b1 : Enable Rx EI indication according to PIPE signal for Recovery FSM	1'b0

Table 145. VESC_REG 45: (Offset BCh): General configuration register

Offset	Bits	Description	Value
Offset	Bits	Description	Value
0x5BC	vesc_reg45[0]	cb_xmode_delay_dis 1'b0: Internal xmode indication is delayed for one cycle 1'b1: Fix of delaying internal xmode indication is disabled	1'b0
0x5BC	vesc_reg45[1]	cb_mask_frame_err_detected 1'b0: No effect 1'b1: Option to mask Frame Error detection (DFT)	1'b0
0x5BC	vesc_reg45[2]	cb_mask_frame_err_tlp 1'b0: No effect 1'b1: Option to mask Frame Error TLP detection (DFT)	1'b0
0x5BC	vesc_reg45[3]	cb_disable_tlp_len_err_x1mode 1'b0: No effect 1'b1: Option to mask TLP length error detection in x1 (DFT)	1'b0
0x5BC	vesc_reg45[4]	cb_disable_tlp_len_err_x2mode 1'b0: No effect 1'b1: Option to mask TLP length error detection in x2 (DFT)	1'b0
0x5BC	vesc_reg45[5]	cb_disable_tlp_len_err_x4mode 1'b0: No effect 1'b1: Option to mask TLP length error detection in x4 (DFT)	1'b0
0x5BC	vesc_reg45[6]	cb_disable_frame_err_x1mode 1'b0: No effect 1'b1: Option to mask Frame Error detection in x1 (DFT)	1'b0
0x5BC	vesc_reg45[7]	cb_disable_frame_err_x2mode 1'b0: No effect 1'b1: Option to mask Frame Error detection in x2 (DFT)	1'b0

Offset	Bits	Description	Value
0x5BC	vesc_reg45[8]	cb_disable_frame_err_x4mode 1'b0: No effect 1'b1: Option to mask Frame Error detection in x4 (DFT)	1'b0
0x5BC	vesc_reg45[9]	cb_stp_align_dllp_detect_x1_dis 1'b0: Fix to ignore DLLP it STP Alignment block in order not to indicate false Framing Errors in x1 mode 1'b1: Fix is disabled	1'b0
0x5BC	vesc_reg45[10]	cb_stp_align_dllp_detect_x2_dis 1'b0: Fix to ignore DLLP it STP Alignment block in order not to indicate false Framing Errors in x2 mode 1'b1: Fix is disabled	1'b0
0x5BC	vesc_reg45[11]	cb_stp_align_dllp_detect_x4_dis 1'b0: Fix to ignore DLLP it STP Alignment block in order not to indicate false Framing Errors in x4 mode 1'b1: Fix is disabled	1'b0
0x5BC	vesc_reg45[12]	cb_cfg_frame_err_dis 1'b0: No Effect 1'b1: Disable Frame Error detection in Configuration (DFT)	1'b0
0x5BC	vesc_reg45[13]	cb_recov_frame_err_dis 1'b0: No Effect 1'b1: Disable Frame Error detection in Recovery (DFT)	1'b0
0x5BC	vesc_reg45[14]	cb_gen3_count_sync_fix_en 1'b0: No Effect 1'b1: Part of bad fix trial of sync TxDataValid and TxEI (vesc_reg46[22] is the correct fix)	1'b0
0x5BC	vesc_reg45[15]	cb_gen3_count_sync_early_en 1'b0: No Effect 1'b1: Part of bad fix trial of sync TxDataValid and TxEI (vesc_reg46[22] is the correct fix)	1'b0
0x5BC	vesc_reg45[16]	cb_move_to_rcvr_cfg_fix_dis 1'b0: Fix to move from Recovery.Lock to Recovery.Cfg only when detected exit from Rx EI 1'b1: Transition from Recovery.Lock to Recovery.Cfg ignores exit from Rx EI	1'b0
0x5BC	vesc_reg45[17]	cb_late_eios_fix_dis 1'b0: Fix to send EIOS one cycle earlier in Configuration state 1'b1: EIOS is sent one cycle later in Configuration state	1'b0
0x5BC	vesc_reg45[18]	cb_delay_upcomp0_ph2_dis 1'b0: Fix to delay Phase 2 to meet correct transition 1'b1: Transition happens earlier and some TS data is wrong (This bit is valid in Up/Ep ports and reserved in Dn port)	(Up/Ep) 1'b0



Offset	Bits	Description	Value
0x5BC	vesc_reg45[19]	cb_delay_upcomp1_ph3_dis 1'b0: Fix to delay Phase 3 to meet correct transition 1'b1: Transition happens earlier and some TS data is wrong (This bit is valid in Dn ports and reserved in Up/Ep port)	(Dn) 1'b0
0x5BC	vesc_reg45[20]	cb_sync_hdr_mux_del_delay_en 1'b0: No effect 1'b1: Fix to delay one cycle the value of 2'b01 of SyncHdr	1'b0
0x5BC	vesc_reg45[21]	cb_sync_hdr_early_tx_ei_fix_en 1'b0: No effect 1'b1: Internal sync hdr signal changes one earlier (Bad fix)	1'b0
0x5BC	vesc_reg45[22]	cb_dynamic_coeff_calc_en 1'b0: Coefficient are taken according to Preset form LUT 1'b1: Option to calculate the coefficient dynamically	1'b0
0x5BC	vesc_reg45[23]	cb_upcomp0_ec11_delay_fix_dis 1'b0: Fix to delay EC = 2'b11 to meet correct transition timing 1'b1: Issue where EC turns to value 2'b11 to early	1'b0
0x5BC	vesc_reg45[24]	cb_last_rd_ptr_durig_replay_fix_dis 1'b0: Fix to load correct pointer for Replay 1'b1: Issue with loading bad pointer during Replay	1'b0
0x5BC	vesc_reg45[25]	cb_check_fcrc_min_len_fix_dis 1'b0: Ignore not valid length for FCRC calculation (below min) 1'b1: FCRC Calculation checks any length TLP	1'b0
0x5BC	vesc_reg45[26]	cb_check_fcrc_max_len_fix_dis 1'b0: Ignore not valid length for FCRC calculation (above max) 1'b1: FCRC Calculation checks any length TLP	1'b0
0x5BC	vesc_reg45[27]	cb_ignore_phy_errors_en 1'b0: No Effect 1'b1: Option to ignore PHY related errors for Advanced Error Reporting status bits (DFT)	1'b0
0x5BC	vesc_reg45[28]	cb_ignore_tlp_errors 1'b0: No Effect 1'b1: Option to ignore TLP related errors for Advanced Error Reporting status bits (DFT)	1'b0
0x5BC	vesc_reg45[29]	cb_ignore_dllp_errors 1'b0: No Effect 1'b1: Option to ignore DLLP related errors for Advanced Error Reporting status bits (DFT)	1'b0
0x5BC	vesc_reg45[30]	cb_ignore_replay_errors 1'b0: No Effect 1'b1: Option to ignore Replay related errors for Advanced Error Reporting status bits (DFT)	1'b0

Offset	Bits	Description	Value
0x5BC	vesc_reg45[31]	cb_ignore_ur_errors 1'b0: No Effect 1'b1: Option to ignore UR related errors for Advanced Error Reporting status bits (DFT)	1'b0

Table 146. VESC_REG 46: (Offset C0h): General configuration register

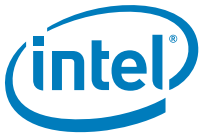
Offset	Bits	Description	Value
0x5C0	vesc_reg46[0]	cb_force_fs_from_reg (Gen3) 1'b0: Local FS value is taken from PHY 1'b1: Local FS value is taken from bits 7:2 (DFT)	1'b0
0x5C0	vesc_reg46[1]	cb_force_lf_from_reg (Gen3) 1'b0: Local LF value is taken from PHY 1'b1: Local LF value is taken from bits 13:8 (DFT)	1'b0
0x5C0	vesc_reg46[7:2]	cb_local_fs_from_reg (Gen3) Local FS value to take instead of PHY value This value is used if bit 0 is set	5'h0
0x5C0	vesc_reg46[13:8]	cb_local_lf_from_reg (Gen3) Local LF value to take instead of PHY value This value is used if bit 1 is set	5'h0
0x5C0	vesc_reg46[14]	cb_mask_start_block_after_ei_en (Gen3) 1'b0: No effect 1'b1: Internally mask start block signals during Tx EI	1'b0
0x5C0	vesc_reg46[15]	cb_mask_data_sync_hdr_after_ei_dis (Gen3) 1'b0: Internally force sync header signals during Tx EI to 2'b01 1'b1: Sync Header is driven to 2'b10 during Tx EI (bug)	1'b0
0x5C0	vesc_reg46[16]	cb_l0s_rx_entry_upon_rx_ei 1'b0: EI detection for entry to L0sRx upon EIOS on any lane. 1'b1: EI detection for entry to L0sRx upon Rx EI on all lanes.	1'b0
0x5C0	vesc_reg45[17]	cb_early_skip_det_fix_dis 1'b0: Fix of issue in L0sRx where SKIP detection is too early. 1'b1: Disable the fix of too early SKIP detection in L0sRx.	1'b0
0x5C0	vesc_reg46[18]	cb_l0s_skip_detect_fix_dis 1'b0: Fix to save the indication of received Skip in L0sRx 1'b1: Disable the fix of Skip detection flag.	1'b0
0x5C0	vesc_reg46[19]	cb_early_sds_det_fix_dis (Gen3) 1'b0: Fix of issue in L0sRx where SDS detection is too early. 1'b1: Disable the fix of too early SDS detection in L0sRx.	1'b0
0x5C0	vesc_reg46[20]	cb_l0s_sds_detect_fix_dis (Gen3) 1'b0: Fix to save the indication of received SDS in L0sRx 1'b1: Disable the fix of SDS detection flag.	1'b0

Offset	Bits	Description	Value
0x5C0	vesc_reg46[21]	cb_sel_time_of_invalid_request (Grn3) Selects the time invalid request will be asserted 1'b0: 2 cycles 1'b1: 8 cycles	1'b0
0x5C0	vesc_reg46[22]	cb_sync_tx_valid_and_ei_fix_dis (Gen3) 1'b0: Fix to sync TxDataValid assertion to de-assertion of Rx Electrical Idle to meet PIPE Spec timing 1'b1: The issue is not fixed	1'b0
0x5C0	vesc_reg46[23]	cb_xmode_phy_tx_delay_dis 1'b0: Fix to delay xmode indication for Rx block 1'b1: Fix to delay xmode indication for Rx block is disabled	1'b0
0x5C0	vesc_reg46[24]	cb_xmode_phy_rx_delay_dis 1'b0: Fix to delay xmode indication for Tx block 1'b1: Fix to delay xmode indication for Tx block is disabled	1'b0
0x5C0	vesc_reg46[25]	cb_dn_retrain_link_upon_up_rate_change_en 1'b0: No effect 1'b1: Retrain Link of Dn Port while Up Port changes speed (This bit is valid for Dn port and reserved for Up/Ep)	(Dn) 1'b0
0x5C0	vesc_reg46[26]	cb_disable_retrain_link_dllp_absence 1'b0: No Effect 1'b1: Disable Link Recovery due to absence of DLLP (DFT)	1'b0
0x5C0	vesc_reg46[28:27]	cb_retrain_link_value_sel Selects timeout value of DLLP absence for Link Recovery 2'b00: 256 us 2'b01: 512 us 2'b10: 1 ms 2'b11: 4 ms	2'b00
0x5C0	vesc_reg46[29]	cb_send_less_periodic_fc_dllp 1'b0: No effect 1'b1: Send less periodic DLLP FC Update	1'b0
0x5C0	vesc_reg46[30]	cb_slow_clk_faster_dllp_update_en 1'b0: No effect 1'b1: During L1/L2 without Clock and using slow internal clock periodic DLLP timer acceleration	1'b1
0x5C0	vesc_reg46[31]	Reserved	1'b0

Table 147. VESC_REG 47: (Offset C4h): General configuration register

Offset	Bits	Description	Value
0x5C4	vesc_reg47[0]	cb_skip_det_shift_en 1'b0: No effect 1'b1: Option to detect SKIP if internally it was shifted	1'b0

Offset	Bits	Description	Value
0x5C4	vesc_reg47[1]	cb_sds_detect_by_12_bytes 1'b0: No effect 1'b1: Option to detect SDS by less bytes (12 instead of 16)	1'b0
0x5C4	vesc_reg47[2]	cb_main_lane_not_active_fix_en 1'b0: No effect 1'b1: Fix to reset Rx Data Path is main lane is not active	1'b1
0x5C4	vesc_reg47[3]	cb_false_dllp_chk_dis 1'b0: Fix for not to miss TLP because of DLLP before it 1'b1: Fix is disabled	1'b0
0x5C4	vesc_reg47[4]	cb_false_dllp_chk_dis_short 1'b0: Fix for not to miss TLP because of back to back DLLP before it (treats slightly different case them bit 3) 1'b1: Fix is disabled	1'b0
0x5C4	vesc_reg47[5]	cb_plmux_tx_ei_gap_fix_dis 1'b0: Fix to leave Tx EI asserted till TxDataValid is asserted 1'b1: Fix is disabled	1'b0
0x5C4	vesc_reg47[6]	cb_early_tx_ei_fall_2mux 1'b0 : No effect 1'b1 : Option to de-assert internal Tx EI earlier (DFT)	1'b0
0x5C4	vesc_reg47[7]	cb_slave_delay_byte6_fix_dis 1'b0: Fix to align TS byte 6 with EC during Eq slave phase 1'b1: Fix is disabled	1'b0
0x5C4	vesc_reg47[8]	cb_custom_clr_equalization_done 1'b0 : No effect 1'b1 : Custom DFT bit to clear Equalization done indication	1'b0
0x5C4	vesc_reg47[9]	cb_perform_equal_every_rate_change 1'b0: No effect 1'b1: Equalization will be performed at every entry to Gen3	1'b0
0x5C4	vesc_reg47[10]	cb_upcomp0_end_of_phase3_fix_dis 1'b0: Align TS EC/coeff fields at the end of Eq Phase 3 1'b1: The delay is disabled	1'b0
0x5C4	vesc_reg47[11]	cb_upcomp1_end_of_phase2_fix_dis 1'b0: Align TS EC/coeff fields at the end of Eq Phase 2 1'b1: The delay is disabled	1'b0
0x5C4	vesc_reg47[12]	cb_delay_frame_error_dis 1'b0 : Frame Error indication is delayed in LTSSM 1'b1 : The delay is disabled	1'b0
0x5C4	vesc_reg47[13]	cb_mask_frame_err_with_ei 1'b0: Frame Error indication is valid only if there is no Rx EI 1'b1: Rx EI doesn't mask Framing Error	1'b0

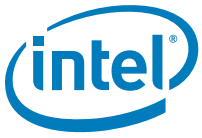


Offset	Bits	Description	Value
0x5C4	vesc_reg47[14]	cb_tx_data_valid_fall_sync_fix_en 1'b0: Fix to align TxDataValid cycle shortly after end of Tx EI 1'b1: Fix is disabled	
0x5C4	vesc_reg47[15]	cb_gen3_delay_tx_ei_fix_dis 1'b0: Fix to delay Tx EI de-assertion till TxDataValid cycle 1'b1: Fix is disabled	1'b0
0x5C4	vesc_reg47[16]	cb_reset_fsm_in_tx_ei_fix_dis 1'b0: Reset PIPEMux FSM during Tx EI in Gen3 fix 1'b1: Fix is disabled	1'b0
0x5C4	vesc_reg47[17]	cb_gen3_mult_eieos_fix_dis (Recovery) 1'b0: Send several EIEOS during exit from Tx EI (in Gen3) 1'b1: Send only one EIEOS during exit from TxEI (One EIEOS can be missed due to TxEI /TDataValid fixes)	1'b0
0x5C4	vesc_reg47[18]	cb_gen3_num_of_eieos_sel (Recovery) 1'b0: Launch 3 EIEOS (should insure at least one EIEOS in PIPE) 1'b1: Launch 4 EIEOS	1'b0
0x5C4	vesc_reg47[19]	cb_gen3_l0stx_mult_eieos_fix_dis (L0s) 1'b0: Send several EIEOS during exit from Tx EI (in Gen3) 1'b1: Send only one EIEOS during exit from TxEI (One EIEOS can be missed due to TxEI /TDataValid fixes)	1'b0
0x5C4	vesc_reg47[20]	cb_gen3_l0stx_num_of_eieos_sel (L0s) 1'b0: Launch 3 EIEOS (should insure at least one EIEOS in PIPE) 1'b1: Launch 4 EIEOS	1'b0
0x5C4	vesc_reg47[21]	cfg_lane_num_wait_timer_fix_dis 1'b0: Extra time wait enable in Config.LaneNumAccept state 1'b1: Extra time wait disabled in Config.LaneNumAccept state	1'b0
0x5C4	vesc_reg47[22]	cfg_lane_num_wait_sel 1'b0: Extra time wait is till next us tick 1'b1: Extra time wait is till end of state timeout	1'b0
0x5C4	vesc_reg47[23]	cb_gen3_comp_pattern_align_fix_dis 1'b0: Fix of delaying start of Compliance Pattern till de-assertion of Tx Electrical Idle 1'b1: Fix is disabled	1'b0
0x5C4	vesc_reg47[24]	cb_gen3_eieos_pipe_demux_align_en 1'b0: No effect 1'b1: Re-align PIPEDemux at EIEOS	1'b0
0x5C4	vesc_reg47[25]	cb_pipe_demux_rst_after_de_skew_en 1'b0: No effect 1'b1: Reset PIPEDemux after each change of De-Skew	1'b1

Offset	Bits	Description	Value
0x5C4	vesc_reg47[26]	cb_chan0_short_ipg_fix_dis 1'b0 : Arbiter wait 2 cycles in Fine Adjust state 1'b1 : Arbiter wait 3 cycles in Fine Adjust state	1'b0
0x5C4	vesc_reg47[27]	cb_chan1_short_ipg_fix_dis 1'b0: Arbiter wait 2 cycles in Fine Adjust state 1'b1: Arbiter wait 3 cycles in Fine Adjust state	1'b0
0x5C4	vesc_reg47[28]	cb_chan2_short_ipg_fix_dis 1'b0: Arbiter wait 2 cycles in Fine Adjust state 1'b1: Arbiter wait 3 cycles in Fine Adjust state	1'b0
0x5C4	vesc_reg47[29]	cb_fine_adjust_shorter_dis While comes to this state from Credit Update state 1'b0: Arbiter wait 2 cycles in Fine Adjust state 1'b1: Arbiter wait 3 cycles in Fine Adjust state	1'b0
0x5C4	vesc_reg47[30]	cb_chan0_skip_update_credit_state_sel 1'b0: No Effect 1'b1: Skip Update Credit state on channel 0	(EP port) 1'b0
0x5C4	vesc_reg47[31]	cb_chan1_skip_update_credit_state_sel 1'b0: No Effect 1'b1: Skip Update Credit state on channel 1	(EP port) 1'b0

Table 148. VESC_REG 48: (Offset C8h): General configuration register

Offset	Bits	Description	Value
0x5C8	vesc_reg48[0]	cb_pmtop_ei_alllanes_sel (all lanes for PMTop block) 1'b0: Rx EI detection according to PIPE signals 1'b1: Rx EI detection according internal indication (in non Gen1 mode generated from EIOS / EIEOS packets)	1'b0
0x5C8	vesc_reg48[1]	cb_after_invalid_request_change_coeff 1'b0: Try same coeffs after invalid request 1'b1: Try different coeffs after invalid request	1'b0
0x5C8	vesc_reg48[2]	cb_upcomp0_end_of_ph3_delay_sel 1'b0: Fix of delaying Phase 3 in Dn Port 1'b1: Fix is disabled	1'b0
0x5C8	vesc_reg48[3]	cb_upcomp1_end_of_ph2_delay_sel 1'b0 : Fix of delaying Phase 2 in Up/Rp Port 1'b1 : Fix is disabled	1'b0
0x5C8	vesc_reg48[4]	cb_wait_for_preset_change 1'b0: Fix is not enabled 1'b1: During Equalization Slave phase wait for Preset change before each new validation of coeffs	1'b1



Offset	Bits	Description	Value
0x5C8	vesc_reg48[5]	cb_detect_rx_ei_any_sel_det (any lane for Detect) 1'b0: Rx EI is detected according to PIPE signal 1'b1: Rx EI is detected according PIPE signal in Gen1 and according EIOS/PIPE signal in Gen2/Gen3 (vesc_reg41[3:1])	1'b0
0x5C8	vesc_reg48[6]	cb_detect_rx_ei_any_sel_poll (any lane for Polling) 1'b0: Rx EI is detected according to PIPE signal 1'b1: Rx EI is detected according PIPE signal in Gen1 and according EIOS/PIPE signal in Gen2/Gen3 (vesc_reg41[3:1])	1'b0
0x5C8	vesc_reg48[7]	cb_detect_rx_ei_any_sel_recov (any lane for Recovery) 1'b0: Rx EI is detected according to PIPE signal 1'b1: Rx EI is detected according PIPE signal in Gen1 and according EIOS/PIPE signal in Gen2/Gen3 (vesc_reg41[3:1])	1'b1
0x5C8	vesc_reg48[8]	cb_detect_rx_ei_all_sel_ltssm (all lanes for LTSSM) 1'b0: Rx EI is detected according PIPE signal in Gen1 and according EIOS/PIPE signal in Gen2/Gen3 (vesc_reg41[3:1]) 1'b1: Rx EI is detected according to PIPE signal	1'b0
0x5C8	vesc_reg48[9]	cb_detect_rx_ei_all_sel_hot (all lanes for Hot Reset) 1'b0: Rx EI is detected according PIPE signal in Gen1 and according EIOS/PIPE signal in Gen2/Gen3 (vesc_reg41[3:1]) 1'b1: Rx EI is detected according to PIPE signal	1'b0
0x5C8	vesc_reg48[10]	cb_detect_rx_ei_all_sel_l0s (all lanes for L0s) 1'b0: Rx EI is detected according PIPE signal in Gen1 and according EIOS/PIPE signal in Gen2/Gen3 (vesc_reg41[3:1]) 1'b1: Rx EI is detected according to PIPE signal	1'b0
0x5C8	vesc_reg48[11]	cb_detect_rx_ei_all_sel_l1prep (all lanes for L1Prep) 1'b0: Rx EI is detected according PIPE signal in Gen1 and according EIOS/PIPE signal in Gen2/Gen3 (vesc_reg41[3:1]) 1'b1: Rx EI is detected according to PIPE signal	1'b0
0x5C8	vesc_reg48[12]	cb_detect_rx_ei_all_sel_l1seq (all lanes for L1Seq) 1'b0: Rx EI is detected according PIPE signal in Gen1 and according EIOS/PIPE signal in Gen2/Gen3 (vesc_reg41[3:1]) 1'b1: Rx EI is detected according to PIPE signal	1'b0
0x5C8	vesc_reg48[13]	cb_detect_rx_ei_all_sel_l2seq (all lanes for L2Seq) 1'b0: Rx EI is detected according PIPE signal in Gen1 and according EIOS/PIPE signal in Gen2/Gen3 (vesc_reg41[3:1]) 1'b1: Rx EI is detected according to PIPE signal	1'b0
0x5C8	vesc_reg48[14]	cb_anylane_exit_rx_ei_sel_detect (any lane for Detect) 1'b0: Rx EI exit is detected according to PIPE signal 1'b1: Rx EI exit is detected according PIPE signal in Gen1 and according EIOS/PIPE signal in Gen2/Gen3 (vesc_reg41[3:1])	1'b0

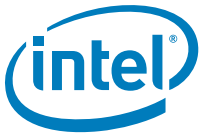
Offset	Bits	Description	Value
0x5C8	vesc_reg48[15]	cb_anylane_exit_rx_ei_sel_comp (any lane for Comp) 1'b0: Rx EI exit is detected according to PIPE signal 1'b1: Rx EI exit is detected according PIPE signal in Gen1 and according EIOS/PIPE signal in Gen2/Gen3 (vesc_reg41[3:1])	1'b0
0x5C8	vesc_reg48[16]	cb_anylane_exit_rx_ei_sel_dis (any lane for Disabled) 1'b0: Rx EI exit is detected according to PIPE signal 1'b1: Rx EI exit is detected according PIPE signal in Gen1 and according EIOS/PIPE signal in Gen2/Gen3 (vesc_reg41[3:1])	1'b0
0x5C8	vesc_reg48[17]	cb_alllanes_exit_rx_ei_sel_poll (all lane for Polling) 1'b0: Rx EI exit is detected according to PIPE signal 1'b1: Rx EI exit is detected according PIPE signal in Gen1 and according EIOS/PIPE signal in Gen2/Gen3 (vesc_reg41[3:1])	1'b0
0x5C8	vesc_reg48[18]	cb_alllanes_exit_rx_ei_sel_loop (all lane for Loop) 1'b0: Rx EI exit is detected according to PIPE signal 1'b1: Rx EI exit is detected according PIPE signal in Gen1 and according EIOS/PIPE signal in Gen2/Gen3 (vesc_reg41[3:1])	1'b0
0x5C8	vesc_reg48[19]	cb_rst_ts_detection_during_speed_fix 1'b0: Fix is not enabled 1'b1: Fix in Recovery.Speed to reset TS detection	1'b1
0x5C8	vesc_reg48[20]	cb_delay_exit_from_comp 1'b0: No effect 1'b1: Delay of one cycle during exit from Compliance	1'b0
0x5C8	vesc_reg48[21]	cb_gen3_longer_eios_detect_en 1'b0: Gen3 EIOS detection according to Spec (4 symbols) 1'b1: EIOS detection based on 8 symbols	1'b0
0x5C8	vesc_reg48[22]	cb_gen3_l0srx_deskew_on_sds 1'b0: Perform Gen3 de-skew on FTS during exit from L0sRx 1'b1: Perform Gen3 de-skew on SDS during exit from L0sRx	1'b0
0x5C8	vesc_reg48[23]	cb_gen2_l0srx_deskew_on_fts 1'b0: Perform Gen2 de-skew on SKIP during exit from L0sRx 1'b1: Perform Gen2 de-skew on FTS during exit from L0sRx	1'b1
0x5C8	vesc_reg48[24]	cb_second_l1soft_dis 1'b0: Fix to disable second L1Soft after D-state return to D0 (bad fix) 1'b1: Fix to disable second L1Soft after D-state return to D0	1'b1
0x5C8	vesc_reg48[25]	cb_recov_eq_counter_value_sel Up/Dn wait time in Phase 0/1 1'b0: 200ns 1'b1: 400ns	1'b0

Offset	Bits	Description	Value
0x5C8	vesc_reg48[26]	cb_gen3_hot_reset_change_en 1’b0: No effect 1’b1: Gen3 change for Hot Reset (not required)	1'b0
0x5C8	vesc_reg48[27]	cb_l1_aspm_l1_timer_en 1’b0: After detecting Rx EI in ASPM L1 exit condition valid immediately 1’b1: After detecting Rx EI in ASPM L1 exit condition valid after some time	1'b0
0x5C8	vesc_reg48[28]	cb_l1_soft_l1_timer_en 1’b0: After detecting Rx EI in Soft L1 exit condition valid immediately 1’b1: After detecting Rx EI in Soft L1 exit condition valid after some time	1'b0
0x5C8	vesc_reg48[29]	cb_pipe_mux_delay_tx_ei_dis 1’b0: PIPE Mux Tx EI is delayed by one cycle 1’b1: PIPE Mux Tx EI is not delayed by one cycle	1'b0 1'b1 – for gen3 compliance testing
0x5C8	vesc_reg48[30]	cb_pipe_mux_ei_start_block_fix_dis 1’b0: No effect 1’b1: Last Start Block after EIOS is masked	1'b0
0x5C8	vesc_reg48[31]	cb_pipe_mux_ei_data_valid_fix_dis 1’b0: No effect 1’b1: Fix to leave TxDataValid high during TxEI	1'b0

Table 149. VESC_REG 49: (Offset CCh): General configuration register

Offset	Bits	Description	Value
0x5CC	vesc_reg49[7:0]	cb_custom_init_bus_num_load The value will be loaded to Bus Number after Link Up	8'h0
0x5CC	vesc_reg49[8]	cb_custom_send_pm_pme_msg 1’b0: No effect 1’b1: Option to trigger PM_PME message Note: relevant to the XHC EMEP only.	1’b0
0x5CC	vesc_reg49[9]	cb_disable_pm_pme_msg 1’b0: No effect 1’b1: Disable PM_PME message send	1’b0
0x5CC	vesc_reg49[10]	cb_early_send_eios_fix_dis 1’b0: EIOS send fix 1’b1:Fix is disabled	1’b0
0x5CC	vesc_reg49[11]	cb_exit_ei_flag_fall_upon_rx_ei_en 1’b0: No effect 1’b1: Rx EI exit flag is de-asserted upon Rx EI signal	1’b1

Offset	Bits	Description	Value
0x5CC	vesc_reg49[12]	cb_exit_ei_flag_rise_upon_rx_ei_en 1'b0: No effect 1'b1: Rx EI exit flag is asserted upon Rx EI signal	1'b0
0x5CC	vesc_reg49[13]	cb_chan_arb_rr_fix_dis 1'b0: Channel Arbiter is Round Robin (fix) 1'b1: Channel Arbiter is Round Robin only under stress traffic	1'b0
0x5CC	vesc_reg49[14]	cb_chan_arb_vc0_cfg 1'b0: Default order of channel in arbitration (VC0) 1'b1: Different order of channels for Up/Dn (VC0)	1'b0
0x5CC	vesc_reg49[15]	cb_chan_arb_vc1_cfg 1'b0: Default order of channel in arbitration (VC1) 1'b1: Different order of channels for Up/Dn (VC1)	1'b0
0x5CC	vesc_reg49[16]	cb_l1_aspm_timer_sel Select the l1 ASPM timer value (clock cycles) 1'b0: 30 1'b1: 60	1'b0
0x5CC	vesc_reg49[17]	cb_l1_soft_timer_sel Select the l1 Soft timer value (clock cycles) 1'b0: 30 1'b1: 60	1'b0
0x5CC	vesc_reg49[18]	cb_init_l1_exit_en 1'b0: L1 exit indication toward other ports is forced to zero 1'b1: Enable to assert L1 exit indication toward other ports	1'b0
0x5CC	vesc_reg49[19]	cb_exit_l1_by_other_port_dis 1'b0: Exit from L1 triggered by indication from other ports 1'b1: Exit from L1 by indication from other ports is disabled	1'b0
0x5CC	vesc_reg49[20]	cb_l0s_gen2_exit_12_eie_en 1'b0: Rx EI exit is detected by full EIEOS. 1'b1: Enable to detect Rx EI exit in gen2 by 12 EIE symbols	1'b0
0x5CC	vesc_reg49[21]	cb_send_extra_skip_in_recov_cfg 1'b0: No effect 1'b1: Send extra Skip during transition to Recovery.Cfg	1'b0
0x5CC	vesc_reg49[22]	cb_gen2_4_eie_detect_en 1'b0: Rx EI exit is detected by 8 or more EIE (also EIEOS) 1'b1: Enable to detect Rx EI exit in gen2 by 4 EIE symbols	1'b0
0x5CC	vesc_reg49[23]	cb_dllp_detect_mask_during_tlp_ip_x1_en 1'b0: No effect 1'b1: Mask DLLP detection during valid TLP in gen3 x1 mode	1'b1

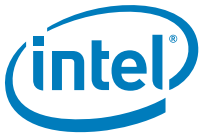


Offset	Bits	Description	Value
0x5CC	vesc_reg49[24]	cb_dllp_detect_mask_during_tlp_ip_x2_en 1'b0: No effect 1'b1: Mask DLLP detection during valid TLP in gen3 x2 mode	1'b0
0x5CC	vesc_reg49[25]	cb_dllp_detect_mask_during_tlp_ip_x4_en 1'b0: No effect 1'b1: Mask DLLP detection during valid TLP in gen3 x4 mode	1'b0
0x5CC	vesc_reg49[26]	cb_enable_extra_skip_after_l0 1'b0: No effect 1'b1: Adds extra Skip in the beginning of Recovery state	1'b0
0x5CC	vesc_reg49[27]	cb_entry_to_recov_speed_strech 1'b0: No effect 1'b1: Stretches entry to Recovery.Speed indication	1'b1
0x5CC	vesc_reg49[28]	cb_consider_eios_detected_on_rx_ei_rise 1'b0: No effect 1'b1: EIOS detected indication is asserted on Rx EI rise (This can be used if Rx EI detection happens in the PHY and EIOS is not reliably detected)	1'b0
0x5CC	vesc_reg49[29]	cb_redund_recov_after_l1_hot_reset_fix_dis 1'b0: Fix to eliminate redundant Recovery in case of Hot Reset trigger during L1 state. 1'b1: Fix is disabled	1'b0
0x5CC	vesc_reg49[30]	cb_redund_recov_after_l1_retrain_fix_dis 1'b0: Fix to eliminate redundant Recovery in case of Link Retraining trigger during L1 state. 1'b1: Fix is disabled	1'b0
0x5CC	vesc_reg49[31]	Reserved	1'b0

Table 150. VESC_REG 50: (Offset D0h): General configuration register

Offset	Bits	Description	Value
0x5D0	vesc_reg50[1:0]	cb_delay_ei_infer_detect_indication Control the delays of EI inferring indication to PHY 2'b00: 4 cycles 1'b01: 8 cycles 1'b01: 12 cycles 1'b01: 16 cycles	2'b00
0x5D0	vesc_reg50[2]	cb_delay_eios_detect_indication 1'b0: No effect 1'b1: Delays EIOS detection indication to PHY for 2 cycles	1'b0
0x5D0	vesc_reg50[3]	cb_gen2_rxvalid_rise_rst_pipedemux 1'b0: No effect 1'b1: Reset PIPEDemux upon any RxValid rise in Gen2	1'b0

Offset	Bits	Description	Value
0x5D0	vesc_reg50[4]	cb_gen3_rxvalid_rise_rst_pipedemux 1'b0: No effect 1'b1: Reset PIPEDemux upon any RxValid rise in Gen3	1'b0/1'b1
0x5D0	vesc_reg50[5]	cb_dllsm_inactive_for_l0s_fix_dis 1'b0: L0sPrep FSM doesn?t enter L0s during DLLSM activity 1'b1: Disable the fix	1'b0
0x5D0	vesc_reg50[6]	cb_pol_force_deemp_from_link_ctrl2_reg_en 1'b0: No effect 1'b1: Forces TxDemph directly from link ctrl 2 register	1'b0
0x5D0	vesc_reg50[7]	cb_rx_valid_drop_upon_rx_ei_en 1'b0: No effect 1'b1: Drops RxValid upon Rx EI assertion in LaneReversal	1'b1
0x5D0	vesc_reg50[8]	cb_rx_data_valid_drop_upon_rx_ei_en 1'b0: No effect 1'b1: Drops RxDataValid upon Rx EI assertion in LaneReversal	1'b1
0x5D0	vesc_reg50[9]	cb_blk_align_assert_during_recovery 1'b0: No effect 1'b1: Block align control is asserted during Recovery state	1'b1
0x5D0	vesc_reg50[10]	cb_blk_align_assert_during_configuration 1'b0: No effect 1'b1: Block align control is asserted during Configuration state	1'b1
0x5D0	vesc_reg50[11]	cb_blk_align_assert_during_l0s 1'b0: No effect 1'b1: Block align control is asserted during L0sRx state	1'b1
0x5D0	vesc_reg50[12]	cb_reset_lane_reverse_l0srx_to_reco_en 1'b0: No effect 1'b1: Reset Valid in Lane Reversal block on transition from L0sRx to Recovery	1'b0
0x5D0	vesc_reg50[13]	cb_reset_lane_reverse_recov_en 1'b0: No effect 1'b1: Reset Valid in Lane Reversal block on entry to Recovery	1'b0
0x5D0	vesc_reg50[14]	cb_sds_easy_detection 1'b0: No effect 1'b1: Enable easier detection of SDS (without start/end DW)	1'b0
0x5D0	vesc_reg50[15]	cb_mask_frame_for_descranbler 1'b0: No effect 1'b1: Mask Framing error for descrambler (DFT)	1'b0



Offset	Bits	Description	Value
0x5D0	vesc_reg50[16]	cb_mask_frame_error_in_recov_idle 1'b0: No effect 1'b1: Mask Framing error in recovery idle (for descrambler)	1'b0
0x5D0	vesc_reg50[17]	cb_clr_data_strm_valid_upon_frame_err_en 1'b0: No effect 1'b1:Frame Error clears Data Stream Valid flag	1'b0
0x5D0	vesc_reg50[18]	cb_clr_data_stream_valid_upon_bad_sync_hdr 1'b0: No effect 1'b1:Bad Sync header clears Data Stream Valid flag	1'b0
0x5D0	vesc_reg50[19]	cb_set_data_stream_valid_upon_sds_en 1'b0: No effect 1'b1: SDS set the Data Stream Valid	1'b0/1'b1
0x5D0	vesc_reg50[20]	cb_set_data_stream_valid_upon_sds_after_err_dis 1'b0: Setting Data Stream Valid is upon SDS if there was error 1'b1: Setting Data Stream Valid is upon SDS (This bit effects only if bit 19 is set)	1'b0/1'b1
0x5D0	vesc_reg50[23:21]	cb_reduce_post_fc_credits Controls the Post Hdr FC credit reduction 3'b000 - Default value 3'b001 - Default value -4 3'b010 - Default value divided by 2 3'b011 - Default value divided by 2 plus 2 3'b100 - Default value divided by 2 minus 2 3'b101 - 8 credits 3'b110 - 6 credits 3'b111 - 4 credits	3'b000
0x5D0	vesc_reg50[24]	cb_ignore_recovery_for_clk_req 1'b0: port considered not idle if its LTSSM is in Recovery 1'b1: port considered idle if its LTSSM is in Recovery	1'b0
0x5D0	vesc_reg50[25]	cb_mask_ts_detection_during_rx_ei_dis 1'b0: TS detection is masked with Rx EI 1'b1:TS detection is not masked with Rx EI (minor bug)	1'b0
0x5D0	vesc_reg50[26]	cb_dont_perform_eq_if_optimal_dis 1'b0: Equalization is not triggered in Recovery entry if Equalization was done once well 1'b1: Equalization is triggered in Recovery entry even if Equalization was done once well	1'b0

Offset	Bits	Description	Value
0x5D0	vesc_reg50[27]	cb_perform_eq_only_from_non_gen3_dis 1'b0: Equalization is triggered in Recovery entry only if rate is not Gen3 and the target link speed is Gen3 1'b1: Equalization is triggered in Recovery entry if the target link speed is Gen3 (no matter if it comes from Gen3)	1'b0
0x5D0	vesc_reg50[28]	cb_invert_start_equalization_w_preset 1'b0: no change 1'b1: (Legacy)	1'b0
0x5D0	vesc_reg50[29]	cb_l0s_to_l0_without_skp_sds_en 1'b0: No effect 1'b1: Enable to exit from L0sRx to L0 without SKP / SDS	1'b0
0x5D0	vesc_reg50[30]	cb_recov_cfg_gen2_deemp_update_en 1'b0: No effect 1'b1: Port updates de-emphasis for Gen2 in Recoevery.Cfg	1'b0/1'b1 (Dn = 1) (Up = 0)
0x5D0	vesc_reg50[31]	cb_recov_cfg_gen2_deemp_value 1'b0: No effect 1'b1: Option to set value of -3.5dB while Port goes to Gen2 (Relevant if bit 30 is set)	1'b0

Table 151. VESC_REG 51: (Offset D4h): General configuration register

Offset	Bits	Description	Value
0x5D4	vesc_reg51[0]	cb_recovery_lock_to_cfg_force 1'b0: No effect 1'b1: Force recovery lock to cfg transition condition (DFT)	1'b0
0x5D4	vesc_reg51[1]	cb_recovery_cfg_to_idle_force 1'b0: No effect 1'b1: Force recovery cfg to idle transition condition (DFT)	1'b0
0x5D4	vesc_reg51[2]	cb_recovery_got_idle_force 1'b0: No effect 1'b1: Force got idle condition in recovery (DFT)	1'b0
0x5D4	vesc_reg51[3]	cb_configuration_got_idle_force 1'b0: No effect 1'b1: Force got idle condition in configuration (DFT)	1'b0
0x5D4	vesc_reg51[4]	cb_recov_lock_to_detect_timeout_cancel 1'b0: No effect 1'b1: Mask timeout exp for recovery lock to detect (DFT)	1'b0
0x5D4	vesc_reg51[5]	cb_recov_cfg_to_detect_timeout_cancel 1'b0: No effect 1'b1: Mask timeout exp for recovery cfg to detect (DFT)	1'b0

Offset	Bits	Description	Value
0x5D4	vesc_reg51[6]	cb_recov_idle_to_detect_timeout_cancel 1'b0: No effect 1'b1: Mask timeout exp for recovery idle to detect (DFT)	1'b0
0x5D4	vesc_reg51[7]	cb_cfg_lane_num_to_detect_timeout_cancel 1'b0: No effect 1'b1: Mask timeout exp for configuration lane num accept to detect (DFT)	1'b0
0x5D4	vesc_reg51[8]	cb_cfg_complete_to_detect_timeout_cancel 1'b0: No effect 1'b1: Mask timeout exp for configuration complete to detect (DFT)	1'b0
0x5D4	vesc_reg51[9]	cb_cfg_idle_num_to_detect_timeout_cancel 1'b0: No effect 1'b1: Mask timeout exp for configuration idle to detect (DFT)	1'b0
0x5D4	vesc_reg51[10]	Mask Lane error status 1'b0: No effect 1'b1: Mask lane error status in PCIE Secondary Capability (DFT)	1'b0
0x5D4	vesc_reg51[11]	Mask Receiver error status 1'b0: No effect 1'b1: Mask receiver error status in Advanced Error Reporting Capability (DFT)	1'b0
0x5D4	vesc_reg51[12]	cb_force_rcvr_detected_according_to_xmode 1'b0: No effect 1'b1: Rx Detection successful indication is forced.	1'b0
0x5D4	vesc_reg51[13]	cb_reset_eios_det_on_pol_com_exit 1'b0: No effect 1'b1: Reset EIOS detection upon exit from Polling Compliance	1'b0
0x5D4	vesc_reg51[14]	cb_stay_in_p0_during_link_dis 1'b0: During Link Disable PHY is directed to P1 (Spec) 1'b1: During Link Disable PHY is directed to stay in P0	1'b0
0x5D4	vesc_reg51[15]	cb_dft_force_ts_detect 1'b0: No effect 1'b0: DFT option to force TS detection	1'b0
0x5D4	vesc_reg51[16]	cb_dft_force_enter_ei 1'b0: No effect 1'b0: DFT option to force Tx EI entry	1'b0
0x5D4	vesc_reg51[17]	cb_dft_force_idle_detect 1'b0: No effect 1'b0: DFT option to force IDLE detection	1'b0

Offset	Bits	Description	Value
0x5D4	vesc_reg51[18]	cb_dft_force_eios_detect 1'b0: No effect 1'b0: DFT option to force EIOS detection	1'b0
0x5D4	vesc_reg51[19]	cb_dft_force_exit_l1 1'b0: No effect 1'b0: DFT option to force exit L1	1'b0
0x5D4	vesc_reg51[23:20]	cb_gen3_preset_coeff_ctrl Control of the coefficients in Preset table	4'h0
0x5D4	vesc_reg51[24]	Force pipe rate signal 1'b0: No Effect 1'b1: pipe rate is overwritten by bits [26:25]	1'b0
0x5D4	vesc_reg51[26:25]	Pipe Rate force value Value that is forced if bit 24 is set	2'b00
0x5D4	vesc_reg51[27]	Force power dowm signal 1'b0: No Effect 1'b1: power down is overwritten by bits [29:28]	1'b0
0x5D4	vesc_reg51[29:28]	Power Down force value Value that is forced if bit 27 is set	2'b00
0x5D4	vesc_reg51[30]	Force Tx Electrical Idle 1?b0: No Effect 1?b1: Tx Electrical Idle is overwritten by bits [31]	1'b0
0x5D4	vesc_reg51[31]	Tx Electrical Idle force value Value that is forced if bit 24 is set	1'b0

4.5.12.1 TBT Registers access through PCIE

The access is done through three registers in Upstream Port Vendor register Space (Reg10,11,12 - 0x530,0x534, 0x538).

- **Register 1 (0x530)** is a Command (two special bits: 30,31)
  - Bit 30 is a status bit that indicates that access is in progress (set by SW cleared by HW)
  - Bit 31 is a timeout bit that indicates that the returned data is invalid (loaded with ack)
- **Register 2 (0x534)** is a Write Data Register (simple Wr/Rd register)
- **Register 3 (0x538)** is a Read Data Register (Rd Only register)loaded with ack by HW.

Write command flow:

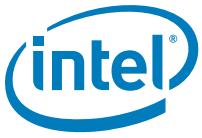
- PCIE Software writes Data to Write Data Register

- PCIE Software writes Command Register - bit 30 indicates to start write command

- PCIE Switch wrapper logic perform write of CIO register

- Ack and timeout are returned (bits 30 is cleared by ack, bit 31 is loaded from timeout input)

- SW read the Command Register to see if there is no timeout (bit 30 and 31 are zero)



Read command flow:

- PCIE Software writes Command Register - bit 30 indicates to start read command

- PCIE Switch wrapper logic perform read of CIO register.

- Ack and timeout are returned (bits 30 is cleared by ack,31 is loaded from timeout input)

- Input DW rd_data signal is loaded to Read Data Register based on ack input pulse.

- SW read the Command Register to see if there is no timeout (bit 30 and 31 are zero)

- PCIE Software can read Data Register (if transaction is finished and there is no timeout - bits 30,31)

See also Table 17, “Command Register Parameters” on page 83.

4.5.12.2 Custom PCIE-TBT Mailbox Registers

The registers TBT2PCIE/PCIE2TBT act as a Mailbox and enable communication between the SW and the CM/LC

- SW initiates a transaction through the PCIE2TBT Mailbox by setting PCIE2TBT with a message and setting the "Valid" bit
- CM/LC are interrupted on this transaction, CM/LC execute on the transaction
- Once done CM/LC sets the "Done" bit in TBT2PCIE with the proper command and data
- SW polls TBT2PCIE for the "Done" bit (and potential data as needed)
- SW clears the PCIE2TBT "Valid" bit, CM is interrupted on this transaction
- CM clears the TBT2PCIE "Done" bit
- SW should poll to see Done bit is cleared
- At this point the SW driver can issue another PCIE2TBT transaction as needed

4.5.12.3 Custom LTR Registers

Custom LTR registers are located under Vendor Defined Extended Capability that starts at offset 0x500.

Downstream Port (offsets 0x53C, 0x540 and 0x544)

- Configurable LTRDnport registers for snoop / non-snoop (one DW similar to the Message)
  - register captures latency from LTR message (unless "lock" bit is set)
  - software or internal chip logic can override and lock this register.
  - change of the register triggers LTR message on Upstream Port (if conglomerated value was changed)
- Configurable bit in to ignore this Downstream Port LTR values for calculation
  - change of the register trigger LTR message on Upstream Port (if conglomerated value was changed)

Offset 0x53C - LTR Idle Value.

See Figure 66.

Figure 66. LTR Idle Value

Offset 0x540 - LTR Active Value (Same structure as Idle beside the bits 29 and 13 are reserved)

Offset 0x544 - LTR active timer initial value control (Rd / Wr DW)

Embedded Endpoint (offset 0x53C)

- Configurable **LTREMEP** register for LTR snoop / non-snoop latency (one DW as in Message)
  - — software or internal chip logic can load this register.
  - — change of the register triggers LTR message in Embedded Endpoint (if value was changed or "send" bit)

Figure 67. LTR Value of Embedded Endpoint

Note: "send" bit is self-cleared (cleared after the message has been sent)

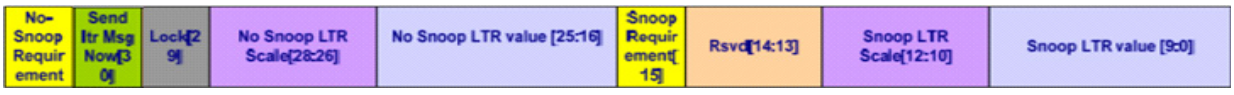
Upstream Port (offsets 0x53C and 0x540)

- Configurable **LTRConglomerated** register for snoop / non-snoop
  - — register is calculated according to Spec (unless "lock" bit is set)
  - — software or internal chip logic can override this register.
  - — change of the register trigger LTR message on Upstream Port (if value was changed or "send" bit)
- Configurable **LSwitch** registers to enable control over Switch latency value.
  - — software or internal chip logic can override this register.
  - — change of the register triggers LTR message on Upstream Port (if conglomerated value was changed)

Offset 0x53C - LTR Conglomerated Value

See Figure 68.

Figure 68. LTR Conglomerated Value



Offset 0x540 - LSwitch register

SeeFigure 69.

Figure 69. LSwitch register

Note: "send" bit is self-cleared (cleared after the message has been sent)

Offset 0x544 - BIOS mailbox (Rd / Wr)

Table 152. VESC_REG 49: (Offset CCh): General configuration register

Offset	Bits	Description	Value
0x544	vesc_reg15[0]	Hot plug filter indication, if read as 1, BIOS should clear the bit and continue normal flow, if read as 0 BIOS should exit the GPIO handler. This bit is only implemented in AR, not applicable for older projects.	1'b0
0x544	vesc_reg15[31:1]	Reserved	31'b0

4.5.13 Latency Tolerance Reporting Capability

Latency Tolerance Reporting (LTR) Capability is an Extended Capability that allows software to provide platform latency information to components with Upstream Ports. This capability is implemented in Upstream Port and Embedded endpoint.

Figure 70 details the structure of register fields for LTR capability registers andTable 153 describes the registers' fields.

Figure 70. LTR Registers

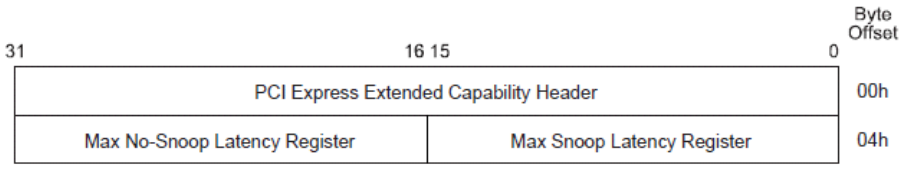


Table 153. LTR Capability Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x600	LTR_CAP_0	31:0	PCI Express Enhance Capability Header	RO	32'h00010018
0x604	LTR_CAP_1	15:0	Max Snoop Latency Register	R/W	0
0x604	LTR_CAP_1	31:16	Max Snoop Latency Register	R/W	0

4.5.14 Secondary PCIE Extended Capability

The Secondary PCIE Extended Capaility structure is required in all Ports that supports Gen3.

Figure 71 details the structure of register fields for Secondary PCIE registers and Table 154 describes the registers' fields.

Figure 71. Secondary PCIE Registers

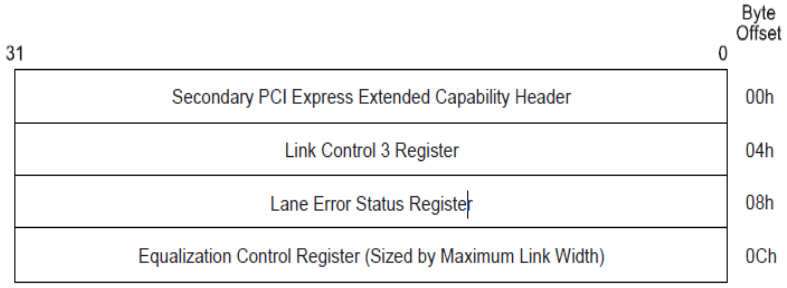


Table 154. LTR Capability Registers Fields

Offset	Register Name	Bit(s)	Field Name and Description	Type	Default Value
0x700	SPCIE_CAP_0	31:0	PCI Express Enhance Capability Header	RO	32'h00010018
0x704	SPCIE_CAP_1	15:0	Max Snoop Latency Register	R/W	0
0x704	SPCIE_CAP_1	31:16	Max Snoop Latency Register	R/W	0

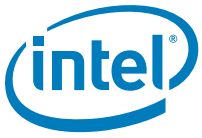
4.6 Display Port Registers

Vendor space registers of re-driver DP Source ports can be accessed through the DP-In port configuration space. In fact, DP-In CIO ports have two sets of vendor specific registers - the first one contains the registers of the re-driver Source port, while the second one (chained through the next-capability pointer of the first one) contains the register of the Sink port. These two vendor register spaces have the same Capability ID (0x5) and different VSEC-ID: 0x1 for Source vendor register space and 0x0 for Sink vendor register space. In Alpine-Ridge DP for example, Source-A vendor registers start at offset 0x3E of Port 9 configuration space, while Sink-0 vendor register space starts at offset 0x7B (of the same CIO Port 9). CIO Port 8 (DP-Out) contains only one vendor register space with the registers of Source-0 - its VSEC-ID is 0x1.

4.6.1 Receiver

The display port receiver uses a 13 bit address space for internal register access. This address space is divided into several separate banks, as defined in the following list. When accessed through Jtag "by 8051", that's the addresses that should be used (plus 3 MSbits (16 bits in total) that identify the accessed port - 0/1/2/3/4 for src0/snk0/snk1/src_pa/src_pb, respectively). When accessed by a target access (indirectly through DP Vendor capability space) the below addresses should be logically OR'ed with 0xC000, e.g. the base address of Bank 1 is 0xC200.

- 0x0200 Bank 1 - Framer - Framer of Display Port, receive.
- 0x0400 Bank2 - Reserved.
- 0x0600 Bank 3 - Physical Layer - PHY of Display Port, receive.
- 0x0800 Bank4 - Miscellaneous 2.
- 0x0A00 Bank 5 - Auxiliary - Auxiliary of Display Port, receive.
- 0x0C00 Bank 6 - Miscellaneous - hpd, error counters, MISC registers, configuration.
- 0x0E00 Bank 7 - Analog Interface.



- 0x1600 Bank 11 - Phy Digital Lane
- 0x1800 Bank 12 - Phy Digital Common

The following sections define the registers used in each bank. The real address of a register is the register number + bank offset.

4.6.1.1 Bank 1 - Framer

Table 155 is a summary of the Framer registers without registers description. The detailed description of the register list is given in the following sections. When Sink operates in redriver mode, the only accessible register is RX_FRAMER_CONFIG_REG.

Table 155. 0x200 Framer Registers Summary

Register Number	Register Name	Section #
0	RX_FRAMER_CONFIG_REG	"RX_FRAMER_CONFIG_REG" on page 376

4.6.1.1.1 RX_FRAMER_CONFIG_REG

Configuration register.

Offset	Bit(s)	Field Name	Description	Type	Default Value
0	7:4	Reserved	Reserved	RO	0
0	3	rx_framer_cio_mask	Selection of either masking the outputs to the CIO interface, or not. '0' = normal operation with no mask, '1' = outputs to CIO interface are masked. This bit has no effect in DP Tunneling mode	R/W	0
0	2:1	rx_framer_training_sel	Selection of training modes checker or normal operation.This bit has no effect	R/W	2'b1
0	0	rx_framer_en	RX framer block enable. This bit has no effect	R/W	1

4.6.1.2 Bank 3 - PHY Layer

Table 156 is a summary of the PHY Layer registers without registers description. The detailed description of the register list is given in the following sections.

Table 156. 0x600 PHY Layer Registers Summary

Register Number	Register Name	Section #
0	PHY_CONFIG_0	"PHY_CONFIG_0" on page 378
1	PHY_CONFIG_1	"PHY_CONFIG_1" on page 378
2	PHY_CONFIG_2	"PHY_CONFIG_2" on page 378
3	PHY_CONFIG_3	"PHY_CONFIG_3" on page 378

Table 156. 0x600 PHY Layer Registers Summary

Register Number	Register Name	Section #
4	PHY_CONFIG_4	“PHY_ CONFIG_4” on page 378
5	PHY_CONFIG_5	“PHY_ CONFIG_5” on page 379
6	PHY_CONFIG_6	“PHY_ CONFIG_6” on page 379
7	PHY_CONFIG_7	“PHY_ CONFIG_7” on page 379

4.6.1.2.1 PHY_CONFIG_0

Offset	Bit(s)	Field Name	Description	Type	Default Value
0	7	hard_decision	When equal number of detected and undetected SR: 1 - undetected wins 0 - detected wins	R/W	0
0	5	align_en	Enables sync state machine to align data: 1 - enable sync 0 - disable sync	R/W	0
0	6	disable_detection	Disables SR majority voting: 1 - disable majority voting 0 - enable majority voting	R/W	0
0	4	deskew_bypass	1 - bypass skew block 0 - normal mode	R/W	0
0	3:2	Reserved	Reserved	RO	0
0	1	keep_special	For all lanes: 1 - keep special character when decoder error 0 - delete special character when decoder error	R/W	0
0	0	scrambler_bypass	For all lanes: 1 - scramble bypass 0 - normal mode	R/W	0

4.6.1.2.2 PHY_CONFIG_1

Offset	Bit(s)	Field Name	Description	Type	Default Value
1	7:5	Reserved	Reserved	RO	0
1	4	deskew_enable	Enables deskew by management: 1 - enable 0 - normal	R/W	0
1	3:0	enable_cgalign	Enables code alignment by management: 1 - enable 0 - normal	R/W	0

4.6.1.2.3 PHY_CONFIG_2

Offset	Bit(s)	Field Name	Description	Type	Default Value
2	7:4	Reserved	Reserved	RO	0
	3:0	disable_filter	Disable SR filter in enhanced mode lane: 1 - disable filter 0 - enable filter	R/W	0000

4.6.1.2.4 PHY_CONFIG_3

Offset	Bit(s)	Field Name	Description	Type	Default Value
3	7:0	Reserved	Reserved	RO	0

4.6.1.2.5 PHY_ CONFIG_4

Offset	Bit(s)	Field Name	Description	Type	Default Value
4	7	Reserved	Reserved	RO	0

4	6:4	lane_count1	Diagnostic: Relative skew of lane1 ready when deskew_done is high.	RO	0
4	3	Reserved	Reserved	RO	0
4	2:0	lane_count0	Diagnostic: Relative skew of lane0 ready when deskew_done is high.	RO	0

4.6.1.2.6 PHY_ CONFIG_5

Offset	Bit(s)	Field Name	Description	Type	Default Value
5	7	Reserved	Reserved	RO	0
5	6:4	lane_count3	Diagnostic: Relative skew of lane3 ready when deskew_done is high.	RO	0
5	3	Reserved	Reserved	RO	0
5	2:0	lane_count2	Diagnostic: Relative skew of lane2 ready when deskew_done is high.	RO	0

4.6.1.2.7 PHY_ CONFIG_6

Offset	Bit(s)	Field Name	Description	Type	Default Value
6	7:6	Reserved	Reserved	RO	0
6	5	deskew_error	1 - deskew error 0 - no error	RO	0
6	4	deskew_done	1 - deskew done 0 - deskew undone	RO	0
6	3:0	sync_acquired	Diagnostic: 1 - lane sync 0 - no sync	RO	0

4.6.1.2.8 PHY_ CONFIG_7

Offset	Bit(s)	Field Name	Description	Type	Default Value
7	7:0	Reserved	Reserved	RO	0

4.6.1.3 Bank 4 - Miscellaneous-2

Table 157 provides a summary of the Misc2 registers without registers description. The detailed description of the register list is given in the following sections.

Table 157. 0x800 Misc2 Registers Summary

Register Number	Register Name	Section #
0	MODE	“Mode” on page 382
1	IDENTITY	“Identity” on page 382
2	DP_STATUS	“DP Status” on page 382
3	HDMI_STATUS	“HDMI Status” on page 382
4	HDP_CTRL_0	“HDP_CTRL_0” on page 382
5	HDP_CTRL_1	“HDP_CTRL_1” on page 383

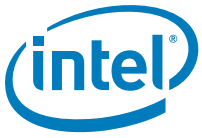


Table 157. 0x800 Misc2 Registers Summary

Register Number	Register Name	Section #
6	HDP_CTRL_2	"HDP_CTRL_2" on page 383
7	HDP_CTRL_3	"HDP_CTRL_3" on page 383
8	GENREG0	"GENREG 0" on page 383
9	GENREG1	"GENREG 1" on page 383
10	GENREG2	"GENREG 2" on page 383
11	GENREG3	"GENREG 3" on page 384
15	CAR_CONTROL	"CAR CTRL" on page 384
16	TAR_CTRL_0	"TAR_CTRL_0" on page 384
17	TAR_CTRL_1	"TAR_CTRL_1" on page 384
18	TAR_CTRL_2	"TAR_CTRL_2" on page 384
19	TAR_CTRL_3	"TAR_CTRL_3" on page 384
20	TAR_WR_DATA_0	"TAR_WR_DATA 0" on page 385
21	TAR_WR_DATA_1	"TAR_WR_DATA 1" on page 385
22	TAR_WR_DATA_2	"TAR_WR_DATA 2" on page 385
23	TAR_WR_DATA_3	"TAR_WR_DATA 3" on page 385
24	TAR_RD_DATA_0	"TAR_RD_DATA 0" on page 385
25	TAR_RD_DATA_1	"TAR_ RD _DATA 1" on page 385
26	TAR_RD_DATA_2	"TAR_ RD _DATA 2" on page 385
27	TAR_RD_DATA_3	"TAR_ RD _DATA 3" on page 386
32	EE_CTRL	"EE_CTRL" on page 386
33	EE_ADDR_0	"EE_ADDR 0" on page 386
34	EE_ADDR_1	"EE_ADDR 1" on page 386
35	EE_RD_DATA_0	"EE_RD_DATA 0" on page 386
36	EE_RD_DATA_1	"EE_ RD _DATA 1" on page 386
37	EE_RD_DATA_2	"EE_ RD _DATA 2" on page 386
38	EE_RD_DATA_3	"EE_ RD _DATA 3" on page 386
40	VSPE_INIT0	"VSPE_INIT 0" on page 386
41	VSPE_INIT1	"VSPE_INIT 1" on page 386
42	VSPE_INIT2	"VSPE_INIT 2" on page 387
43	VSPE_INIT3	"VSPE_INIT 3" on page 387
44	EE2TAR_LOAD_DONE	"EE2TAR_LOAD_DONE" on page 387
48	SELF_BASE_ADDR_LO	"ELF_BASE_ADDR_LO" on page 387
49	SELF_BASE_ADDR_HI	"SELF_BASE_ADDR_HI" on page 387
52	PRTN_BASE_ADDR_LO	"PRTN_BASE_ADDR_LO" on page 387
53	PRTN_BASE_ADDR_HI	"PRTN_BASE_ADDR_HI" on page 387
54	PRTN_PORT_ID	"PRTN_PORT_ID" on page 388
56	ANA_ADDR_IDX_LO	"ANA_ADDR_IDX_LO" on page 388
57	ANA_ADDR_IDX_HI	"NA_ADDR_IDX_HI" on page 388
58	ANA_DATA_IDX_LO	"NA_ADDR_IDX_HI" on page 388
59	ANA_DATA_IDX_HI	"ANA_DATA_IDX_HI" on page 388
60	PRTN_ANA_ADDR_IDX_LO	"PRTN_ANA_ADDR_IDX_LO" on page 388
61	PRTN_ANA_ADDR_IDX_HI	"PRTN_ANA_ADDR_IDX_HI" on page 388

Table 157. 0x800 Misc2 Registers Summary

Register Number	Register Name	Section #
62	PRTN_ANA_DATA_IDX_LO	"PRTN_ANA_DATA_IDX_LO" on page 389
63	PRTN_ANA_DATA_IDX_HI	"PRTN_ANA_DATA_IDX_HI" on page 389
64	SYNC_FIFO_VIOL	"SYNC_FIFO_VIOL" on page 389
65	CRUX_FIFO_VIOL	"CRUX_FIFO_VIOL" on page 389
72	HPD_UNPLG_ON_START	"HPD_UNPLG_ON_START" on page 389
73	CHICKEN0	"CHICKEN0" on page 389
74	EE_GP_CFG2	"EE_GP_CFG2" on page 389
75	EE_GP_CFG3	"EE_GP_CFG3" on page 389
76	EE_REGION_ADDR0	"EE_REGION_ADDR0" on page 390
77	EE_REGION_ADDR1	"EE_REGION_ADDR1" on page 390
78	EE_REGION_ADDR2	"EE_REGION_ADDR2" on page 390
80	DFT	"DFT" on page 390
81	DFT2	"DFT2" on page 390
96	DP_STATUS_1	"DP_STATUS_1" on page 390
97	DP_STATUS_2	"DP_STATUS_2" on page 390
98	DP_CTRL_0	"DP_CTRL_0" on page 390
99	DP_CTRL_1	"DP_CTRL_1" on page 391
100	SYMB_PTTRN_1st	"SYMB_PTTRN_1st" on page 391
101	SYMB_PTTRN_2nd	"SYMB_PTTRN_2nd" on page 391
102	DESKEW_PTTRN_1st	"DESKEW_PTTRN_1st" on page 391
103	DESKEW_PTTRN_2nd	"DESKEW_PTTRN_2nd" on page 391
104	HI_BITS_PTTRN	"HI_BITS_PTTRN" on page 392
105	DP_ERR_WGHT	"DP_ERR_WGHT" on page 392
106	DP_NON_ERR_WGHT	"DP_NON_ERR_WGHT" on page 392
107	DP_ERR_THRSH	"DP_ERR_THRSH" on page 392
112	TST_PTTRN_CTRL_0	"TST_PTTRN_CTRL_0" on page 392
113	TST_PTTRN_CTRL_1	"TST_PTTRN_CTRL_1" on page 392
114	TST_PTTRN_CTRL_2	"TST_PTTRN_CTRL_2" on page 393
115	TST_PTTRN_K	"TST_PTTRN_K" on page 393
116	TST_PTTRN_BS_0	"TST_PTTRN_BS_0" on page 393
117	TST_PTTRN_BS_1	"TST_PTTRN_BS_1" on page 393
118	TST_PTTRN_BS_2	"TST_PTTRN_BS_2" on page 393
119	TST_PTTRN_BS_3	"TST_PTTRN_BS_3" on page 393
120	TST_PTTRN_SR_0	"TST_PTTRN_SR_0" on page 393
121	TST_PTTRN_SR_1	"TST_PTTRN_SR_1" on page 393
122	TST_PTTRN_SR_2	"TST_PTTRN_SR_2" on page 393
123	TST_PTTRN_SR_3	"TST_PTTRN_SR_3" on page 394
124	TST_PTTRN_BS_RATIO_0	"TST_PTTRN_BS_RATIO_0" on page 394
125	TST_PTTRN_BS_RATIO_1	"TST_PTTRN_BS_RATIO_1" on page 394
126	TST_PTTRN_SR_RATIO_0	"TST_PTTRN_SR_RATIO_0" on page 394
127	TST_PTTRN_SR_RATIO_1	"TST_PTTRN_SR_RATIO_1" on page 394
128	TST_PTTRN_SR_SYMB_0	"TST_PTTRN_SR_SYMB_0" on page 394
129	TST_PTTRN_SR_SYMB_1	"TST_PTTRN_SR_SYMB_1" on page 394
130	TST_PTTRN_SR_SYMB_2	"TST_PTTRN_SR_SYMB_2" on page 395

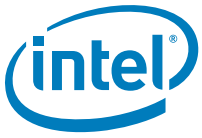


Table 157. 0x800 Misc2 Registers Summary

Register Number	Register Name	Section #
151	AUX_PHY_CTRL	"AUX_PHY_CTRL" on page 395

4.6.1.3.1 Mode

Offset	Bit(s)	Field Name	Description	Type	Default Value
0	7	Redriv_en	Current redriver/tunneling mode: 0 – Tunneling 1 – Redriver	RO	0
0	6:3	reserved	reserved	RO	0
0	2:1	Redriv_partner	Current partner (valid only in redriver mode): 0 - Source 0 1 - Source A 2 - Source B		
0	0	HDMI1_DP0	Current HDP mode: 0 – DP 1 – HDMI **HDP In/Out bypass mode** HDP IN -> OUT HDMI bypass enable	RO	0

4.6.1.3.2 Identity

Offset	Bit(s)	Field Name	Description	Type	Default Value
1	7	Redriv_en	Current mode: 0 – Tunneling 1 – Redriver	RO	0
1	6:1	Reserved	Reserved	RO	0
1	0	Port_ID	CIO Port ID of this Sink.	RO	0

4.6.1.3.3 DP Status

Offset	Bit(s)	Field Name	Description	Type	Default Value
2	7:4	Rx_locked	Rx locked indication for each one of the lanes.	RO	0
2	3:0	DP_poor_signal	Poor signal indication for each one of the lanes.	RO	0

4.6.1.3.4 HDMI Status

Offset	Bit(s)	Field Name	Description	Type	Default Value
3	7	crux_hdpcmn_ready	Sync FIFO between Sink and Source is active. (write and read clocks are valid)	RO	0
3	6:0	reserved	Reserved	RO	0

4.6.1.3.5 HDP_CTRL_0

Offset	Bit(s)	Field Name	Description	Type	Default Value
4	7	force_hpd_lo_n	While 0 HPD is driven low.	RO	0
4	6:3	reserved	reserved	RO	0
4	2:0	DP_state	0 – Pre link training 1 – TPS1 2 – TPS2 3 – TPS3 4 – Post link training	RO	0

4.6.1.3.6 HDP_CTRL_1

Offset	Bit(s)	Field Name	Description	Type	Default Value
5	7:3	reserved	reserved	RO	0
5	2	aux_extra_info_dis	Enable extra info sent between dp_in and dp_out along with AUX packet. (used to correspond responses to requests and to transfer GTC indication)	RW	1
5	1	Sync_en	Enable synchronization of DP lanes to a common rx_clk. (Not relevant in Alpine-Ridge DP)	RO	0
5	0	Link_init	Initiate link drop on Source side. (similar to adapter error detection in DP_Out)	RO	0

4.6.1.3.7 HDP_CTRL_2

Offset	Bit(s)	Field Name	Description	Type	Default Value
6	7:2	TPS_ERR_THRESH	Number of acceptable consecutive mismatches of TPS before symbol relock is initiated.	R/W	4
6	1	LL_bypass	Bypass Link Layer. Rx Phy data (10b per lane) received in Sink is bypassing Link Layer logic and driven to Tx Phy. (it is only synchronized to the common rx_clk in the Sink and then to tx_clk in the Source)	R/W	0
6	0	Leg_Phy_en	Legacy logic is used when this bit is set.	R/W	1

4.6.1.3.8 HDP_CTRL_3

Offset	Bit(s)	Field Name	Description	Type	Default Value
6	7:3	reserved	reserved	RO	0
6	2	gtc_freq_off_restart	GTC Freq offset calculation restart		
6	1	gtc_init_n	Digital reset of GTC Calc unit		
6	0	reserved	reserved	RO	0

4.6.1.3.9 GENREG 0

Offset	Bit(s)	Field Name	Description	Type	Default Value
8	7:0	gp_reg0	General purpose register	R/W	0

4.6.1.3.10 GENREG 1

Offset	Bit(s)	Field Name	Description	Type	Default Value

9	7:0	gp_reg1	General purpose register	R/W	0

4.6.1.3.11 GENREG 2

Offset	Bit(s)	Field Name	Description	Type	Default Value
10	7:0	gp_reg2	General purpose register	R/W	0

4.6.1.3.12 GENREG 3

Offset	Bit(s)	Field Name	Description	Type	Default Value
11	7:0	gp_reg3	General purpose register	R/W	0

4.6.1.3.13 CAR CTRL

Offset	Bit(s)	Field Name	Description	Type	Default Value
15	7	frc_uctl_rst	When set to '1', holds 8051 in reset	R/W	0
15	6	reserved	reserved	R/W	0
15	5	frc_hdp_in_ll_clk_en	When set to '1' it ungates HDP clock in the crux.	R/W	0
15	4	frc_hd_in_ll_clk_en	When set to '1' it ungates HDMI clock in the Sink**HDP In/Out bypass mode** HDP IN -> OUT HDMI bypass enable	R/W	0
15	3	frc_adpt_in_en	When set to '1' it ungates DP clock in DP_In adapter	R/W	0
15	2	frc_cmn_dp_in_en	When set to '1' it ungates DP clock in the Sink	R/W	0
15	1	frc_snk_rxX_clk_gate_ctl	When set to '1' it controls the gating of rxX_clk's. (otherwise it is according to rx_locked indication)	R/W	1
15	0	frc_snk_rxX_clk_gate_val	When frc_snk_rxX_clk_gate_ctl is '1' rxX_clk's are gated or not according to this value.	R/W	0

4.6.1.3.14 TAR_CTRL_0

Offset	Bit(s)	Field Name	Description	Type	Default Value
16	7:0	hdp_tar_dw_index[7:0]	The lower byte of tar_dw_index used when the Sink is mastering the target access.	R/W	0

4.6.1.3.15 TAR_CTRL_1

Offset	Bit(s)	Field Name	Description	Type	Default Value
17	7:5	reserved	reserved	RO	0
17	4:0	hdp_tar_dw_index[12:8]	The upper 5 bits of tar_dw_index used when the Sink is mastering the target access.	R/W	0

4.6.1.3.16 TAR_CTRL_2

Offset	Bit(s)	Field Name	Description	Type	Default Value
18	7:6	hdp_tar_cs[1:0]	tar_cs[1:0] used when the Sink is mastering the target access.	R/W	0
18	5:0	hdp_tar_port[5:0]	tar_port[5:0] used when the Sink is mastering the target access.	R/W	0

4.6.1.3.17 TAR_CTRL_3

Offset	Bit(s)	Field Name	Description	Type	Default Value
19	7	hdp_tar_valid	Setting to '1' activates HDP master target access. Self cleared when the access completes.	R/W	0
19	6:3	reserved	reserved	RO	0
19	2	hdp_pcie_sw_regs_access	pcie_sw_regs_access used when the Sink is mastering the target access.		
19	1	hdp_cio_sw_regs_access	cio_sw_regs_access used when the Sink is mastering the target access.		
19	0	hdp_tar_wr1_rd0	tar_wr1_rd0 used when the Sink is mastering the target access.	R/W	0

4.6.1.3.18 TAR_WR_DATA 0

Offset	Bit(s)	Field Name	Description	Type	Default Value
20	7:0	hdp_tar_wr_data[7:0]	tar_wr_data[7:0] used when the Sink is mastering the target access.	R/W	0

4.6.1.3.19 TAR_WR_DATA 1

Offset	Bit(s)	Field Name	Description	Type	Default Value
21	7:0	hdp_tar_wr_data[15:8]	tar_wr_data[15:8] used when the Sink is mastering the target access.	R/W	0

4.6.1.3.20 TAR_WR_DATA 2

Offset	Bit(s)	Field Name	Description	Type	Default Value
22	7:0	hdp_tar_wr_data[23:16]	tar_wr_data[23:16] used when the Sink is mastering the target access.	R/W	0

4.6.1.3.21 TAR_WR_DATA 3

Offset	Bit(s)	Field Name	Description	Type	Default Value
23	7:0	hdp_tar_wr_data[31:24]	tar_wr_data[31:24] used when the Sink is mastering the target access.	R/W	0

4.6.1.3.22 TAR_RD_DATA 0

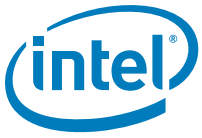
Offset	Bit(s)	Field Name	Description	Type	Default Value
24	7:0	tar_hdp_rd_data_latched[7:0]	Latches tar_ rd_data[7:0] when read access by HDP is accomplished.	RO	0

4.6.1.3.23 TAR_ RD _DATA 1

Offset	Bit(s)	Field Name	Description	Type	Default Value
25	7:0	tar_hdp_rd_data_latched [15:8]	Latches tar_ rd_data[15:8] when read access by HDP is accomplished.	RO	0

4.6.1.3.24 TAR_ RD _DATA 2

Offset	Bit(s)	Field Name	Description	Type	Default Value
26	7:0	tar_hdp_rd_data_latched [23:16]	Latches tar_ rd_data[23:16] when read access by HDP is accomplished.	RO	0



4.6.1.3.25 TAR_ RD _DATA 3

Offset	Bit(s)	Field Name	Description	Type	Default Value
27	7:0	tar_hdp_rd_data_latched [31:24]	Latches tar_ rd_data[31:24] when read access by HDP is accomplished.	RO	0

4.6.1.3.26 EE_CTRL

Offset	Bit(s)	Field Name	Description	Type	Default Value
32	7	hdp_ee_rd	When set, HDP FLASH access is initiated.	R/W	0
32	6:0	reserved	reserved	RO	0

4.6.1.3.27 EE_ADDR 0

Offset	Bit(s)	Field Name	Description	Type	Default Value
33	7:0	hdp_ee_rd_addr[7:0]	HDP FLASH address low.	R/W	0

4.6.1.3.28 EE_ADDR 1

Offset	Bit(s)	Field Name	Description	Type	Default Value
34	7:0	hdp_ee_rd_addr[15:8]	HDP FLASH address high.	R/W	0

4.6.1.3.29 EE_RD_DATA 0

Offset	Bit(s)	Field Name	Description	Type	Default Value
35	7:0	ee_hdp_data_latched[7:0]	Latches ee_data[7:0] when read access by HDP is accomplished.	RO	0

4.6.1.3.30 EE_ RD _DATA 1

Offset	Bit(s)	Field Name	Description	Type	Default Value
36	7:0	ee_hdp_data_latched[15:0]	Latches ee_data[15:8] when read access by HDP is accomplished.	RO	0

4.6.1.3.31 EE_ RD _DATA 2

Offset	Bit(s)	Field Name	Description	Type	Default Value
37	7:0	ee_hdp_data_latched[23:16]	Latches ee_data[23:16] when read access by HDP is accomplished.	RO	0

4.6.1.3.32 EE_ RD _DATA 3

Offset	Bit(s)	Field Name	Description	Type	Default Value
38	7:0	ee_hdp_data_latched[31:24]	Latches ee_data[31:24] when read access by HDP is accomplished.	RO	0

4.6.1.3.33 VSPE_INIT 0

Offset	Bit(s)	Field Name	Description	Type	Default Value
40	7:4	VSPE_1p62	ee_dp_in_init_preemph[1:0] ee_dp_in_init_swing[1:0]	RO	0
40	3:0	VSPE_1p62	ee_dp_in_init_preemph[1:0] ee_dp_in_init_swing[1:0]	RO	0

4.6.1.3.34 VSPE_INIT 1

Offset	Bit(s)	Field Name	Description	Type	Default Value

41	7:4	VSPE_2p7	ee_dp_in_init_preemph[3:2] ee_dp_in_init_swing[3:2]	RO	0
41	3:0	VSPE_2p7	ee_dp_in_init_preemph[3:2] ee_dp_in_init_swing[3:2]	RO	0

4.6.1.3.35 VSPE_INIT 2

Offset	Bit(s)	Field Name	Description	Type	Default Value
42	7:4	VSPE_5p4	ee_dp_in_init_preemph[5:4] ee_dp_in_init_swing[5:4]	RO	0
42	3:0	VSPE_5p4	ee_dp_in_init_preemph[5:4] ee_dp_in_init_swing[5:4]	RO	0

4.6.1.3.36 VSPE_INIT 3

Offset	Bit(s)	Field Name	Description	Type	Default Value
43	7:4	reserved	ee_dp_in_init_preemph[7:6] ee_dp_in_init_swing[7:6]	RO	0
43	3:0	reserved	ee_dp_in_init_preemph[7:6] ee_dp_in_init_swing[7:6]	RO	0

4.6.1.3.37 EE2TAR_LOAD_DONE

Offset	Bit(s)	Field Name	Description	Type	Default Value
44	7:1	reserved	reserved	RO	0
44	0	reserved	ee_to_tar_dp_domain_done	RO	0

4.6.1.3.38 ELF_BASE_ADDR_LO

Offset	Bit(s)	Field Name	Description	Type	Default Value
48	7:0	self_base_addr[7:0]	The offset to its own vendor register space in the Port configuration space.	RO	0

4.6.1.3.39 SELF_BASE_ADDR_HI

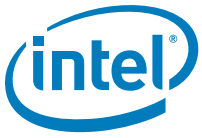
Offset	Bit(s)	Field Name	Description	Type	Default Value
49	7:4	reserved	reserved	RO	0
49	3:0	self_base_addr[12:8]	The offset to its own vendor register space in the Port configuration space.	RO	0

4.6.1.3.40 PRTN_BASE_ADDR_LO

Offset	Bit(s)	Field Name	Description	Type	Default Value
52	7:0	partner_base_addr[7:0]	The offset to the partner's vendor register space in the Port configuration space.	RO	0

4.6.1.3.41 PRTN_BASE_ADDR_HI

Offset	Bit(s)	Field Name	Description	Type	Default Value
53	7:4	reserved	reserved	RO	0
53	3:0	partner_base_addr[12:8]	The offset to the partner's vendor register space in the Port configuration space.	RO	0



4.6.1.3.42 PRTN_PORT_ID

Offset	Bit(s)	Field Name	Description	Type	Default Value
54	7:6	reserved	reserved	RO	0
54	5:0	partner_port_id	The partner's Port ID.	RO	0

4.6.1.3.43 ANA_ADDR_IDX_LO

Offset	Bit(s)	Field Name	Description	Type	Default Value
56	7:0	ana_addr_index[7:0]	The address of the register that contains the offset in the analog register space. (for indirect access into the analog register space)	RO	0

4.6.1.3.44 NA_ADDR_IDX_HI

Offset	Bit(s)	Field Name	Description	Type	Default Value
57	7:4	reserved	reserved	RO	0
57	3:0	ana_addr_index[12:8]	The address of the register that contains the offset in the analog register space. (for indirect access into the analog register space)	RO	0

4.6.1.3.45 ANA_DATA_IDX_LO

Offset	Bit(s)	Field Name	Description	Type	Default Value
58	7:0	ana_data_index[7:0]	The address of the register that contains the data of the analog register space. (for indirect access into the analog register space)	RO	0

4.6.1.3.46 ANA_DATA_IDX_HI

Offset	Bit(s)	Field Name	Description	Type	Default Value
59	7:4	reserved	reserved	RO	0
59	3:0	ana_data_index[12:8]	The address of the register that contains the data of the analog register space. (for indirect access into the analog register space)	RO	0

4.6.1.3.47 PRTN_ANA_ADDR_IDX_LO

Offset	Bit(s)	Field Name	Description	Type	Default Value
60	7:0	partner_ana_addr_index[7:0]	The address of the register that contains the offset in the partner's analog register space. (for indirect access into the partner's analog register space)	RO	0

4.6.1.3.48 PRTN_ANA_ADDR_IDX_HI

Offset	Bit(s)	Field Name	Description	Type	Default Value
61	7:4	reserved	reserved	RO	0
61	3:0	partner_ana_addr_index[12:8]	The address of the register that contains the offset in the partner's analog register space. (for indirect access into the partner's analog register space)	RO	0

4.6.1.3.49 PRTN_ANA_DATA_IDX_LO

Offset	Bit(s)	Field Name	Description	Type	Default Value
62	7:0	partner_ana_data_index[7:0]	The address of the register that contains the data of the partner's analog register space. (for indirect access into the partner's analog register space)	RO	0

4.6.1.3.50 PRTN_ANA_DATA_IDX_HI

Offset	Bit(s)	Field Name	Description	Type	Default Value
63	7:4	reserved	reserved	RO	0
63	3:0	partner_ana_data_index[12:8]	The address of the register that contains the data of the partner's analog register space. (for indirect access into the partner's analog register space)	RO	0

4.6.1.3.51 SYNC_FIFO_VIOL

Offset	Bit(s)	Field Name	Description	Type	Default Value
64	7:4	sync_fifo_full	Sync FIFO full indication (per lane). Cleared on write.	RO	0
64	3:0	sync_fifo_empty	Sync FIFO empty indication (per lane). Cleared on write.	RO	0

4.6.1.3.52 CRUX_FIFO_VIOL

Offset	Bit(s)	Field Name	Description	Type	Default Value
65	7:2	reserved	reserved	RO	0
65	1	crux_fifo_full	Crux FIFO full indication. Cleared on write.	RO	0
65	0	crux_fifo_empty	Crux FIFO empty indication. Cleared on write.	RO	0

4.6.1.3.53 HPD_UNPLG_ON_START

Offset	Bit(s)	Field Name	Description	Type	Default Value
72	7:0	HPD_UNPLG_ON_START	ee_hdp_in_gp_cfg0	RO	from flash address 0x8e

4.6.1.3.54 CHICKEN0

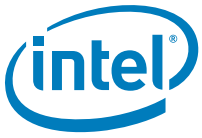
Offset	Bit(s)	Field Name	Description	Type	Default Value
73	7:0	CHICKEN0	ee_hdp_in_gp_cfg1	RO	0

4.6.1.3.55 EE_GP_CFG2

Offset	Bit(s)	Field Name	Description	Type	Default Value
74	7:0	EE_GP_CFG2	ee_hdp_in_gp_cfg2	RO	0

4.6.1.3.56 EE_GP_CFG3

Offset	Bit(s)	Field Name	Description	Type	Default Value
75	0		forces DP_IN FW to an eternal loop before waiting for HPD. Can be released by writing register 0xCC92 to value > 3 ([3:1] cause eternal loop in other places)		
75	7:1	EE_GP_CFG3	ee_hdp_in_gp_cfg3	RO	0



4.6.1.3.57 EE_REGION_ADDR0

Offset	Bit(s)	Field Name	Description	Type	Default Value
76	7:0	EE_REGION_ADDR0	ee_hdp_in_region_addr0	RO	0

4.6.1.3.58 EE_REGION_ADDR1

Offset	Bit(s)	Field Name	Description	Type	Default Value
77	7:0	EE_REGION_ADDR1	ee_hdp_in_region_addr1	RO	0

4.6.1.3.59 EE_REGION_ADDR2

Offset	Bit(s)	Field Name	Description	Type	Default Value
78	7:0	EE_REGION_ADDR2	ee_hdp_in_region_addr2	RO	0

4.6.1.3.60 DFT

Offset	Bit(s)	Field Name	Description	Type	Default Value
80	7:2	reserved	reserved	RO	0
80	2	fast_count	Speed up various timers. (for simulation only)	R/W	0
80	1	quick_link	Speed up link establishment. (for simulation only)	R/W	0

4.6.1.3.61 DFT2

Offset	Bit(s)	Field Name	Description	Type	Default Value
81	7:0	printf	FW uses this register to printf its current location.	RO	0

4.6.1.3.62 DP_STATUS_1

Offset	Bit(s)	Field Name	Description	Type	Default Value
96	7:6	reserved		RO	0
96	5	SYNC_DONE	All of the active lanes locked and synchronized to one common clock (usually the clock of lane-0)	RO	
96	4	DESKEW_DONE	De-skew between the active lanes accomplished	RO	
96	3:0	TPS_FOUND	TPS found (per lane)	RO	0

4.6.1.3.63 DP_STATUS_2

Offset	Bit(s)	Field Name	Description	Type	Default Value
97	7:4	SYMB_LOCK_STABLE	Symbol locked (per lane)	RO	0
97	3:0	TPS_FOUND	TPS found (per lane)	RO	0

4.6.1.3.64 DP_CTRL_0

Offset	Bit(s)	Field Name	Description	Type	Default Value
98	7:6	fw_dsk_pttrn_mask	Mask for de-skew pattern	R/W	0x0
98	5	frc_dsk_pttrn_mask	If set to '1' use fw_dsk_pttrn_mask[1:0] to mask the second/first deskew pattern while looking for a deskewing point on each lane. (otherwise both symbols define the de-skewing reference point)	R/W	0
98	4	frc_dsk_pttrn	Force the reference de-skewing point to be according to {DESKEW_PTTRN_2nd, DESKEW_PTTRN_1st} (otherwise it's {D11.6,D10.2} in case of TPS2, and {K28.5,D10.2} in case of TPS3)	R/W	0

98	3	frc_symb_pttrn	Force the reference symbol for locking to be SYMB_PTTRN_1st and SYMB_PTTRN_2nd. (otherwise it's K28.5)	R/W	0
98	2	frc_redeskew	Causes de-skew mechanism to restart	R/W	0
98	1	frc_symb_relock	Causes symbol lock mechanism to restart	R/W	0
98	0	frc_symb_lock_en	Allows to enable symbol lock mechanism not only during training	R/W	0

4.6.1.3.65 DP_CTRL_1

Offset	Bit(s)	Field Name	Description	Type	Default Value
99	7:5	reserved		RO	0
99	4:3	frc_symb_relock_mask	[0] – masks relock as result of incorrect TPS [1] – masks relock as result of decoding/ disparity errors	R/W	0x1
99	2	frc_err_filt_en	Enable error filtering – if enabled, too many consecutive errors will trigger symbol relocking. (this mechanism is always enabled in most training state, but can be masked using frc_symb_relock_mask[1])	R/W	0
99	1:0	frc_symb_pttrn_mask	When set to '1' it masks the second/first symbol lock pattern while the symbol on each lane. (otherwise both symbols are used as a locking pattern)	R/W	0x0

4.6.1.3.66 SYMB_PTTRN_1st

Offset	Bit(s)	Field Name	Description	Type	Default Value
100	7:0	fw_symb_pattern1[7:0]	1st pattern used as a reference for symbol lock	R/W	0xFA

4.6.1.3.67 SYMB_PTTRN_2nd

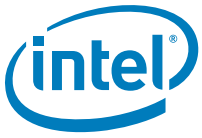
Offset	Bit(s)	Field Name	Description	Type	Default Value
101	7:0	fw_symb_pattern2[7:0]	2nd pattern used as a reference for symbol lock	R/W	0x05

4.6.1.3.68 DESKEW_PTTRN_1st

Offset	Bit(s)	Field Name	Description	Type	Default Value
102	7:0	fw_desk_pattern[7:0]	Pattern used while searching de-skewing point between the lanes. (two symbols in 1+8b format)	R/W	0x4A

4.6.1.3.69 DESKEW_PTTRN_2nd

Offset	Bit(s)	Field Name	Description	Type	Default Value
103	7:0	fw_desk_pattern[16:9]	Pattern used while searching de-skewing point between the lanes. (two symbols in 1+8b format)	R/W	0xBC



4.6.1.3.70 HI_BITS_PTTRN

Offset	Bit(s)	Field Name	Description	Type	Default Value
104	7:6	reserved		RO	0
104	5	fw_desk_pattern[17]	Pattern used while searching de-skewing point between the lanes. (two symbols in 1+8b format)	R/W	1
104	4	fw_desk_pattern[8]	Pattern used while searching de-skewing point between the lanes. (two symbols in 1+8b format)	R/W	0
104	3:2	fw_symb_pattern2[9:8]	2nd pattern used as a reference for symbol lock	R/W	0x3
104	1:0	fw_symb_pattern1[9:8]	1st pattern used as a reference for symbol lock	R/W	0x0

4.6.1.3.71 DP_ERR_WGHT

Offset	Bit(s)	Field Name	Description	Type	Default Value
105	7:0	fw_err_weight	bigger value means lower weight for the errors, i.e. longer to reach err_hit	R/W	0x0

4.6.1.3.72 DP_NON_ERR_WGHT

Offset	Bit(s)	Field Name	Description	Type	Default Value
106	7:0	fw_non_err_weight	bigger value means lower weight for the errors, i.e. faster to reach err_hit	R/W	0x4

4.6.1.3.73 DP_ERR_THRSH

Offset	Bit(s)	Field Name	Description	Type	Default Value
107	7:0	fw_err_thrsh	Error filter using fw_err_weight and fw_non_err_weight triggers symbol relock when this threshold is achieved	R/W	0x4

4.6.1.3.74 TST_PTTRN_CTRL_0

Offset	Bit(s)	Field Name	Description	Type	Default Value
112	7:4	PRBS_EN	Enable (per lane) receiving PRBS7	R/W	0
112	3:0	IDLE_PATTERN_EN	Enable (per lane) receiving Idle pattern	R/W	0

4.6.1.3.75 TST_PTTRN_CTRL_1

Offset	Bit(s)	Field Name	Description	Type	Default Value
113	7	TST_PTTRN_ERR_CNT_B	Enable counter-B to count test pattern errors	R/W	0
113	6	TST_PTTRN_ERR_CNT_A	Enable counter-A to count test pattern errors	R/W	0
113	5:0	reserved		RO	0

4.6.1.3.76 TST_PTTRN_CTRL_2

Offset	Bit(s)	Field Name	Description	Type	Default Value
114	7:2	reserved		RO	0
114	1	IDLE_PTTRN_CNT_BIT_ERR	Count bit errors instead of symbol errors.	R/W	0
114	0	IDLE_PTTRN_ENHANCED	The length of the special character sequence in the Eye pattern: 0: 1 Byte 1: 4 Bytes	R/W	1

4.6.1.3.77 TST_PTTRN_K

Offset	Bit(s)	Field Name	Description	Type	Default Value
115	7:4	IDLE_PTTRN_SR_K	Per TST_PTTRN_SR_x: (0 ≤x ≤3) 0 – data symbol 1 – k-symbol	R/W	0xF
115	3:0	IDLE_PTTRN_BS_K	Per TST_PTTRN_BS_x: (0 ≤x ≤3) 0 – data symbol 1 – k-symbol	R/W	0xF

4.6.1.3.78 TST_PTTRN_BS_0

Offset	Bit(s)	Field Name	Description	Type	Default Value
116	7:0	IDLE_PTTRN_BS_0	8b representation of the 1st BS symbol	R/W	0xBC

4.6.1.3.79 TST_PTTRN_BS_1

Offset	Bit(s)	Field Name	Description	Type	Default Value
117	7:0	IDLE_PTTRN_BS_1	8b representation of the 2nd BS symbol	R/W	0x7C

4.6.1.3.80 TST_PTTRN_BS_2

Offset	Bit(s)	Field Name	Description	Type	Default Value
118	7:0	IDLE_PTTRN_BS_2	8b representation of the 3rd BS symbol	R/W	0x7C

4.6.1.3.81 TST_PTTRN_BS_3

Offset	Bit(s)	Field Name	Description	Type	Default Value
119	7:0	IDLE_PTTRN_BS_3	8b representation of the 4th BS symbol	R/W	0xBC

4.6.1.3.82 TST_PTTRN_SR_0

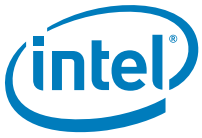
Offset	Bit(s)	Field Name	Description	Type	Default Value
120	7:0	IDLE_PTTRN_BS_0	8b representation of the 1st SR symbol	R/W	0x1C

4.6.1.3.83 TST_PTTRN_SR_1

Offset	Bit(s)	Field Name	Description	Type	Default Value
121	7:0	IDLE_PTTRN_BS_1	8b representation of the 2nd SR symbol	R/W	0x7C

4.6.1.3.84 TST_PTTRN_SR_2

Offset	Bit(s)	Field Name	Description	Type	Default Value
122	7:0	IDLE_PTTRN_BS_2	8b representation of the 3rd SR symbol	R/W	0x7C



4.6.1.3.85 TST_PTTRN_SR_3

Offset	Bit(s)	Field Name	Description	Type	Default Value
123	7:0	IDLE_PTTRN_BS_3	8b representation of the 4th SR symbol	R/W	0x1C

4.6.1.3.86 TST_PTTRN_BS_RATIO_0

Offset	Bit(s)	Field Name	Description	Type	Default Value
124	7:0	IDLE_PTTRN_BS_RATIO_LO	Number of cycles between the first symbol of one BS sequence and the first symbol of the next BS sequence. (Low byte)	R/W	0x0

4.6.1.3.87 TST_PTTRN_BS_RATIO_1

Offset	Bit(s)	Field Name	Description	Type	Default Value
125	7:0	IDLE_PTTRN_BS_RATIO_HI	Number of cycles between the first symbol of one BS sequence and the first symbol of the next BS sequence. (High byte)	R/W	0x20

4.6.1.3.88 TST_PTTRN_SR_RATIO_0

Offset	Bit(s)	Field Name	Description	Type	Default Value
125	7:0	IDLE_PTTRN_BS_RATIO_HI	Number of cycles between the first symbol of one BS sequence and the first symbol of the next BS sequence. (High byte)	R/W	0x20

4.6.1.3.89 TST_PTTRN_SR_RATIO_1

Offset	Bit(s)	Field Name	Description	Type	Default Value
127	7:0	IDLE_PTTRN_SR_RATIO_HI	Once in a while BS sequence is substituted by SR sequence. This field defines the number of BS sequences between any two SR sequences. (High byte)	R/W	0x1

4.6.1.3.90 TST_PTTRN_SR_SYMB_0

Offset	Bit(s)	Field Name	Description	Type	Default Value
128	7:0	IDLE_PTTRN_SR_n_7_0	10b representation of the 1st SR symbol negative disparity. (bits [7:0])	R/W	0xF4

4.6.1.3.91 TST_PTTRN_SR_SYMB_1

Offset	Bit(s)	Field Name	Description	Type	Default Value
129	7:0	IDLE_PTTRN_SR_p_7_0	10b representation of the 1st SR symbol positive disparity. (bits [7:0])	R/W	0x0B

4.6.1.3.92 TST_PTTRN_SR_SYMB_2

Offset	Bit(s)	Field Name	Description	Type	Default Value
130	7:4	reserved		RO	0
130	3:2	IDLE_PTTRN_SR_p_9_8	10b representation of the 1st SR symbol negative disparity. (bits [9:8] – bit 9 is the first on the wire)	R/W	0x3
130	1:0	IDLE_PTTRN_SR_n_9_8	10b representation of the 1st SR symbol negative disparity. (bits [9:8] – bit 9 is the first on the wire)		0x0

4.6.1.3.93 AUX_PHY_CTRL

Offset	Bit(s)	Field Name	Description	Type	Default Value
151	7:4	reserved	Reserved	RW	0
151		aux_phy_amp_ctl	Adjust Tx swing amplitude	RW	0
151	1	common_mode_en	Charge the PHY to its common mode	RW	0
151	0	single_ended_en	When asserted, the PHY will operate based on AUX_P only	RW	0

4.6.1.4 Bank 5 - Auxiliary

Table 158 is a summary of the AUX registers without registers description. The detailed description of the register list is given in the following sections.

Table 158. 0xA00 AUX Channel Registers Summary

Register Number	Register Name	Section #
0	HOST_CONTROL	"HOST_CONTROL Control bits." on page 400
1	SWAP_CONTROL	"SWAP_CONTROL" on page 401
8	SEND_INTERNAL_TRANSACTION	"SEND_INTERNAL_TRANSACTION." on page 401
9	SEND_EXTERNAL_TRANSACTION	"SEND_EXTERNAL_TRANSACTIO?N" on page 401
10	SEND_NACK_TRANSACTION	"SEND_NACK_TRANSACTION" on page 401
11	SEND_TO_ADAPTER	"SEND_TO_ADAPTER" on page 401
12	CLEAR_RX	"CLEAR_RX" on page 401
13	CLEAR_EXTERNAL	"CLEAR_EXTERNAL" on page 402
14	CLEAR_TIMER	"CLEAR_TIMER" on page 402
15	RESET_DP_AUX_SW	"RESET_DP_AUX_SW" on page 402
16	DIVIDE_2M	"DIVIDE_2M" on page 402
17	TX_PREACHARGE _LENGTH	"TX_PRECHARGE_LENGTH" on page 402
20	FREQUENCY_1M_MAX	"FREQUENCY_1M_MAX" on page 402

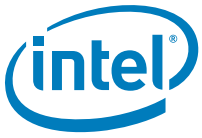


Table 158. 0xA00 AUX Channel Registers Summary

Register Number	Register Name	Section #
21	FREQUENCY_1M_MIN	"FREQUENCY_1M_MIN" on page 403
22	RX_PRE _MIN	"RX_PRE_MIN" on page 403
23	RX_PRE_MAX	"RX_PRE_MAX" on page 403
24	TIMER_PRESET_DP_IN_HIGH	"TIMER_PRESET_DP_IN_HIGH" on page 403
25	TIMER_PRESET_DP_IN_LOW	"TIMER_PRESET_DP_IN_LOW" on page 403
26	TIMER_PRESET_DP_OUT_HIGH	"TIMER_PRESET_DP_OUT_HIGH" on page 403
27	TIMER_PRESET_DP_OUT_LOW	"TIMER_PRESET_DP_OUT_LOW" on page 403
28	NACK_FORMAT	"NACK_FORMAT" on page 404
32	INTERNAL_TRANSACTION_LENGTH	"INTERNAL_TRANSACTION_LENGTH" on page 404
33	INTERNAL_DATA_00A	"INTERNAL_DATA_00A" on page 404
34	INTERNAL_DATA_00B	"INTERNAL_DATA_00B" on page 404
35	INTERNAL_DATA_01	"INTERNAL_DATA_01" on page 404
36	INTERNAL_DATA_02	"INTERNAL_DATA_02" on page 404
37	INTERNAL_DATA_03	"INTERNAL_DATA_03" on page 404
38	INTERNAL_DATA_04	"INTERNAL_DATA_04" on page 404
39	INTERNAL_DATA_05	"INTERNAL_DATA_05" on page 405
40	INTERNAL_DATA_06	"INTERNAL_DATA_06" on page 405
41	INTERNAL_DATA_07	"INTERNAL_DATA_07" on page 405
42	INTERNAL_DATA_08	"INTERNAL_DATA_08" on page 405
43	INTERNAL_DATA_09	"INTERNAL_DATA_09" on page 405
44	INTERNAL_DATA_10	"INTERNAL_DATA_10" on page 405
45	INTERNAL_DATA_11	"INTERNAL_DATA_11" on page 405
46	INTERNAL_DATA_12	"INTERNAL_DATA_12" on page 405
47	INTERNAL_DATA_13	"INTERNAL_DATA_13" on page 405
48	INTERNAL_DATA_14	"INTERNAL_DATA_14" on page 405
49	INTERNAL_DATA_15	"INTERNAL_DATA_15" on page 405
50	INTERNAL_DATA_16	"INTERNAL_DATA_16" on page 405
51	INTERNAL_DATA_17	"INTERNAL_DATA_17" on page 406

Table 158. 0xA00 AUX Channel Registers Summary

Register Number	Register Name	Section #
52	INTERNAL_DATA_18	"INTERNAL_DATA_18" on page 406
53	INTERNAL_DATA_19	"INTERNAL_DATA_19" on page 406
64	AUX_STATUS	"AUX_STATUS" on page 406
65	AUX_RX_STATUS	"AUX_RX_STATUS" on page 406
66	EXTERNAL_TRANSACTION_READY	"EXTERNAL_TRANSACTION_READY" on page 407
67	EXTERNAL_STATUS	"EXTERNAL_STATUS" on page 407
68	AUX_TX_STATUS	"AUX_TX_STATUS" on page 407
69	TIMER_STATUS	"TIMER_STATUS" on page 407
90	AUX_POWER_STATE	"AUX_POWER_STATE" on page 407
96	RECEIVE_TRANSACTION_LENGTH	"RECEIVE_TRANSACTION_LENGTH" on page 408
97	RECEIVE_DATA_00A	"RECEIVE_DATA_00A" on page 408
98	RECEIVE_DATA_00B	"RECEIVE_DATA_00B" on page 408
99	RECEIVE_DATA_01	"RECEIVE_DATA_01" on page 408
100	RECEIVE_DATA_02	"RECEIVE_DATA_02" on page 408
101	RECEIVE_DATA_03	"RECEIVE_DATA_03" on page 408
102	RECEIVE_DATA_04	"RECEIVE_DATA_04" on page 408
103	RECEIVE_DATA_05	"RECEIVE_DATA_05" on page 408
104	RECEIVE_DATA_06	"RECEIVE_DATA_06" on page 408
105	RECEIVE_DATA_07	"RECEIVE_DATA_07" on page 409
106	RECEIVE_DATA_08	"RECEIVE_DATA_08" on page 409
107	RECEIVE_DATA_09	"RECEIVE_DATA_09" on page 409
108	RECEIVE_DATA_10	"RECEIVE_DATA_10" on page 409
109	RECEIVE_DATA_11	"RECEIVE_DATA_11" on page 409
110	RECEIVE_DATA_12	"RECEIVE_DATA_12" on page 409
111	RECEIVE_DATA_13	"RECEIVE_DATA_13" on page 409
112	RECEIVE_DATA_14	"RECEIVE_DATA_14" on page 409
113	RECEIVE_DATA_15	"RECEIVE_DATA_15" on page 409
114	RECEIVE_DATA_16	"RECEIVE_DATA_16" on page 409

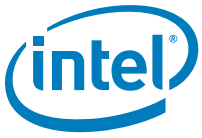


Table 158. 0xA00 AUX Channel Registers Summary

Register Number	Register Name	Section #
115	RECEIVE_DATA_17	"RECEIVE_DATA_17" on page 409
116	RECEIVE_DATA_18	"RECEIVE_DATA_18" on page 409
117	RECEIVE_DATA_19	"RECEIVE_DATA_19" on page 410
120	RECEIVE_LAST_TRANSACTION_LENGTH	"RECEIVE_LAST_TRANSACTION_LENGTH" on page 410
121	RECEIVE_LAST_DATA_LENGTH	"RECEIVE_LAST_DATA_LENGTH" on page 410
128	EXTERNAL_TRANSACTION_LENGTH	"EXTERNAL_TRANSACTION_LENGTH" on page 410
129	EXTERNAL_DATA_00A	"EXTERNAL_DATA_00A" on page 410
130	EXTERNAL_DATA_00B	"EXTERNAL_DATA_00B" on page 410
131	EXTERNAL_DATA_01	"EXTERNAL_DATA_01" on page 410
132	EXTERNAL_DATA_02	"EXTERNAL_DATA_02" on page 410
133	EXTERNAL_DATA_03	"EXTERNAL_DATA_03" on page 410
134	EXTERNAL_DATA_04	"EXTERNAL_DATA_04" on page 411
135	EXTERNAL_DATA_05	"EXTERNAL_DATA_05" on page 411
136	EXTERNAL_DATA_06	"EXTERNAL_DATA_06" on page 411
137	EXTERNAL_DATA_07	"EXTERNAL_DATA_07" on page 411
138	EXTERNAL_DATA_08	"EXTERNAL_DATA_08" on page 411
139	EXTERNAL_DATA_09	"EXTERNAL_DATA_09" on page 411
140	EXTERNAL_DATA_10	"EXTERNAL_DATA_10" on page 411
141	EXTERNAL_DATA_11	"EXTERNAL_DATA_11" on page 411
142	EXTERNAL_DATA_12	"EXTERNAL_DATA_12" on page 411
143	EXTERNAL_DATA_13	"EXTERNAL_DATA_13" on page 411
144	EXTERNAL_DATA_14	"EXTERNAL_DATA_14" on page 411
145	EXTERNAL_DATA_15	"EXTERNAL_DATA_15" on page 411
146	EXTERNAL_DATA_16	"EXTERNAL_DATA_16" on page 412
147	EXTERNAL_DATA_17	"EXTERNAL_DATA_17" on page 412
148	EXTERNAL_DATA_18	"EXTERNAL_DATA_18" on page 412
149	EXTERNAL_DATA_19	"EXTERNAL_DATA_19" on page 412
256	RX_DONE_ALL	"RX_DONE_ALL" on page 412

Table 158. 0xA00 AUX Channel Registers Summary

Register Number	Register Name	Section #
257	RX_DONE_OK	"RX_DONE_OK" on page 412
258	RX_DONE_LAST_EQUAL	"RX_DONE_LAST_EQUAL" on page 412
259	RX_DONE_ERRORS	"RX_DONE_ERRORS" on page 412
260	RX_DONE_ERROR_CORRUPTED	"RX_DONE_ERROR_CORRUPTED" on page 412
261	RX_DONE_ERROR_LONG_DATA	"RX_DONE_ERROR_LONG_DATA" on page 412
262	RX_DONE_ERROR_LONG_PREAMBLE	"RX_DONE_ERROR_LONG_PREAMBLE" on page 413
263	RX_DONE_ERROR_CYCLE_TIME	"RX_DONE_ERROR_CYCLE_TIME" on page 413
272	TX_DONE_ALL	"TX_DONE_ALL" on page 413
273	TX_DONE_NACK	"TX_DONE_NACK" on page 413
274	TX_DONE_INTERNAL	"TX_DONE_INETNAL" on page 413
275	TX_DONE_EXTERNAL	"TX_DONE_EXTERNAL" on page 413
280	EXPIRE_GLOBAL	"EXPIRE_GLOBAL" on page 413
281	EXPIRE_INTERNAL	"EXPIRE_INTERNAL" on page 413
282	EXPIRE_EXTERNAL	"EXPIRE_EXTERNAL" on page 413
288	ADAPTER_OUT	"ADAPTER_OUT" on page 413
289	ADAPTER_IN	"ADAPTER_IN" on page 413
290	ADAPTER_IN_EQUAL	"ADAPTER_IN_EQUAL" on page 414
291	ADAPTER_IN_LOAST_NEW	"ADAPTER_IN_LOST_NEW" on page 414
292	ADAPTER_IN_LOAST_PREVIOUS	"ADAPTER_IN_LOST_PREVIOUS" on page 414
296	TX_STATE	"TX_STATE" on page 414
297	TX_DATA	"TX_DATA" on page 414
298	TX_COUNTER	"TX_COUNTER" on page 414
304	RX_MAIN_STATE	"RX_MAIN_STATE" on page 414
305	RX_PREAMBLE_STATE	"RX_PREAMBLE_STATE" on page 414
306	RX_HHLL_STATE	"RX_HHLL_STATE" on page 414
307	RX_DATA_STATE	"RA_DATA_STATE" on page 415
308	RX_BYTE_COUNTER	"TX_BYTE_COUNTER" on page 415
309	RX_SHIFT_REG	"RX_SHIFT_REG" on page 415

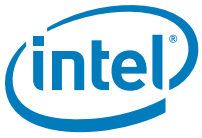


Table 158. 0xA00 AUX Channel Registers Summary

Register Number	Register Name	Section #
310	RX_PREAMBLE_COUNTER	"RX_PREAMBLE_COUNTER" on page 415
311	RX_CYCLE_COUNTER_LOW	"RX_CYCLE_COUNTER_LOW" on page 415
312	RX_CYCLE_COUNTER_HIGH	"RX_CYCLE_COUNTER_HIGH" on page 415
313	RX_LAST_CYCLE	"RX_LAST_CYCLE" on page 415
314	RX_SUM_CYCLE_LOW	"RX_SUM_CYCLE_LOW" on page 415
315	RX_SUM_CYCLE_HIGH	"RX_SUM_CYCLE_HIGH" on page 415
316	RX_CYCLE_AVERAGE	"RX_CYCLE_AVERAGE" on page 416
317	RX_TICK_CYCLE	"RX_TICK_CYCLE" on page 416
320	MAIN_STATES	"MAIN_STATES" on page 416
321	MAIN_TIMER_LOW	"MAIN_TIMER_LOW" on page 416
322	MAIN_TIMER_HIGH	"MAIN_TIMER_HIGH" on page 416
323	MAIN_RX_TO_ADAPTER_COUNTER	"MAIN_RX_TO_ADAPTER_COUNTER" on page 416
324	MAIN_EXTERNAL_STATE	"MAIN_EXTERNAL_STATE" on page 416
325	MAIN_EXTERNAL_COUNTER	"MAIN_EXTERNAL_COUNTER" on page 416
326	MAIN_TX_MUX_COUNTER	"MAIN_TX_MUX_COUNTER" on page 416
328	AUX_AFE_IN	"AUX_AFE_IN" on page 417
329	AUX_AFE_OUT	"AUX_AFE_OUT" on page 417
330	AUX_CHICKEN0	"AUX_CHICKEN0" on page 417

4.6.1.4.1 HOST_CONTROL Control bits.

Register length - 5 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
0	4	aux_host_always_read	Normally the aux_rx is disabled during transmit. Setting this bit allow loopback operation and all transmit transactions will be enter to the receiver. Use for debugging.	R/W	0
0	3	aux_host_precharge_enable	According to the current standard the TX precharge is done by sending 10 to 16 data_0 on the line before the SYNC. Old standard define the precharge by forcing the AFE to be in precharge mode before start transmitting the SYNC.	R/W	0

0	2	aux_host_transmit_immediate_reg	This bit is used only in DP_OUT mode. If SET, a transaction that comes from the adapter will be sent immediately without waiting to send_external_transaction pulse. If CLEAR the MC controls the traffic to/ from adapter.	R/W	1
0	1:0	aux_host_average_no_of_cycles	Calculate the cycle time by doing average of the last 2, 4, 8 cycles in the preamble (00-2 cycles, 01-4 cycles, 1x-8 cycles).	R/W	2'b10

4.6.1.4.2 SWAP_CONTROL

Control the bits ordering of transmit and receive.

Register length - 2 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
1	1	aux_host_tx_swap	Shift right the output data (LSB first).	R/W	0
1	0	aux_host_rx_swap	Shift right (LSB first) of the income data.	R/W	0

4.6.1.4.3 SEND_INTERNAL_TRANSACTION.

Register length - 1 bit

Offset	Bit(s)	Field Name	Description	Type	Default Value
8	0	aux_host_send_internal_transaction	send internal transaction by AUX_TX	WO	0

4.6.1.4.4 SEND_EXTERNAL_TRANSACTIO?N

Register length - 1 bit

Offset	Bit(s)	Field Name	Description	Type	Default Value
9	0	aux_host_send_external_transaction	Send external transaction by AUX_TX.	WO	0

4.6.1.4.5 SEND_NACK_TRANSACTION

Register length - 1 bit

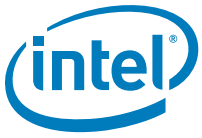
Offset	Bit(s)	Field Name	Description	Type	Default Value
10	0	aux_host_send_nack_transaction	Send NACK transaction by AUX_TX.	WO	0

4.6.1.4.6 SEND_TO_ADAPTER

Register length - 1 bit

Offset	Bit(s)	Field Name	Description	Type	Default Value
11	0	aux_host_forward_rx_to_adpater	Forward the receive transaction to the adapter. It also enables the AUX_RX as the "enable_rx".	WO	0

4.6.1.4.7 CLEAR_RX



Register length - 1 bit

Offset	Bit(s)	Field Name	Description	Type	Default Value
12	0	aux_host_clear_rx	Clear all RX bits in register 64, 65. This command is an indication that the processing of last receive transaction was completed and the AUX_RX can start looking for new receive transaction.	WO	0

4.6.1.4.8 CLEAR_EXTERNAL

Register length - 1 bit

Offset	Bit(s)	Field Name	Description	Type	Default Value
13	0	aux_host_clear_external	Clear all external bits in registers 64, 67.	WO	0

4.6.1.4.9 CLEAR_TIMER

Register length - 1 bit

Offset	Bit(s)	Field Name	Description	Type	Default Value
14	0	aux_host_clear_timer	Clear all expired bits in register 64.	WO	0

4.6.1.4.10 RESET_DP_AUX_SW

Register length - 1 bit

Offset	Bit(s)	Field Name	Description	Type	Default Value
15	0	aux_host_sw_reset	Reset all DP_AUX state machines and clear all the status bits. The registers value remains. (S/W reset)	WO	0

4.6.1.4.11 DIVIDE_2M

Offset	Bit(s)	Field Name	Description	Type	Default Value
16	7:0	aux_host_divide_2m	The ratio between sys_clk and 2MHz, [(sys_clk frequency/2MHz) - 1], for 25MHz sys_clk the value is 11. This register is used by AUX_TX for generating the AUX_TX clock.	R/W	0x30

4.6.1.4.12 TX_PRECHARGE_LENGTH

Register length - 6 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
17	5:0	aux_host_precharge_length	Length of precharge field, standard definition is 10 to 16 bits/clocks.	R/W	16

4.6.1.4.13 FREQUENCY_1M_MAX

Offset	Bit(s)	Field Name	Description	Type	Default Value
20	7:0	aux_host_1m_max	The maximum legal frequency receiving from the line by the standard is 1.25MHz. The calculation is: (1.25 MHz cycle time)/(sys_clk(-15%) cycle time) -1 800/47-1=16	R/W	0x46

4.6.1.4.14 FREQUENCY_1M_MIN

Offset	Bit(s)	Field Name	Description	Type	Default Value
21	7:0	aux_host_1m_min	The minimum legal frequency receiving from the line by the standard is 0.83MHz.The calculation is: (0.83 MHz cycle time)/(sys_clk(+15%) cycle time) -1 1200/35-1=34	R/W	0x8C

4.6.1.4.15 RX_PRE_MIN

Register length - 6 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
22	5:0	aux_host_pre_min	Valid minimum length of preamble during receive. The standard defines pre_min = 26. Restriction: The value of this register should be greater than the average_number_of_cycles defined in register 0 (2, 4 or 8).	R/W	10

4.6.1.4.16 RX_PRE_MAX

Register length - 6 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
23	5:0	aux_host_pre_max	Valid maximum length of preamble during receive. The standard defines pre_max = 32.	R/W	35

4.6.1.4.17 TIMER_PRESET_DP_IN_HIGH

Offset	Bit(s)	Field Name	Description	Type	Default Value
24	7:0	timer_preset_dp_in_high	The preset value of the timer in DP_IN mode. With sys_clk= 25MHz the Timer can measure up to ~2500 micro seconds. The defaults value is 300 microseconds (0x1D4C).	R/W	0x1D

4.6.1.4.18 TIMER_PRESET_DP_IN_LOW

Offset	Bit(s)	Field Name	Description	Type	Default Value
25	7:0	timer_preset_dp_in_low	See	R/W	0x4C

4.6.1.4.19 TIMER_PRESET_DP_OUT_HIGH

Offset	Bit(s)	Field Name	Description	Type	Default Value
26	7:0	timer_preset_dp_out_high	High bits of the preset value of the timer in DP_OUT mode. With sys_clk= 25MHz the Timer can measure up to ~2500 micro seconds. The defaults value is 400 microseconds (0x2710).	R/W	0x27

4.6.1.4.20 TIMER_PRESET_DP_OUT_LOW

Offset	Bit(s)	Field Name	Description	Type	Default Value

27	7:0	timer_preset_dp_out_low	Low bits of the preset value of the timer in DP_OUT mode. With sys_clk= 25MHz the Timer can measure up to ~2500 micro seconds. The defaults value is 400 microseconds (0x2710).	R/W	0x10

4.6.1.4.21 NACK_FORMAT

Offset	Bit(s)	Field Name	Description	Type	Default Value
28	7:0	aux_host_nack_format	NACK or DEFER pattern for transmit (00100000 for DEFER, 00010000 for NACK).	R/W	8'b00100000

4.6.1.4.22 INTERNAL_TRANSACTION_LENGTH

Register length - 5 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
32	4:0	aux_host_internal_length	The length of the internal transaction (maximum 20 bytes).	R/W	0

4.6.1.4.23 INTERNAL_DATA_00A

Register length - 4 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
33	3:0	internal_data_00a	Internal Transaction bits 7:4 of byte 0.	R/W	0

4.6.1.4.24 INTERNAL_DATA_00B

Register length - 4 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
34	3:0	internal_data_00b	Internal Transaction bits 3:0 of byte 0.	R/W	0

4.6.1.4.25 INTERNAL_DATA_01

Offset	Bit(s)	Field Name	Description	Type	Default Value
35	7:0	internal_data_01	Internal Transaction byte 1.	R/W	0

4.6.1.4.26 INTERNAL_DATA_02

Offset	Bit(s)	Field Name	Description	Type	Default Value
36	7:0	internal_data_02	Internal Transaction byte 2.	R/W	0

4.6.1.4.27 INTERNAL_DATA_03

Offset	Bit(s)	Field Name	Description	Type	Default Value
37	7:0	internal_data_03	Internal Transaction byte 3.	R/W	0

4.6.1.4.28 INTERNAL_DATA_04

Offset	Bit(s)	Field Name	Description	Type	Default Value
38	7:0	internal_data_04	Internal Transaction byte 4.	R/W	0

4.6.1.4.29 INTERNAL_DATA_05

Offset	Bit(s)	Field Name	Description	Type	Default Value
39	7:0	internal_data_05	Internal Transaction byte 5.	R/W	0

4.6.1.4.30 INTERNAL_DATA_06

Offset	Bit(s)	Field Name	Description	Type	Default Value
40	7:0	internal_data_06	Internal Transaction byte 6.	R/W	0

4.6.1.4.31 INTERNAL_DATA_07

Offset	Bit(s)	Field Name	Description	Type	Default Value
41	7:0	internal_data_07	Internal Transaction byte 7.	R/W	0

4.6.1.4.32 INTERNAL_DATA_08

Offset	Bit(s)	Field Name	Description	Type	Default Value
42	7:0	internal_data_08	Internal Transaction byte 8.	R/W	0

4.6.1.4.33 INTERNAL_DATA_09

Offset	Bit(s)	Field Name	Description	Type	Default Value
43	7:0	internal_data_09	Internal Transaction byte 9.	R/W	0

4.6.1.4.34 INTERNAL_DATA_10

Offset	Bit(s)	Field Name	Description	Type	Default Value
44	7:0	internal_data_10	Internal Transaction byte 10.	R/W	0

4.6.1.4.35 INTERNAL_DATA_11

Offset	Bit(s)	Field Name	Description	Type	Default Value
45	7:0	internal_data_11	Internal Transaction byte 11.	R/W	0

4.6.1.4.36 INTERNAL_DATA_12

Offset	Bit(s)	Field Name	Description	Type	Default Value
46	7:0	internal_data_12	Internal Transaction byte 12.	R/W	0

4.6.1.4.37 INTERNAL_DATA_13

Offset	Bit(s)	Field Name	Description	Type	Default Value
46	7:0	internal_data_12	Internal Transaction byte 12.	R/W	0

4.6.1.4.38 INTERNAL_DATA_14

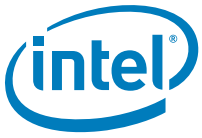
Offset	Bit(s)	Field Name	Description	Type	Default Value
48	7:0	internal_data_14	Internal Transaction byte 14.	R/W	0

4.6.1.4.39 INTERNAL_DATA_15

Offset	Bit(s)	Field Name	Description	Type	Default Value
49	7:0	internal_data_15	Internal Transaction byte 15.	R/W	0

4.6.1.4.40 INTERNAL_DATA_16

Offset	Bit(s)	Field Name	Description	Type	Default Value
50	7:0	internal_data_16	Internal Transaction byte 16.	R/W	0



4.6.1.4.41 INTERNAL_DATA_17

Offset	Bit(s)	Field Name	Description	Type	Default Value
51	7:0	internal_data_17	Internal Transaction byte 17.	R/W	0

4.6.1.4.42 INTERNAL_DATA_18

Offset	Bit(s)	Field Name	Description	Type	Default Value
52	7:0	internal_data_18	Internal Transaction byte 18.	R/W	0

4.6.1.4.43 INTERNAL_DATA_19

Offset	Bit(s)	Field Name	Description	Type	Default Value
53	7:0	internal_data_19	Internal Transaction byte 19.	R/W	0

4.6.1.4.44 AUX_STATUS

Status bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
64	7	Reserved	Reserved	RO	0
64	6	aux_main_expire_external	Timer expires (external) in DP_OUT.	RO	0
64	5	aux_main_expire_internal	Timer expires (internal) in DP_OUT.	RO	0
64	4	aux_main_expire_global	Timer expires in DP_IN, (internal or external).	RO	0
64	3	aux_main_external_ready	AUX_MAIN read all transaction data from adapter. The transaction is ready for transmit by AUX_TX.	RO	0
64	2	aux_main_rx_status_done_external	AUX_RX in DP_OUT mode, completed processing the receiving of external transaction.	RO	0
64	1	aux_main_rx_status_done_internal	AUX_RX in DP_OUT mode, completed processing the receiving of internal transaction.	RO	0
64	0	aux_main_rx_status_done	AUX_RX in DP_IN mode, completed processing the receiving transaction (internal or external).	RO	0

4.6.1.4.45 AUX_RX_STATUS

Status bits of the receive transaction

Offset	Bit(s)	Field Name	Description	Type	Default Value
65	7:6	Reserved	Reserved	RO	0
65	5	aux_main_rx_status_error_corrupted	The received transaction corrupted during the data phase (bad STOP, or un align STOP).	RO	0
65	4	aux_main_rx_status_error_cycle_time	During the received transaction the AUX_RX measured clock cycle that is not on the allowed tolerance (<0.4 ms or >0.6 ms).	RO	0
65	3	aux_main_rx_status_error_long_data	The received transaction had more than 20 data bytes.	RO	0
65	2	aux_main_rx_status_error_long_preamble	The received transaction had preamble greater than the preamble_max.	RO	0

Offset	Bit(s)	Field Name	Description	Type	Default Value
65	1	aux_main_rx_status_last_equal	The receive transaction is equal to the previous transaction. (THIS IS NOT AN ERROR BIT!!).	RO	0
65	0	aux_main_rx_status_error	The transaction has an error. This bit is or of all error bits in this register.	RO	0

4.6.1.4.46 EXTERNAL_TRANSACTION_READY

Register length - 1 bit

Offset	Bit(s)	Field Name	Description	Type	Default Value
66	0	aux_main_external_ready	AUX_MAIN read all transaction data from adapter. The transaction is ready for transmit by AUX_TX.	RO	0

4.6.1.4.47 EXTERNAL_STATUS

Status bits of the external transaction. Register length - 5 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
67	4	aux_main_external_error_lost_new_equal	The new lost transaction is equal to the current transaction.	RO	0
67	3	aux_main_external_error_lost_new	A new transaction lost during transmitting of the current transaction.	RO	0
67	2	aux_main_external_error_lost_previous_equal	The equal bit of the lost previous transaction.	RO	0
67	1	aux_main_external_error_lost_previous	The adapter writes new transaction to the DP_AUX before the previous transaction started its transmission. The previous transaction lost.	RO	0
67	0	aux_main_external_equal_to_last	The current external transaction is equal to the previous external transaction.	RO	0

4.6.1.4.48 AUX_TX_STATUS

Status bit of transmit transaction. Register length - 3 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
68	2	aux_main_tx_status_done_external	AUX_TX completed the transmission of external transaction.	RO	0
68	1	aux_main_tx_status_done_internal	AUX_TX completed the transmission of internal transaction.	RO	0
68	0	aux_main_tx_status_done	AUX_TX completed the transmission of the transaction.	RO	0

4.6.1.4.49 TIMER_STATUS

Status bit of the timer. Register length - 3 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
69	2	aux_main_expire_external	Timer expired (external).	RO	0
69	1	aux_main_expire_internal	Timer expired (internal).	RO	0
69	0	aux_main_expire_global	Timer expired, (internal or external).	RO	0

4.6.1.4.50 AUX_POWER_STATE

AUX Phy power state. Register length - 2 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
90	1:0	aux_phy_power_state	Power state of AUX Phy: 0 – Active 1 – Power Down 2 - HiZ	R/W	2

4.6.1.4.51 RECEIVE_TRANSACTION_LENGTH

Register length - 5 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
96	4:0	aux_rx_length	The length of the receive transaction (maximum 20 bytes).	R/W	0

4.6.1.4.52 RECEIVE_DATA_00A

Register length - 4 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
97	3:0	rx_data_00a	Receive Transaction bits 7:4 of byte 00.	R/W	0

4.6.1.4.53 RECEIVE_DATA_00B

Register length - 4 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
98	3:0	rx_data_00b	Receive Transaction bits 3:0 of byte 00.	R/W	0

4.6.1.4.54 RECEIVE_DATA_01

Offset	Bit(s)	Field Name	Description	Type	Default Value
99	7:0	rx_data_01	Receive Transaction byte 01.	R/W	0

4.6.1.4.55 RECEIVE_DATA_02

Offset	Bit(s)	Field Name	Description	Type	Default Value
100	7:0	rx_data_02	Receive Transaction byte 02.	R/W	0

4.6.1.4.56 RECEIVE_DATA_03

Offset	Bit(s)	Field Name	Description	Type	Default Value
101	7:0	rx_data_03	Receive Transaction byte 03.	R/W	0

4.6.1.4.57 RECEIVE_DATA_04

Offset	Bit(s)	Field Name	Description	Type	Default Value
102	7:0	rx_data_04	Receive Transaction byte 04.	R/W	0

4.6.1.4.58 RECEIVE_DATA_05

Offset	Bit(s)	Field Name	Description	Type	Default Value
103	7:0	rx_data_05	Receive Transaction byte 05.	R/W	0

4.6.1.4.59 RECEIVE_DATA_06

Offset	Bit(s)	Field Name	Description	Type	Default Value
104	7:0	rx_data_06	Receive Transaction byte 06.	R/W	0

4.6.1.4.60 RECEIVE_DATA_07

Offset	Bit(s)	Field Name	Description	Type	Default Value
105	7:0	rx_data_07	Receive Transaction byte 07.	R/W	0

4.6.1.4.61 RECEIVE_DATA_08

Offset	Bit(s)	Field Name	Description	Type	Default Value
106	7:0	rx_data_08	Receive Transaction byte 08.	R/W	0

4.6.1.4.62 RECEIVE_DATA_09

Offset	Bit(s)	Field Name	Description	Type	Default Value
107	7:0	rx_data_09	Receive Transaction byte 09.	R/W	0

4.6.1.4.63 RECEIVE_DATA_10

Offset	Bit(s)	Field Name	Description	Type	Default Value
108	7:0	rx_data_10	Receive Transaction byte 10.	R/W	0

4.6.1.4.64 RECEIVE_DATA_11

Offset	Bit(s)	Field Name	Description	Type	Default Value
109	7:0	rx_data_11	Receive Transaction byte 11.	R/W	0

4.6.1.4.65 RECEIVE_DATA_12

Offset	Bit(s)	Field Name	Description	Type	Default Value
110	7:0	rx_data_12	Receive Transaction byte 12.	R/W	0

4.6.1.4.66 RECEIVE_DATA_13

Offset	Bit(s)	Field Name	Description	Type	Default Value
111	7:0	rx_data_13	Receive Transaction byte 13.	R/W	0

4.6.1.4.67 RECEIVE_DATA_14

Offset	Bit(s)	Field Name	Description	Type	Default Value
112	7:0	rx_data_14	Receive Transaction byte 14.	R/W	0

4.6.1.4.68 RECEIVE_DATA_15

Offset	Bit(s)	Field Name	Description	Type	Default Value
113	7:0	rx_data_15	Receive Transaction byte 15.	R/W	0

4.6.1.4.69 RECEIVE_DATA_16

Offset	Bit(s)	Field Name	Description	Type	Default Value
114	7:0	rx_data_16	Receive Transaction byte 16.	R/W	0

4.6.1.4.70 RECEIVE_DATA_17

Offset	Bit(s)	Field Name	Description	Type	Default Value
115	7:0	rx_data_17	Receive Transaction byte 17.	R/W	0

4.6.1.4.71 RECEIVE_DATA_18

Offset	Bit(s)	Field Name	Description	Type	Default Value
116	7:0	rx_data_18	Receive Transaction byte 18.	R/W	0

4.6.1.4.72 RECEIVE_DATA_19

Offset	Bit(s)	Field Name	Description	Type	Default Value
117	7:0	rx_data_19	Receive Transaction byte 19.	R/W	0

4.6.1.4.73 RECEIVE_LAST_TRANSACTION_LENGTH

Register length - 5 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
120	4:0	aux_rx_last_transaction_length	Shadow register of register 96.	RO	0

4.6.1.4.74 RECEIVE_LAST_DATA_LENGTH

Offset	Bit(s)	Field Name	Description	Type	Default Value
121	7:0	aux_rx_last_data_length	Shadow register of RECEIVE_DATA_05 reg. It contains the data_length field of auxiliary transaction.	RO	0

4.6.1.4.75 EXTERNAL_TRANSACTION_LENGTH

Register length - 5 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
128	4:0	aux_main_external_length	The length of the external transaction (maximum 20 bytes).	R/W	0

4.6.1.4.76 EXTERNAL_DATA_00A

Register length - 4 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
129	3:0	external_data_00a	External Transaction bits 7:4 of byte 00.	R/W	0

4.6.1.4.77 EXTERNAL_DATA_00B

Register length - 4 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
130	3:0	external_data_00a	External Transaction bits 3:0 of byte 00.	R/W	0

4.6.1.4.78 EXTERNAL_DATA_01

Offset	Bit(s)	Field Name	Description	Type	Default Value
131	7:0	external_data_01	External Transaction byte 01.	R/W	0

4.6.1.4.79 EXTERNAL_DATA_02

Offset	Bit(s)	Field Name	Description	Type	Default Value
132	7:0	external_data_02	External Transaction byte 02.	R/W	0

4.6.1.4.80 EXTERNAL_DATA_03

Offset	Bit(s)	Field Name	Description	Type	Default Value
133	7:0	external_data_03	External Transaction byte 03.	R/W	0

4.6.1.4.81 EXTERNAL_DATA_04

Offset	Bit(s)	Field Name	Description	Type	Default Value
134	7:0	external_data_04	External Transaction byte 04.	R/W	0

4.6.1.4.82 EXTERNAL_DATA_05

Offset	Bit(s)	Field Name	Description	Type	Default Value
135	7:0	external_data_05	External Transaction byte 05.	R/W	0

4.6.1.4.83 EXTERNAL_DATA_06

Offset	Bit(s)	Field Name	Description	Type	Default Value
136	7:0	external_data_06	External Transaction byte 06.	R/W	0

4.6.1.4.84 EXTERNAL_DATA_07

Offset	Bit(s)	Field Name	Description	Type	Default Value
137	7:0	external_data_07	External Transaction byte 07.	R/W	0

4.6.1.4.85 EXTERNAL_DATA_08

Offset	Bit(s)	Field Name	Description	Type	Default Value
138	7:0	external_data_08	External Transaction byte 08.	R/W	0

4.6.1.4.86 EXTERNAL_DATA_09

Offset	Bit(s)	Field Name	Description	Type	Default Value
139	7:0	external_data_09	External Transaction byte 09.	R/W	0

4.6.1.4.87 EXTERNAL_DATA_10

Offset	Bit(s)	Field Name	Description	Type	Default Value
140	7:0	external_data_10	External Transaction byte 10.	R/W	0

4.6.1.4.88 EXTERNAL_DATA_11

Offset	Bit(s)	Field Name	Description	Type	Default Value
141	7:0	external_data_11	External Transaction byte 11.	R/W	0

4.6.1.4.89 EXTERNAL_DATA_12

Offset	Bit(s)	Field Name	Description	Type	Default Value
142	7:0	external_data_12	External Transaction byte 12.	R/W	0

4.6.1.4.90 EXTERNAL_DATA_13

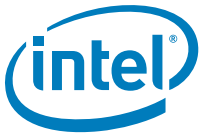
Offset	Bit(s)	Field Name	Description	Type	Default Value
143	7:0	external_data_13	External Transaction byte 13.	R/W	0

4.6.1.4.91 EXTERNAL_DATA_14

Offset	Bit(s)	Field Name	Description	Type	Default Value
144	7:0	external_data_14	External Transaction byte 14.	R/W	0

4.6.1.4.92 EXTERNAL_DATA_15

Offset	Bit(s)	Field Name	Description	Type	Default Value
145	7:0	external_data_15	External Transaction byte 15.	R/W	0



4.6.1.4.93 EXTERNAL_DATA_16

Offset	Bit(s)	Field Name	Description	Type	Default Value
146	7:0	external_data_16	External Transaction byte 16.	R/W	0

4.6.1.4.94 EXTERNAL_DATA_17

Offset	Bit(s)	Field Name	Description	Type	Default Value
147	7:0	external_data_17	External Transaction byte 17.	R/W	0

4.6.1.4.95 EXTERNAL_DATA_18

Offset	Bit(s)	Field Name	Description	Type	Default Value
148	7:0	external_data_18	External Transaction byte 18.	R/W	0

4.6.1.4.96 EXTERNAL_DATA_19

Offset	Bit(s)	Field Name	Description	Type	Default Value
149	7:0	external_data_19	External Transaction byte 19.	R/W	0

4.6.1.4.97 RX_DONE_ALL

Offset	Bit(s)	Field Name	Description	Type	Default Value
256	7:0	rx_done_all	Count all received transactions.	R/W	0

4.6.1.4.98 RX_DONE_OK

Offset	Bit(s)	Field Name	Description	Type	Default Value
257	7:0	rx_done_ok	Count all received transactions without any error.	R/W	0

4.6.1.4.99 RX_DONE_LAST_EQUAL

Offset	Bit(s)	Field Name	Description	Type	Default Value
258	7:0	rx_done_last_equal	Count all received transactions without any error that were equal to their previous transaction.	R/W	0

4.6.1.4.100 RX_DONE_ERRORS

Offset	Bit(s)	Field Name	Description	Type	Default Value
259	7:0	rx_done_errors	Count all received transactions with any error.	R/W	0

4.6.1.4.101 RX_DONE_ERROR_CORRUPTED

Offset	Bit(s)	Field Name	Description	Type	Default Value
260	7:0	rx_done_error_corrupted_data	Count received transactions with error corrupted_data.	R/W	0

4.6.1.4.102 RX_DONE_ERROR_LONG_DATA

Offset	Bit(s)	Field Name	Description	Type	Default Value
261	7:0	rx_done_error_long_data	Count received transactions with error long_data.	R/W	0

4.6.1.4.103 RX_DONE_ERROR_LONG_PREAMBLE

Offset	Bit(s)	Field Name	Description	Type	Default Value
262	7:0	rx_done_error_long_preamble	Count received transactions with error long_preamble.	R/W	0

4.6.1.4.104 RX_DONE_ERROR_CYCLE_TIME

Offset	Bit(s)	Field Name	Description	Type	Default Value
263	7:0	rx_done_error_cycle_time	Count received transactions with error cycle_time.	R/W	0

4.6.1.4.105 TX_DONE_ALL

Offset	Bit(s)	Field Name	Description	Type	Default Value
272	7:0	tx_done_all	Count all transmitted transactions.	R/W	0

4.6.1.4.106 TX_DONE_NACK

Offset	Bit(s)	Field Name	Description	Type	Default Value
273	7:0	tx_done_nack	Count all transmitted nack/defer transactions.	R/W	0

4.6.1.4.107 TX_DONE_INETNAL

Offset	Bit(s)	Field Name	Description	Type	Default Value
274	7:0	tx_done_internal	Count all transmitted internal transactions.	R/W	0

4.6.1.4.108 TX_DONE_EXTERNAL

Offset	Bit(s)	Field Name	Description	Type	Default Value
275	7:0	tx_done_external	Count all transmitted external transactions.	RW	0

4.6.1.4.109 EXPIRE_GLOBAL

Offset	Bit(s)	Field Name	Description	Type	Default Value
280	7:0	expire_global_all	Count all expire_global events.	R/W	0

4.6.1.4.110 EXPIRE_INTERNAL

Offset	Bit(s)	Field Name	Description	Type	Default Value
281	7:0	expire_internal_all	Count all expire_internal events.	R/W	0

4.6.1.4.111 EXPIRE_EXTERNAL

Offset	Bit(s)	Field Name	Description	Type	Default Value
282	7:0	expire_external_all	Count all expire_external events.	R/W	0

4.6.1.4.112 ADAPTER_OUT

Offset	Bit(s)	Field Name	Description	Type	Default Value
288	7:0	adapter_out_all	Count all RX to adapter events.	R/W	0

4.6.1.4.113 ADAPTER_IN

Offset	Bit(s)	Field Name	Description	Type	Default Value

289	7:0	adapter_in_all	Count all adapter in bursts	R/W	0

4.6.1.4.114 ADAPTER_IN_EQUAL

Offset	Bit(s)	Field Name	Description	Type	Default Value
290	7:0	adapter_in_equal	Count all adapter in bursts that were equal to the previous burst.	R/W	0

4.6.1.4.115 ADAPTER_IN_LOST_NEW

Offset	Bit(s)	Field Name	Description	Type	Default Value
291	7:0	adapter_in_lost_new_all	Count all new adapter in bursts that were lost since the previous burst is in process (DP_IN and DP_OUT) or was not transmitted yet (DP_IN).	R/W	0

4.6.1.4.116 ADAPTER_IN_LOST_PREVIOUS

Offset	Bit(s)	Field Name	Description	Type	Default Value
292	7:0	adpter_in_lost_previous_all	Count all the previous adapter in bursts that over write by new bursts.	R/W	0

4.6.1.4.117 TX_STATE

Register length - 7 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
296	6:0	aux_tx_state	aux_tx state machine register.	RO	1

4.6.1.4.118 TX_DATA

Offset	Bit(s)	Field Name	Description	Type	Default Value
297	7:0	aux_tx_data_reg	From this register the serial data is transmitted.	RO	0

4.6.1.4.119 TX_COUNTER

Register length - 7 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
298	6	aux_tx_down_count_end	Count end of down counter.	RO	0
298	5:0	aux_tx_down_counter	Down counter for AUX_TX state machine.	RO	0x3F

4.6.1.4.120 RX_MAIN_STATE

Register length - 5 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
304	4:0	aux_rx_main_state	AUX_RX main state machine register.	RO	2

4.6.1.4.121 RX_PREAMBLE_STATE

Register length - 6 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
305	5:0	aux_rx_preamble_state	AUX_RX preamble state machine register.	RO	2

4.6.1.4.122 RX_HHLL_STATE

Register length - 4 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
306	3:0	aux_rx_hhll_state	AUX_RX hhll state machine register.	RO	1

4.6.1.4.123 RA_DATA_STATE

Offset	Bit(s)	Field Name	Description	Type	Default Value
307	7:0	aux_rx_data_state	AUX_RX data state machine register.	RO	1

4.6.1.4.124 TX_BYTE_COUNTER

Register length - 5 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
308	4:0	aux_rx_byte_counter	Count income data bytes.	RO	0

4.6.1.4.125 RX_SHIFT_REG

Offset	Bit(s)	Field Name	Description	Type	Default Value
309	7:0	aux_rx_shift_reg	Receive shift register.	RO	0

4.6.1.4.126 RX_PREAMBLE_COUNTER

Register length - 7 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
310	6:0	aux_rx_preamble_counter	Count size of preamble.	RO	0

4.6.1.4.127 RX_CYCLE_COUNTER_LOW

Offset	Bit(s)	Field Name	Description	Type	Default Value
311	7:0	aux_rx_cycle_counter	Count system clocks from last change in the auxiliary line input (low part).	RO	0

4.6.1.4.128 RX_CYCLE_COUNTER_HIGH

Register length - 3 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
312	2:0	aux_rx_cycle_counter	Count system clocks from last change in the auxiliary line input (high part).	RO	0

4.6.1.4.129 RX_LAST_CYCLE

Offset	Bit(s)	Field Name	Description	Type	Default Value
313	7:0	aux_rx_last_cycle	Last cycle.	RO	0

4.6.1.4.130 RX_SUM_CYCLE_LOW

Offset	Bit(s)	Field Name	Description	Type	Default Value
314	7:0	aux_rx_sum_cycles_low	Sum of last 8 (or 4 or 2) cycles during preamble (low part).	RO	0

4.6.1.4.131 RX_SUM_CYCLE_HIGH

Register length - 3 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value

315	2:0	aux_rx_sum_cycles_high	Sum of last 8 (or 4 or 2) cycles during preamble (high part).	RO	0

4.6.1.4.132 RX_CYCLE_AVERAGE

Offset	Bit(s)	Field Name	Description	Type	Default Value
316	7:0	cycle_average	Cycle average from last preamble cycles.	RO	0

4.6.1.4.133 RX_TICK_CYCLE

Offset	Bit(s)	Field Name	Description	Type	Default Value
317	7:0	tick_cycle	Current reference cycle.	RO	0

4.6.1.4.134 MAIN_STATES

Offset	Bit(s)	Field Name	Description	Type	Default Value
320	6	Reserved		RO	0
320	5	aux_main_tx_state	AUX_MAIN tx state machine register.	RO	0
320	4:3	aux_main_rx_state	AUX_MAIN rx state machine register.	RO	0
320	2:1	aux_main_dp_state	AUX_MAIN dp state machine register.	RO	0
320	0	aux_main_timer_state	AUX_MAIN timer state machine register.	RO	0

4.6.1.4.135 MAIN_TIMER_LOW

Offset	Bit(s)	Field Name	Description	Type	Default Value
321	7:0	aux_main_timer	Timer (low part).	RO	0xFF

4.6.1.4.136 MAIN_TIMER_HIGH

Offset	Bit(s)	Field Name	Description	Type	Default Value
322	7:0	aux_main_timer	Timer (high part).	RO	0xFF

4.6.1.4.137 MAIN_RX_TO_ADAPTER_COUNTER

Register length - 5 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
323	4:0	rx_to_adapter_counter	Count bytes transfer from RX to adapter out.	RO	0

4.6.1.4.138 MAIN_EXTERNAL_STATE

Register length - 6 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
324	5:0	aux_main_external_state	AUX_MAIN external state machine register.	RO	1

4.6.1.4.139 MAIN_EXTERNAL_COUNTER

Register length - 5 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
325	4:0	aux_main_external_counter	Count data enter from adapter.	RO	0

4.6.1.4.140 MAIN_TX_MUX_COUNTER

Register length - 5 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
326	4:0	aux_main_tx_mux_counter	Count bytes forward to AUX_TX.	RO	0

4.6.1.4.141 AUX_AFE_IN

Register length - 1 bit

Offset	Bit(s)	Field Name	Description	Type	Default Value
328	0	afe_aux_data	Auxiliary data input from AFE.	RO	0

4.6.1.4.142 AUX_AFE_OUT

Register length - 6 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
329	5	aux_host_aux_afe_rx_pd	Drive the aux_afe_rx_pd output to the AFE when aux_host_afe_if_test_en (bit 0) is set.	R/W	0
329	4	aux_host_aux_afe_prech	Drive the aux_afe_prech output to the AFE when aux_host_afe_if_test_en (bit 0) is set.	R/W	0
329	3	aux_host_aux_afe_tx_pd	Drive the aux_afe_tx_pd output to the AFE when aux_host_afe_if_test_en (bit 0) is set.	R/W	0
329	2	aux_host_aux_afe_clk	Drive the aux_afe_clk output to the AFE when aux_host_afe_if_test_en (bit 0) is set.	R/W	0
329	1	aux_host_aux_afe_data	Drive the aux_afe_data output to the AFE when aux_host_afe_if_test_en (bit 0) is set.	R/W	0
329	0	aux_host_afe_if_test_en	TESTER mode enable. Give the TESTER direct interface to the AFE_AUX.	R/W	0

4.6.1.4.143 AUX_CHICKEN0

Extension of Tx transaction - 2 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
330	1:0	aux_host_tx_stop_extend	Extend AUX Tx stage before it change the direction to Rx stage.	R/W	0

4.6.1.5 Bank 6 - Miscellaneous

Table 159 is a summary of the MISC registers without registers description. The detailed description of the register list is given in the following sections.

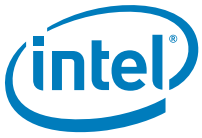


Table 159. 0xC00 MISC Registers Summary

Register	Register Name	Section #
0	LS_RST	"LS_RST" on page 422
1	AUX_RST	"AUX_RST" on page 422
2	ERROR_IND	"ERROR_IND" on page 422
3	DP_MODE	"DP_MODE" on page 423
4	LANE_DATA_ENABLE	"LANE_DATA_ENABLE" on page 423
5	MISC_STATUS_NO_CLR	"MISC_STATUS_NO_CLR" on page 423
6	LS_CLK_SEL	"LS_CLK_SEL" on page 423
7	MISC_USR0	"MISC_USR0" on page 423
8	MISC_COUNTER1_L	"MISC_COUNTER1_L" on page 423
9	MISC_COUNTER1_H	"MISC_COUNTER1_H" on page 423
10	MISC_COUNTER2_L	"MISC_COUNTER2_L" on page 424
11	MISC_COUNTER2_H	"MISC_COUNTER2_H" on page 424
12	MISC_1USEC_FACTOR	"MISC_1USEC_FACTOR" on page 424
14	DWNSPRD_EN	"DWNSPRD_EN" on page 424
15	TESETBUS_SEL	"TESTBUS_SEL" on page 424
16	HPD_IRQ_DET_MIN_TIMER_LO	"HPD_IRQ_DET_MIN_TIMER_LO" on page 424
17	HPD_IRQ_DET_MIN_TIMER_MD	"HPD_IRQ_DET_MIN_TIMER_MD" on page 424
18	HPD_IRQ_DET_MIN_TIMER_HI	"HPD_IRQ_DET_MIN_TIMER_HI" on page 424
19	HPD_IRQ_DET_MAX_TIMER_LO	"HPD_IRQ_DET_MAX_TIMER_LO" on page 424
20	HPD_IRQ_DET_MAX_TIMER_MD	"HPD_IRQ_DET_MAX_TIMER_MD" on page 424
21	HPD_IRQ_DET_MAX_TIMER_HI	"HPD_IRQ_DET_MAX_TIMER_HI" on page 425
22	HPD_UNPLGED_DET_MIN_TIMER_LO	"HPD_UNPLGED_DET_MIN_TIMER_LO" on page 425
23	HPD_UNPLGED_DET_MIN_TIMER_MD	"HPD_UNPLGED_DET_MIN_TIMER_MD" on page 425
24	HPD_UNPLGED_DET_MIN_TIMER_HI	"HPD_UNPLGED_DET_MIN_TIMER_HI" on page 425
28	HPD_IRQ_DET	"HPD_IRQ_DET" on page 425
29	HPD_RE_PLUGGED_DET	"HPD_RE_PLUGGED_DET" on page 425
30	HPD_GEN_TIMER_LO	"HPD_GEN_TIMER_LO" on page 425

Table 159. 0xC00 MISC Registers Summary

Register	Register Name	Section #
31	HPD_GEN_TIMER_MD	"HPD_GEN_TIMER_MD" on page 425
32	HPD_GEN_TIMER_HI	"HPD_GEN_TIMER_HI" on page 425
33	HPD_GEN	"HPD_GEN" on page 425
34	HPD_BYPASS	"HPD_BYPASS" on page 426
35	HPD_STATUS	"HPD_STATUS" on page 426
36	HPD_STABLE_TIMER_LO	"HPD_STABLE_TIMER_LO" on page 426
37	HPD_STABLE_TIMER_MD	"HPD_STABLE_TIMER_MD" on page 426
38	HPD_STABLE_TIMER_HI	"HPD_STABLE_TIMER_HI" on page 426
39	HPD_FILTER_TIMER_LO	"HPD_FILTER_TIMER_LO" on page 426
40	HPD_FILTER_TIMER_MD	"HPD_FILTER_TIMER_MD" on page 426
41	HPD_FILTER_TIMER_HI	"HPD_FILTER_TIMER_HI" on page 426
42	HPD_STABLE_STATUS	"HPD_STABLE_STATUS" on page 426
48	DP_IP_ADAPT_CONF_CHANGE_SET	"DP_IP_ADAPT_CONF_CHANGE_SET" on page 427
49	DP_IP_ADAPT_CONF_DATA0	"DP_IP_ADAPT_CONF_DATA0" on page 427
50	DP_IP_ADAPT_CONF_DATA1	"DP_IP_ADAPT_CONF_DATA1" on page 427
51	DP_IP_ADAPT_CONF_DATA2	"DP_IP_ADAPT_CONF_DATA2" on page 427
52	DP_ADAPT_IP_CONF_CHANGED	"DP_ADAPT_IP_CONF_CHANGED" on page 427
53	DP_ADAPT_IP_CONF_DATA0	"DP_ADAPT_IP_CONF_DATA0" on page 427
54	DP_ADAPT_IP_CONF_DATA1	"DP_ADAPT_IP_CONF_DATA1" on page 428
55	DP_ADAPT_IP_CONF_DATA2	"DP_ADAPT_IP_CONF_DATA2" on page 428
77	ERR_USR0_COUNT_TH_LO_A	"ERR_USR0_COUNT_TH_LO_A" on page 428
78	ERR_USR0_COUNT_TH_MD_A	"ERR_USR0_COUNT_TH_MD_A" on page 428
79	ERR_USR0_COUNT_TH_HI_A	"ERR_USR0_COUNT_TH_HI_A" on page 428
80	ERR_USR0_COUNT_TH_LO_B	"ERR_USR0_COUNT_TH_LO_B" on page 428
81	ERR_USR0_COUNT_TH_MD_B	"ERR_USR0_COUNT_TH_LO_B" on page 428
82	ERR_USR0_COUNT_TH_HI_B	"ERR_USR0_COUNT_TH_HI_B" on page 428
83	ERR_WINDOW_WIDTH_LO_A	"ERR_WINDOW_WIDTH_LO_A" on page 428
84	ERR_WINDOW_WIDTH_M0_A	"ERR_WINDOW_WIDTH_M0_A" on page 428

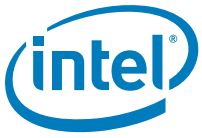


Table 159. 0xC00 MISC Registers Summary

Register	Register Name	Section #
85	ERR_WINDOW_WIDTH_M1_A	"ERR_WINDOW_WIDTH_M1_A" on page 428
86	ERR_WINDOW_WIDTH_HI_A	"ERR_WINDOW_WIDTH_HI_A" on page 429
87	ERR_COUNT_TH_LO_A	"ERR_COUNT_TH_LO_A" on page 429
88	ERR_COUNT_TH_MD_A	"ERR_COUNT_TH_MD_A" on page 429
89	ERR_COUNT_TH_HI_A	"ERR_COUNT_TH_HI_A" on page 429
90	ERR_WINDOW_WIDTH_LO_B	"ERR_WINDOW_WIDTH_LO_B" on page 429
91	ERR_WINDOW_WIDTH_M0_B	"ERR_WINDOW_WIDTH_M0_B" on page 429
92	ERR_WINDOW_WIDTH_M1_B	"ERR_WINDOW_WIDTH_M1_B" on page 429
93	ERR_WINDOW_WIDTH_HI_B	"ERR_WINDOW_WIDTH_HI_B" on page 429
94	ERR_SELECT	"ERR_SELECT" on page 429
95	ERR_COUNT_TH_LO_B	"ERR_COUNT_TH_LO_B" on page 429
96	ERR_COUNT_TH_MD_B	"ERR_COUNT_TH_MD_B" on page 429
97	ERR_COUNT_TH_HI_B	"ERR_COUNT_TH_HI_B" on page 429
98	ERR_COUNT_0A_LO	"ERR_COUNT_0A_LO" on page 430
99	ERR_COUNT_0A_MD	"ERR_COUNT_0A_MD" on page 430
100	ERR_COUNT_0A_HI	"ERR_COUNT_0A_HI" on page 430
101	ERR_COUNT_1A_LO	"ERR_COUNT_1A_LO" on page 430
102	ERR_COUNT_1A_MD	"ERR_COUNT_1A_MD" on page 430
103	ERR_COUNT_1A_HI	"ERR_COUNT_1A_HI" on page 430
104	ERR_COUNT_2A_LO	"ERR_COUNT_2A_LO" on page 430
105	ERR_COUNT_2A_MD	"ERR_COUNT_2A_MD" on page 430
106	ERR_COUNT_2A_HI	"ERR_COUNT_2A_HI" on page 430
107	ERR_COUNT_3A_LO	"ERR_COUNT_3A_LO" on page 430
108	ERR_COUNT_3A_MD	"ERR_COUNT_3A_MD" on page 430
109	ERR_COUNT_3A_HI	"ERR_COUNT_3A_HI" on page 431
110	ERR_COUNT_0B_LO	"ERR_COUNT_0B_LO" on page 431
111	ERR_COUNT_0B_MD	"ERR_COUNT_0B_MD" on page 431
112	ERR_COUNT_0B_HI	"ERR_COUNT_0B_HI" on page 431

Table 159. 0xC00 MISC Registers Summary

Register	Register Name	Section #
113	ERR_COUNT_1B_LO	"ERR_COUNT_1B_LO" on page 431
114	ERR_COUNT_1B_MD	"ERR_COUNT_1B_MD" on page 431
115	ERR_COUNT_1B_HI	"ERR_COUNT_1B_HI" on page 431
116	ERR_COUNT_2B_LO	"ERR_COUNT_2B_LO" on page 431
117	ERR_COUNT_2B_MD	"ERR_COUNT_2B_MD" on page 431
118	ERR_COUNT_2B_HI	"ERR_COUNT_2B_HI" on page 431
119	ERR_COUNT_3B_LO	"ERR_COUNT_3B_LO" on page 431
120	ERR_COUNT_3B_MD	"ERR_COUNT_3B_MD" on page 431
121	ERR_COUNT_3B_HI	"ERR_COUNT_3B_HI" on page 432
122	ERR_FLAGS_A	"ERR_FLAGS_A" on page 432
123	ERR_FLAGS_B	"ERR_FLAGS_B" on page 432
124	ERR_LOCK_COUNT_A	"ERR_LOCK_COUNT_A" on page 432
125	ERR_LOCK_COUNT_B	"ERR_LOCK_COUNT_B" on page 432
140	GP0	"GP0" on page 432
141	GP1	"GP1" on page 432
142	GP2	"GP2" on page 432
143	GP3	"GP3" on page 433
144	GP4	"GP4" on page 433
145	GP5	"GP5" on page 433
146	GP6	"GP6" on page 433
147	GP7	"GP7" on page 433
148	GP8	"GP8" on page 433
149	GP9	"GP9" on page 433
150	GP10	"GP10" on page 433
151	GP11	"GP11" on page 433
152	GP12	"GP12" on page 433
153	GP13	"GP13" on page 433
154	GP14	"GP14" on page 433

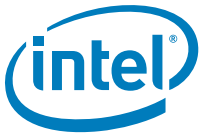


Table 159. 0xC00 MISC Registers Summary

Register	Register Name	Section #
155	GP15	"GP15" on page 434
272	ERR_COUNT_STD_0A_LO	"ERR_COUNT_STD_0A_LO" on page 434
273	ERR_COUNT_STD_0A_HI	"ERR_COUNT_STD_0A_HI" on page 434
274	ERR_COUNT_STD_1A_LO	"ERR_COUNT_STD_1A_LO" on page 434
275	ERR_COUNT_STD_1A_HI	"ERR_COUNT_STD_1A_HI" on page 434
276	ERR_COUNT_STD_2A_LO	"ERR_COUNT_STD_2A_LO" on page 434
277	ERR_COUNT_STD_2A_HI	"ERR_COUNT_STD_2A_HI" on page 434
278	ERR_COUNT_STD_3A_LO	"ERR_COUNT_STD_3A_LO" on page 434
279	ERR_COUNT_STD_3A_HI	"ERR_COUNT_STD_3A_HI" on page 434
280	ERR_COUNT_STD_0B_LO	"ERR_COUNT_STD_0B_LO" on page 434
281	ERR_COUNT_STD_0B_HI	"ERR_COUNT_STD_0B_HI" on page 434
282	ERR_COUNT_STD_1B_LO	"ERR_COUNT_STD_1B_LO" on page 434
283	ERR_COUNT_STD_1B_HI	"ERR_COUNT_STD_1B_HI" on page 435
284	ERR_COUNT_STD_2B_LO	"ERR_COUNT_STD_2B_LO" on page 435
285	ERR_COUNT_STD_2B_HI	"ERR_COUNT_STD_2B_HI" on page 435
286	ERR_COUNT_STD_3B_LO	"ERR_COUNT_STD_3B_LO" on page 435
287	ERR_COUNT_STD_3B_HI	"ERR_COUNT_STD_3B_HI" on page 435

4.6.1.5.1 LS_RST

Offset	Bit(s)	Field Name	Description	Type	Default Value
0	7:1	Reserved		RO	0
0	0	ls_rst_req	ls_rst setting/resetting. Polarity: positive.	R/W	1

4.6.1.5.2 AUX_RST

Offset	Bit(s)	Field Name	Description	Type	Default Value
1	7:1	Reserved		RO	0
1	0	aux_rst_req	Aux rest.	R/W	0

4.6.1.5.3 ERROR_IND

Error indication from various blocks

Offset	Bit(s)	Field Name	Description	Type	Default Value
2	7:2	Reserved		RO	0
2	1	error_frm		RO	0

2	0	error_phy		RO	0

4.6.1.5.4 DP_MODE

Offset	Bit(s)	Field Name	Description	Type	Default Value
3	7:1	Reserved		RO	0
3	0	mi_dp_mode	DP mode: tx=1, rx=0.	R/W	0

4.6.1.5.5 LANE_DATA_ENABLE

Enable for lanes 0,1,2,3

Offset	Bit(s)	Field Name	Description	Type	Default Value
4	7:4	Reserved		RO	0
4	3	mi_lane_data_enable_3		RO	0
4	2	mi_lane_data_enable_2		RO	0
4	1	mi_lane_data_enable_1		RO	0
4	0	mi_lane_data_enable_0		RO	0

4.6.1.5.6 MISC_STATUS_NO_CLR

Offset	Bit(s)	Field Name	Description	Type	Default Value
5	7:1	Reserved		RO	0
5	0	mi_status_no_clr	0: Status registers reset by read. 1: Status registers reset by write.	R/W	0

4.6.1.5.7 LS_CLK_SEL

Offset	Bit(s)	Field Name	Description	Type	Default Value
6	7:2	Reserved		RO	0
6	1:0	ls_clk_sel		R/W	3h

4.6.1.5.8 MISC_USR0

Offset	Bit(s)	Field Name	Description	Type	Default Value
7	7:6	Reserved		RO	0
7	5	mi_adapt_ip_link_init_usr0		R/Clr or R/W1C	0
7	4	mi_link_errors_b_usr0		R/Clr or R/W1C	0
7	3	mi_link_errors_a_usr0		R/Clr or R/W1C	0
7	2	mi_adapt_ip_conf_changed_usr0		R/Clr or R/W1C	0
7	1	mi_hpd_irq_det_usr0		R/Clr or R/W1C	0
7	0	mi_hpd_unplugged_det		RO	0

4.6.1.5.9 MISC_COUNTER1_L

Offset	Bit(s)	Field Name	Description	Type	Default Value
8	7:0	misc_counter1_lo		RO/1C	0

4.6.1.5.10 MISC_COUNTER1_H

Offset	Bit(s)	Field Name	Description	Type	Default Value
9	7:0	misc_counter1_hi		RO	0

4.6.1.5.11 MISC_COUNTER2_L

Offset	Bit(s)	Field Name	Description	Type	Default Value
10	7:0	misc_counter2_lo		R/Clr or R/W1C	0

4.6.1.5.12 MISC_COUNTER2_H

Offset	Bit(s)	Field Name	Description	Type	Default Value
11	7:0	misc_counter1_hi		RO	0

4.6.1.5.13 MISC_1USEC_FACTOR

Offset	Bit(s)	Field Name	Description	Type	Default Value
12	7:0	mi_1usec_factor		R/W	64

4.6.1.5.14 DWNSPRD_EN

Offset	Bit(s)	Field Name	Description	Type	Default Value
14	7:1	Reserved		RO	0
14	0	dp_in_ip_adapt_dwnsprd_en	Down spread enable.	R/W	0

4.6.1.5.15 TESTBUS_SEL

Offset	Bit(s)	Field Name	Description	Type	Default Value
15	7:3	Reserved		RO	0
15	2:0	testbus_sel	Test bus select: 0 = no selection 1h = Phy testbus 2h = DeFramer testbus 3h = aux testbus 4h = analog IF testbus	R/W	0

4.6.1.5.16 HPD_IRQ_DET_MIN_TIMER_LO

Offset	Bit(s)	Field Name	Description	Type	Default Value
16	7:0	mi_hpd_irq_det_min_timer_lo	hpd min timer for irq, 8 lsb.	R/W	0xA4

4.6.1.5.17 HPD_IRQ_DET_MIN_TIMER_MD

Offset	Bit(s)	Field Name	Description	Type	Default Value
17	7:0	mi_hpd_irq_det_min_timer_md	hpd min timer for irq, bits 15:8.	R/W	0x61

4.6.1.5.18 HPD_IRQ_DET_MIN_TIMER_HI

Offset	Bit(s)	Field Name	Description	Type	Default Value
18	7:0	mi_hpd_irq_det_min_timer_hi	hpd min timer for irq, bits 23:16.	R/W	0

4.6.1.5.19 HPD_IRQ_DET_MAX_TIMER_LO

Offset	Bit(s)	Field Name	Description	Type	Default Value
19	7:0	mi_hpd_irq_det_max_timer_lo	hpd max timer, bits 7:0.	R/W	0x3C

4.6.1.5.20 HPD_IRQ_DET_MAX_TIMER_MD

Offset	Bit(s)	Field Name	Description	Type	Default Value

20	7:0	mi_hpd_irq_det_max_timer_md	hpd max timer, bits 15:8.	R/W	0xOD

4.6.1.5.21 HPD_IRQ_DET_MAX_TIMER_HI

Offset	Bit(s)	Field Name	Description	Type	Default Value
21	7:0	mi_hpd_irq_det_max_timer_hi	hpd max timer, bits 23:16.	R/W	3

4.6.1.5.22 HPD_UNPLGED_DET_MIN_TIMER_LO

Offset	Bit(s)	Field Name	Description	Type	Default Value
22	7:0	mi_hpd_unplged_det_min_timer_lo	hpd unplugged timer, bits 7:0.	R/W	0x3C

4.6.1.5.23 HPD_UNPLGED_DET_MIN_TIMER_MD

Offset	Bit(s)	Field Name	Description	Type	Default Value
23	7:0	mi_hpd_unplged_det_min_timer_md	hpd unplugged timer, bits 15:8.	R/W	0x0F

4.6.1.5.24 HPD_UNPLGED_DET_MIN_TIMER_HI

Offset	Bit(s)	Field Name	Description	Type	Default Value
24	7:0	mi_hpd_unplged_det_min_timer_hi	hpd unplugged timer, bits 23:16.	R/W	3

4.6.1.5.25 HPD_IRQ_DET

Offset	Bit(s)	Field Name	Description	Type	Default Value
28	7:1	Reserved		RO	0
28	0	mi_hpd_irq_det_bit	irq detect. Clear on Write '0. Write '1' is not allowed.	R/Clr or R/W1C	0

4.6.1.5.26 HPD_RE_PLUGGED_DET

Offset	Bit(s)	Field Name	Description	Type	Default Value
29	7:1	Reserved		RO	0
29	0	hpd_re_plged_det_bit	hpd re-plugged detect. Clear on read or by Write '0. Write '1' is not allowed.	R/Clr or R/W1C	0

4.6.1.5.27 HPD_GEN_TIMER_LO

Offset	Bit(s)	Field Name	Description	Type	Default Value
30	7:0	mi_hpd_gen_timer_lo	hpd generation timer bits 7:0.	R/W	0xF8

4.6.1.5.28 HPD_GEN_TIMER_MD

Offset	Bit(s)	Field Name	Description	Type	Default Value
31	7:0	mi_hpd_gen_timer_md	hpd generation timer bits 15:8.	R/W	0x24

4.6.1.5.29 HPD_GEN_TIMER_HI

Offset	Bit(s)	Field Name	Description	Type	Default Value
32	7:0	mi_hpd_gen_timer_hi	hpd generation timer bits 23:16.	R/W	1

4.6.1.5.30 HPD_GEN

Offset	Bit(s)	Field Name	Description	Type	Default Value

33	7:1	Reserved		RO	0
33	0	mi_hpd_gen	Generate hpd.	R/W SC	0

4.6.1.5.31 HPD_BYPASS

Offset	Bit(s)	Field Name	Description	Type	Default Value
34	7:1	Reserved		RO	0
34	0	mi_hpd_bypass	Bypass hpd in.	R/W	0

4.6.1.5.32 HPD_STATUS

Offset	Bit(s)	Field Name	Description	Type	Default Value
35	7:1	Reserved		RO	0
35	0	dp_ip_adapt_hpd_sync	Status of hpd (out).	RO	0

4.6.1.5.33 HPD_STABLE_TIMER_LO

Offset	Bit(s)	Field Name	Description	Type	Default Value
36	36.7:0	mi_hpd_stable_timer_lo	Cycles to identify stable hpd, from rising hpd after it was unplugged. Bits 7:0. '0' is illegal.	R/W	1

4.6.1.5.34 HPD_STABLE_TIMER_MD

Offset	Bit(s)	Field Name	Description	Type	Default Value
37	7:0	mi_hpd_stable_timer_md	Cycles to identify stable hpd, from rising hpd after it was unplugged. Bits 15:8. '0' is illegal.	R/W	0

4.6.1.5.35 HPD_STABLE_TIMER_HI

Offset	Bit(s)	Field Name	Description	Type	Default Value
38	7:0	mi_hpd_stable_timer_hi	Cycles to identify stable hpd, from rising hpd after it was unplugged. Bits 23:16. '0' is illegal.	R/W	0

4.6.1.5.36 HPD_FILTER_TIMER_LO

Offset	Bit(s)	Field Name	Description	Type	Default Value
39	7:0	mi_hpd_filter_timer_lo	hpd filter timer, bits 7:0.	R/W	0

4.6.1.5.37 HPD_FILTER_TIMER_MD

Offset	Bit(s)	Field Name	Description	Type	Default Value
40	7:0	mi_hpd_filter_timer_md	hpd filter timer, bits 15:8.	R/W	0

4.6.1.5.38 HPD_FILTER_TIMER_HI

Offset	Bit(s)	Field Name	Description	Type	Default Value
41	7:0	mi_hpd_filter_timer_hi	hpd filter timer, bits 23:16.	R/W	0

4.6.1.5.39 HPD_STABLE_STATUS

Offset	Bit(s)	Field Name	Description	Type	Default Value

42	7:1	Reserved		RO	0
42	0	mi_hpd_stable		RO	0

4.6.1.5.40 MISC_COUNTER3_L

Offset	Bit(s)	Field Name	Description	Type	Default Value
43	7:0	misc_counter3_lo		RO/1C	0

4.6.1.5.41 MISC_COUNTER3_H

Offset	Bit(s)	Field Name	Description	Type	Default Value
44	7:0	misc_counter3_hi		RO	0

4.6.1.5.42 MISC_COUNTER4_L

Offset	Bit(s)	Field Name	Description	Type	Default Value
45	7:0	misc_counter4_lo		R/Clr or R/W1C	0

4.6.1.5.43 MISC_COUNTER4_H

Offset	Bit(s)	Field Name	Description	Type	Default Value
46	7:0	misc_counter4_hi		RO	0

4.6.1.5.44 DP_IP_ADAPT_CONF_CHANGE_SET

Offset	Bit(s)	Field Name	Description	Type	Default Value
48	7:1	Reserved		RO	0
48	0	mi_conf_change_set	Configuration data changed from ip to adapt.	R/W SC	0

4.6.1.5.45 DP_IP_ADAPT_CONF_DATA0

Offset	Bit(s)	Field Name	Description	Type	Default Value
49	7:0	mi_ip_adapt_conf_data0	Configuration data0 from ip to adapt.	R/W	0

4.6.1.5.46 DP_IP_ADAPT_CONF_DATA1

Offset	Bit(s)	Field Name	Description	Type	Default Value
50	7:0	mi_ip_adapt_conf_data1	Configuration data1 from ip to adapt.	R/W	0

4.6.1.5.47 DP_IP_ADAPT_CONF_DATA2

Offset	Bit(s)	Field Name	Description	Type	Default Value
51	7:0	mi_ip_adapt_conf_data2	Configuration data2 from ip to adapt.	R/W	0

4.6.1.5.48 DP_ADAPT_IP_CONF_CHANGED

Offset	Bit(s)	Field Name	Description	Type	Default Value
52	7:1	Reserved		RO	0
52	0	mi_adapt_ip_conf_ changed	Configuration data had changed. Clear by read or by write '0'. Write '1' is not allowed.	R/Clr or R/W1C	0

4.6.1.5.49 DP_ADAPT_IP_CONF_DATA0

Offset	Bit(s)	Field Name	Description	Type	Default Value

53	7:0	mi_adapt_ip_conf_data0	Adapt to ip configuration data0.	RO	0

4.6.1.5.50 DP_ADAPT_IP_CONF_DATA1

Offset	Bit(s)	Field Name	Description	Type	Default Value
54	7:0	mi_adapt_ip_conf_data1	Adapt to ip configuration data1.	RO	0

4.6.1.5.51 DP_ADAPT_IP_CONF_DATA2

Offset	Bit(s)	Field Name	Description	Type	Default Value
55	7:0	mi_adapt_ip_conf_data2	Adapt to ip configuration data2.	RO	0

4.6.1.5.52 ERR_USR0_COUNT_TH_LO_A

Offset	Bit(s)	Field Name	Description	Type	Default Value
77	7:0	mi_usr0_error_count_th_lo_a		R/W	0xFF

4.6.1.5.53 ERR_USR0_COUNT_TH_MD_A

Offset	Bit(s)	Field Name	Description	Type	Default Value
78	7:0	mi_usr0_error_count_th_md_a		R/W	0xFF

4.6.1.5.54 ERR_USR0_COUNT_TH_HI_A

Offset	Bit(s)	Field Name	Description	Type	Default Value
79	7:0	mi_usr0_error_count_th_hi_a		R/W	0xFF

4.6.1.5.55 ERR_USR0_COUNT_TH_LO_B

Offset	Bit(s)	Field Name	Description	Type	Default Value
80	7:0	mi_usr0_error_count_th_lo_b		R/W	0xFF

4.6.1.5.56 ERR_USR0_COUNT_TH_MD_B

Offset	Bit(s)	Field Name	Description	Type	Default Value
81	7:0	mi_usr0_error_count_th_md_b		R/W	0xFF

4.6.1.5.57 ERR_USR0_COUNT_TH_HI_B

Offset	Bit(s)	Field Name	Description	Type	Default Value
82	7:0	mi_usr0_error_count_th_hi_b		R/W	0xFF

4.6.1.5.58 ERR_WINDOW_WIDTH_LO_A

Offset	Bit(s)	Field Name	Description	Type	Default Value
83	7:0	mi_err_window_width_lo_a		R/W	0xFF

4.6.1.5.59 ERR_WINDOW_WIDTH_M0_A

Offset	Bit(s)	Field Name	Description	Type	Default Value
84	7:0	mi_err_window_width_m0_a		R/W	0xFF

4.6.1.5.60 ERR_WINDOW_WIDTH_M1_A

Offset	Bit(s)	Field Name	Description	Type	Default Value
85	7:0	mi_err_window_width_m1_a		R/W	0xFF

4.6.1.5.61 ERR_WINDOW_WIDTH_HI_A

Offset	Bit(s)	Field Name	Description	Type	Default Value
86	7:0	mi_err_window_width_hi_a		R/W	0xFF

4.6.1.5.62 ERR_COUNT_TH_LO_A

Offset	Bit(s)	Field Name	Description	Type	Default Value
87	7:0	mi_error_count_th_lo_a		R/W	0

4.6.1.5.63 ERR_COUNT_TH_MD_A

Offset	Bit(s)	Field Name	Description	Type	Default Value
88	7:0	mi_error_count_th_md_a		R/W	1

4.6.1.5.64 ERR_COUNT_TH_HI_A

Offset	Bit(s)	Field Name	Description	Type	Default Value
89	7:0	mi_error_count_th_hi_a		R/W	2

4.6.1.5.65 ERR_WINDOW_WIDTH_LO_B

Offset	Bit(s)	Field Name	Description	Type	Default Value
90	7:0	mi_err_window_width_lo_b		R/W	0xFF

4.6.1.5.66 ERR_WINDOW_WIDTH_M0_B

Offset	Bit(s)	Field Name	Description	Type	Default Value
91	7:0	mi_err_window_width_m0_b		R/W	0xFF

4.6.1.5.67 ERR_WINDOW_WIDTH_M1_B

Offset	Bit(s)	Field Name	Description	Type	Default Value
92	7:0	mi_err_window_width_m1_b		R/W	0xFF

4.6.1.5.68 ERR_WINDOW_WIDTH_HI_B

Offset	Bit(s)	Field Name	Description	Type	Default Value
93	7:0	mi_err_window_width_hi_b		R/W	0xFF

4.6.1.5.69 ERR_SELECT

Offset	Bit(s)	Field Name	Description	Type	Default Value
94	7:4	mi_error_select_b		R/W	0x5
94	3:0	mi_error_select_a		R/W	0x5

4.6.1.5.70 ERR_COUNT_TH_LO_B

Offset	Bit(s)	Field Name	Description	Type	Default Value
95	7:0	mi_error_count_th_lo_b		R/W	0

4.6.1.5.71 ERR_COUNT_TH_MD_B

Offset	Bit(s)	Field Name	Description	Type	Default Value
96	7:0	mi_error_count_th_md_b		R/W	1

4.6.1.5.72 ERR_COUNT_TH_HI_B

Offset	Bit(s)	Field Name	Description	Type	Default Value

97	7:0	mi_error_count_th_hi_b		R/W	2

4.6.1.5.73 ERR_COUNT_0A_LO

Offset	Bit(s)	Field Name	Description	Type	Default Value
98	7:0	mi_err_count_0a_hc_lo		RO	0

4.6.1.5.74 ERR_COUNT_0A_MD

Offset	Bit(s)	Field Name	Description	Type	Default Value
99	7:0	mi_err_count_0a_hc_md		RO	0

4.6.1.5.75 ERR_COUNT_0A_HI

Offset	Bit(s)	Field Name	Description	Type	Default Value
100	7:0	mi_err_count_0a_hc_hi		RO	0

4.6.1.5.76 ERR_COUNT_1A_LO

Offset	Bit(s)	Field Name	Description	Type	Default Value
101	7:0	mi_err_count_1a_hc_lo		RO	0

4.6.1.5.77 ERR_COUNT_1A_MD

Offset	Bit(s)	Field Name	Description	Type	Default Value
102	7:0	mi_err_count_1a_hc_md		RO	0

4.6.1.5.78 ERR_COUNT_1A_HI

Offset	Bit(s)	Field Name	Description	Type	Default Value
103	7:0	mi_err_count_1a_hc_hi		RO	0

4.6.1.5.79 ERR_COUNT_2A_LO

Offset	Bit(s)	Field Name	Description	Type	Default Value
104	7:0	mi_err_count_2a_hc_lo		RO	0

4.6.1.5.80 ERR_COUNT_2A_MD

Offset	Bit(s)	Field Name	Description	Type	Default Value
105	7:0	mi_err_count_2a_hc_md		RO	0

4.6.1.5.81 ERR_COUNT_2A_HI

Offset	Bit(s)	Field Name	Description	Type	Default Value
106	7:0	mi_err_count_2a_hc_hi		RO	0

4.6.1.5.82 ERR_COUNT_3A_LO

Offset	Bit(s)	Field Name	Description	Type	Default Value
107	7:0	mi_err_count_3a_hc_lo		RO	0

4.6.1.5.83 ERR_COUNT_3A_MD

Offset	Bit(s)	Field Name	Description	Type	Default Value
108	7:0	mi_err_count_3a_hc_md		RO	0

4.6.1.5.84 ERR_COUNT_3A_HI

Offset	Bit(s)	Field Name	Description	Type	Default Value
109	7:0	mi_err_count_3a_hc_hi		RO	0

4.6.1.5.85 ERR_COUNT_0B_LO

Offset	Bit(s)	Field Name	Description	Type	Default Value
110	7:0	mi_err_count_0b_hc_lo		RO	0

4.6.1.5.86 ERR_COUNT_0B_MD

Offset	Bit(s)	Field Name	Description	Type	Default Value
111	7:0	mi_err_count_0b_hc_md		RO	0

4.6.1.5.87 ERR_COUNT_0B_HI

Offset	Bit(s)	Field Name	Description	Type	Default Value
112	7:0	mi_err_count_0b_hc_hi		RO	0

4.6.1.5.88 ERR_COUNT_1B_LO

Offset	Bit(s)	Field Name	Description	Type	Default Value
113	7:0	mi_err_count_1b_hc_lo		RO	0

4.6.1.5.89 ERR_COUNT_1B_MD

Offset	Bit(s)	Field Name	Description	Type	Default Value
114	7:0	mi_err_count_1b_hc_md		RO	0

4.6.1.5.90 ERR_COUNT_1B_HI

Offset	Bit(s)	Field Name	Description	Type	Default Value
115	7:0	mi_err_count_1b_hc_hi		RO	0

4.6.1.5.91 ERR_COUNT_2B_LO

Offset	Bit(s)	Field Name	Description	Type	Default Value
116	7:0	mi_err_count_2b_hc_lo		RO	0

4.6.1.5.92 ERR_COUNT_2B_MD

Offset	Bit(s)	Field Name	Description	Type	Default Value
117	7:0	mi_err_count_2b_hc_md		RO	0

4.6.1.5.93 ERR_COUNT_2B_HI

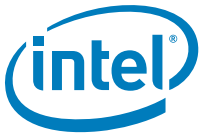
Offset	Bit(s)	Field Name	Description	Type	Default Value
118	7:0	mi_err_count_2b_hc_hi		RO	0

4.6.1.5.94 ERR_COUNT_3B_LO

Offset	Bit(s)	Field Name	Description	Type	Default Value
119	7:0	mi_err_count_3b_hc_lo		RO	0

4.6.1.5.95 ERR_COUNT_3B_MD

Offset	Bit(s)	Field Name	Description	Type	Default Value
120	7:0	mi_err_count_3b_hc_md		RO	0



4.6.1.5.96 ERR_COUNT_3B_HI

Offset	Bit(s)	Field Name	Description	Type	Default Value
121	7:0	mi_err_count_3b_hc_hi		RO	0

4.6.1.5.97 ERR_FLAGS_A

Offset	Bit(s)	Field Name	Description	Type	Default Value
122	7:4	Reserved		RO	0
122	3	mi_err_flag_3a		R/Clr	0
122	2	mi_err_flag_2a		R/Clr	0
122	1	mi_err_flag_1a		R/Clr	0
122	0	mi_err_flag_0a		R/Clr	0

4.6.1.5.98 ERR_FLAGS_B

Offset	Bit(s)	Field Name	Description	Type	Default Value
123	7:4	Reserved		RO	0
123	3	mi_err_flag_3b		R/Clr	0
123	2	mi_err_flag_2b		R/Clr	0
123	1	mi_err_flag_1b		R/Clr	0
123	0	mi_err_flag_0b		R/Clr	0

4.6.1.5.99 ERR_LOCK_COUNT_A

Offset	Bit(s)	Field Name	Description	Type	Default Value
124	7:4	Reserved		RO	0
124	3	mi_err_count_lock_3a		R/W SC	0
124	2	mi_err_count_lock_2a		R/W SC	0
124	1	mi_err_count_lock_2a		R/W SC	0
124	0	mi_err_count_lock_0a		R/W SC	0

4.6.1.5.100 ERR_LOCK_COUNT_B

Offset	Bit(s)	Field Name	Description	Type	Default Value
125	7:4	Reserved		RO	0
125	3	mi_err_count_lock_3b		R/W SC	0
125	2	mi_err_count_lock_2b		R/W SC	0
125	1	mi_err_count_lock_2b		R/W5SC	0
125	0	mi_err_count_lock_0b		R/W SC	0

4.6.1.5.101 GP0

Offset	Bit(s)	Field Name	Description	Type	Default Value
140	7:0	mi_gp0	General purpose.	R/W	0

4.6.1.5.102 GP1

Offset	Bit(s)	Field Name	Description	Type	Default Value
141	7:0	mi_gp1	General purpose.	R/W	0

4.6.1.5.103 GP2

Offset	Bit(s)	Field Name	Description	Type	Default Value
142	7:0	mi_gp2	General purpose.	R/W	0

4.6.1.5.104 GP3

Offset	Bit(s)	Field Name	Description	Type	Default Value
143	7:0	mi_gp3	General purpose.	R/W	0

4.6.1.5.105 GP4

Offset	Bit(s)	Field Name	Description	Type	Default Value
144	7:0	mi_gp4	General purpose.	R/W	0

4.6.1.5.106 GP5

Offset	Bit(s)	Field Name	Description	Type	Default Value
145	7:0	mi_gp5	General purpose.	R/W	0

4.6.1.5.107 GP6

Offset	Bit(s)	Field Name	Description	Type	Default Value
146	7:0	mi_gp6	General purpose.	R/W	0

4.6.1.5.108 GP7

Offset	Bit(s)	Field Name	Description	Type	Default Value
147	7:0	mi_gp7	General purpose.	R/W	0

4.6.1.5.109 GP8

Offset	Bit(s)	Field Name	Description	Type	Default Value
148	7:0	mi_gp8	General purpose.	R/W	0

4.6.1.5.110 GP9

Offset	Bit(s)	Field Name	Description	Type	Default Value
149	7:0	mi_gp9	General purpose.	R/W	0

4.6.1.5.111 GP10

Offset	Bit(s)	Field Name	Description	Type	Default Value
150	7:0	mi_gp10	General purpose.	R/W	0

4.6.1.5.112 GP11

Offset	Bit(s)	Field Name	Description	Type	Default Value
151	7:0	mi_gp11	General purpose.	R/W	0

4.6.1.5.113 GP12

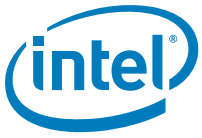
Offset	Bit(s)	Field Name	Description	Type	Default Value
152	7:0	mi_gp12	General purpose.	R/W	0

4.6.1.5.114 GP13

Offset	Bit(s)	Field Name	Description	Type	Default Value
153	7:0	mi_gp13	General purpose.	R/W	0

4.6.1.5.115 GP14

Offset	Bit(s)	Field Name	Description	Type	Default Value
154	7:0	mi_gp14	General purpose.	R/W	0



4.6.1.5.116 GP15

Offset	Bit(s)	Field Name	Description	Type	Default Value
155	7:0	mi_gp15	General purpose.	R/W	0

4.6.1.5.117 ERR_COUNT_STD_0A_LO

Offset	Bit(s)	Field Name	Description	Type	Default Value
272	7:0	mi_err_count_std_0a_lo		RO	0

4.6.1.5.118 ERR_COUNT_STD_0A_HI

Offset	Bit(s)	Field Name	Description	Type	Default Value
273	7:0	mi_err_count_std_0a_hi		RO	0

4.6.1.5.119 ERR_COUNT_STD_1A_LO

Offset	Bit(s)	Field Name	Description	Type	Default Value
274	7:0	mi_err_count_std_1a_lo		RO	0

4.6.1.5.120 ERR_COUNT_STD_1A_HI

Offset	Bit(s)	Field Name	Description	Type	Default Value
275	7:0	mi_err_count_std_1a_hi		RO	0

4.6.1.5.121 ERR_COUNT_STD_2A_LO

Offset	Bit(s)	Field Name	Description	Type	Default Value
276	7:0	mi_err_count_std_2a_lo		RO	0

4.6.1.5.122 ERR_COUNT_STD_2A_HI

Offset	Bit(s)	Field Name	Description	Type	Default Value
277	7:0	mi_err_count_std_2a_hi		RO	0

4.6.1.5.123 ERR_COUNT_STD_3A_LO

Offset	Bit(s)	Field Name	Description	Type	Default Value
278	7:0	mi_err_count_std_3a_lo		RO	0

4.6.1.5.124 ERR_COUNT_STD_3A_HI

Offset	Bit(s)	Field Name	Description	Type	Default Value
279	7:0	mi_err_count_std_3a_hi		RO	0

4.6.1.5.125 ERR_COUNT_STD_0B_LO

Offset	Bit(s)	Field Name	Description	Type	Default Value
280	7:0	mi_err_count_std_0b_lo		RO	0

4.6.1.5.126 ERR_COUNT_STD_0B_HI

Offset	Bit(s)	Field Name	Description	Type	Default Value
281	7:0	mi_err_count_std_0b_hi		RO	0

4.6.1.5.127 ERR_COUNT_STD_1B_LO

Offset	Bit(s)	Field Name	Description	Type	Default Value
282	7:0	mi_err_count_std_1b_lo		RO	0

4.6.1.5.128 ERR_COUNT_STD_1B_HI

Offset	Bit(s)	Field Name	Description	Type	Default Value
283	7:0	mi_err_count_std_1b_hi		RO	0

4.6.1.5.129 ERR_COUNT_STD_2B_LO

Offset	Bit(s)	Field Name	Description	Type	Default Value
284	7:0	mi_err_count_std_2b_lo		RO	0

4.6.1.5.130 ERR_COUNT_STD_2B_HI

Offset	Bit(s)	Field Name	Description	Type	Default Value
285	7:0	mi_err_count_std_2b_hi		RO	0

4.6.1.5.131 ERR_COUNT_STD_3B_LO

Offset	Bit(s)	Field Name	Description	Type	Default Value
286	7:0	mi_err_count_std_3b_lo		RO	0

4.6.1.5.132 ERR_COUNT_STD_3B_HI

Offset	Bit(s)	Field Name	Description	Type	Default Value
287	7:0	mi_err_count_std_3b_hi		RO	0

4.6.1.6 Bank 7 - Analog Interface

Table 160 is a summary of the Analog registers without registers description. The detailed description of the register list is given in the following sections.

Table 160. 0xE00 Analog Interface Registers Summary

Register Number	Register Name	Section #
6	CDR0_PD_CNTRL	"CDR0_PD_CNTRL" on page 435
224	EQ0_WIDTH_OK	"EQ0_WIDTH_OK" on page 435
225	EQ1_WIDTH_OK	"EQ1_WIDTH_OK" on page 436
226	EQ2_WIDTH_OK	"EQ2_WIDTH_OK" on page 436
227	EQ3_WIDTH_OK	"EQ3_WIDTH_OK" on page 436

4.6.1.6.1 CDR0_PD_CNTRL

Offset	Bit(s)	Field Name	Description	Type	Default Value
6	7	an_cdr0_reset	CDR reset.	R/W	1
6	4:3	SPEED	Bit rate control: 2'b00 - low bit rate (1.62Gb/s). 2'b01 - high bit rate (2.7Gb/s). 2'b10 – high bit rate 2 (5.4Gb/s)	R/W	0

4.6.1.6.2 EQ0_WIDTH_OK

Offset	Bit(s)	Field Name	Description	Type	Default Value
224	7:1	Reserved		RO	0

224	0	an_eq0_width_ok	This is another way to read the PLL_LOCK indication for lane 0 from the PHY	RO	0

4.6.1.6.3 EQ1_WIDTH_OK

Offset	Bit(s)	Field Name	Description	Type	Default Value
225	7:1	Reserved		RO	0
225	0	an_eq1_width_ok	This is another way to read the PLL_LOCK indication for lane 1 from the PHY	RO	0

4.6.1.6.4 EQ2_WIDTH_OK

Offset	Bit(s)	Field Name	Description	Type	Default Value
226	7:1	Reserved		RO	0
226	0	an_eq2_width_ok	This is another way to read the PLL_LOCK indication for lane 2from the PHY	RO	0

4.6.1.6.5 EQ3_WIDTH_OK

Offset	Bit(s)	Field Name	Description	Type	Default Value
227	7:1	Reserved		RO	0
227	0	an_eq3_width_ok	This is another way to read the PLL_LOCK indication for lane 3 from the PHY	RO	0

4.6.1.7 Bank 11 Phy Digital Lane

Table 161. 0x1600 Phy Digital Lane Registers Summary

Register Number	Register Name	Section #
92, 220, 348, 476	GP_LANE_REG	See section 4.6.1.7.1
66, 194, 322, 450	CUR_PI_VAL_L	See section 4.6.1.7.2
67, 195, 323, 451	CUR_PI_VAL_H	See section 4.6.1.7.3
31, 159, 287, 415	EYEMON_SYMBOL_COUNT_L	See section 4.6.1.7.4
32, 160, 288, 416	EYEMON_SYMBOL_COUNT_M	See section 4.6.1.7.5
33, 161, 289, 417	EYEMON_SYMBOL_COUNT_H	See section 4.6.1.7.6
28, 156, 284, 412	EYEMON_MASK_SEL	See section 4.6.1.7.7
0, 128, 256, 384	RX_EYEMON_VREF	See section 4.6.1.7.8
82, 210, 338, 466	RX_EYEMON_PHSHIFT_DIR	See section 4.6.1.7.9
83, 211, 339, 467	RX_EYEMON_PHSHIFT_STROBE	See section 4.6.1.7.10
27, 155, 283, 411	EYEMON_MODE	See section 4.6.1.7.11
23, 151, 279, 407	EYEMON_GO	See section 4.6.1.7.12
52, 180, 308, 436	EYEMON_DONE	See section 4.6.1.7.13
43, 171, 299, 427	EYEMON_ERR_COUNT_L	See section 4.6.1.7.14
44, 172, 300, 428	EYEMON_ERR_COUNT_M	See section 4.6.1.7.15
45, 173, 301, 429	EYEMON_ERR_COUNT_H	See section 4.6.1.7.16
46, 174, 302, 430	EYEMON_ERR_COUNT_VH	See section 4.6.1.7.17

4.6.1.7.1 GP_LANE_REG

Offset	Bit(s)	Field Name	Description	Type	Default Value
92 220 348 476	7:0	gp_lane_reg	A General Purpose register for lane 0, used to overcome a bug in EYEMON_VREF writing: value written to this register will be mirrored to eyemon_vref[7:0] output. [7] is sign bit (1 is negative). [6:0] is magnitude. 1.87mV per step	RW	0

4.6.1.7.2 CUR_PI_VAL_L

Offset	Bit(s)	Field Name	Description	Type	Default Value
66 194 322 450	7:0	cur_pi_val[7:0]	Represents bits 7:0 of the current offset of the pi_clk	RO	0

4.6.1.7.3 CUR_PI_VAL_H

Offset	Bit(s)	Field Name	Description	Type	Default Value
67 195 323 451	7:2	Reserved	Reserved	RO	0
	1:0	car_pi_val[9:8]	Represents bits 9:8 of the current offset of the pi_clk	RO	0

4.6.1.7.4 EYEMON_SYMBOL_COUNT_L

Offset	Bit(s)	Field Name	Description	Type	Default Value
31 159 287 415	7:0	eyemon_symbol_count[7:0]	Represents bits 7:0 of the number of symbols the eyemon will compare	RW	0

4.6.1.7.5 EYEMON_SYMBOL_COUNT_M

Offset	Bit(s)	Field Name	Description	Type	Default Value
32 160 288 416	7:0	eyemon_symbol_count[15:8]	Represents bits 15:8 of the number of symbols the eyemon will compare	RW	0

4.6.1.7.6 EYEMON_SYMBOL_COUNT_H

Offset	Bit(s)	Field Name	Description	Type	Default Value
33 161 289 417	7:4	Reserved	Reserved	RW	0
	3:0	eyemon_symbol_count[19:16]	Represents bits 19:16 of the number of symbols the eyemon will compare	RW	0

4.6.1.7.7 EYEMON_MASK_SEL

Offset	Bit(s)	Field Name	Description	Type	Default Value
	7:3	Reserved	Reserved		
28 156 284 412	2:0	eyemon_mask_sel	eyemon bits to compare: 0. Compare all 1. Compare only bits that are after a 1 2. Compare only bits that are after a 0 3. Compare all eyemon bus to 0 (1 counter) 4. Compare all eyemon bus to 1 (0 counter) 5. Compare all data bus to 0 (1 counter) 6. Compare all data bus to 1 (0 counter) Compare only bits that are 1 and come exactly eyemon_mask_shift bits after another 1	RW	0

4.6.1.7.8 RX_EYEMON_VREF

Offset	Bit(s)	Field Name	Description	Type	Default Value
0 128 256 384	7:0	rx_eyemon_vref	Reference voltage for the debug slicer [7] is sign (0 - positive; 1 - negative) [6:0] represent absolute value	RW	0

4.6.1.7.9 RX_EYEMON_PHSHIFT_DIR

Offset	Bit(s)	Field Name	Description	Type	Default Value
	7:1	Reserved	Reserved	RO	0
82 210 338 466	0	rx_eyemon_phshift_dir	Direction in which to change the offset of pi_clk at strobe PI clock phase shift direction 1'b0 - left (decrement phase) 1'b1 - right (increment phase)	RW	0

4.6.1.7.10 RX_EYEMON_PHSHIFT_STROBE

Offset	Bit(s)	Field Name	Description	Type	Default Value
	7:1	Reserved	Reserved	RO	0
83 211 339 467	0	rx_eyemon_phshift_strobe	When set, will create a pulse towards the PHY indicating a single step of the pi_clk offset : 48 steps per UI when rate > 1G (incl. all DP rates) 96 steps per UI when 0.5G < rate < 1G 192 steps per UI when rate < 0.5G This bit is self-clearing	RW	0

4.6.1.7.11 EYEMON_MODE

Offset	Bit(s)	Field Name	Description	Type	Default Value
	7:2	Reserved	Reserved	RO	0
27 155 283 411	1:0	eyemon_mode	Eye Monitor mode: 0. Alignment search 1. Single search using previously found alignment 2. Scan an analog parameter until first time errors count cross threshold 3. Scan an analog parameter for mean error (until first time errors count cross a second threshold)	RW	0

4.6.1.7.12 EYEMON_GO

Offset	Bit(s)	Field Name	Description	Type	Default Value
23	7:1	Reserved	Reserved	RO	0
151 279 407	0	eyemon_go	Activation for eye monitor The signal is level and rising edge is a trigger. Self-clearing bit. Read always zero.	RW	0

4.6.1.7.13 EYEMON_DONE

Offset	Bit(s)	Field Name	Description	Type	Default Value
52	7:1	Reserved	Reserved	RO	0
180 308 436	0	eyemon_done_h_latch	EYEMON operation done The signal is level. Clears on eyemon_go pulse	RW	0

4.6.1.7.14 EYEMON_ERR_COUNT_L

Offset	Bit(s)	Field Name	Description	Type	Default Value
43 171 299 427	7:0	emn_err_count[7:0]	Bits 7:0 of the error count from EMN	RW	0

4.6.1.7.15 EYEMON_ERR_COUNT_M

Offset	Bit(s)	Field Name	Description	Type	Default Value
44 172 300 428	7:0	emn_err_count[15:8]	Bits 15:8 of the error count from EMN	RW	0

4.6.1.7.16 EYEMON_ERR_COUNT_H

Offset	Bit(s)	Field Name	Description	Type	Default Value
45 173 301 429	7:0	emn_err_count[23:16]	Bits 23:16 of the error count from EMN	RW	0

4.6.1.7.17 EYEMON_ERR_COUNT_VH

Offset	Bit(s)	Field Name	Description	Type	Default Value
46 174 302 430	7:2	Reserved	Reserved	RO	0
	1:0	emn_err_count[25:24]	Bits 25:24 of the error count from EMN	RW	0

4.6.1.8 Bank 12- Digital PHY Common

Table 162 provides a summary of the PHY_DIG_CMN registers without registers description. The detailed description of the register list is given in the following sections.

Table 162. 0x800 PHY_DIG_CMN Registers Summary

Register Number	Register Name	Section #
0	AUX_CTRL	
1	RX_MODE	
2	DP_RATE	
3	REFCLK_SEL	
4	RX_EN	
5	CM_AMON_SEL	
6	CM_CTRL	
7	CM_BG_BIASTUNE	
8	CM_RESTUNE_SET	
9	CM_RESTUNE_MON	
10	RX_RST_N	

Table 162. 0x800 PHY_DIG_CMN Registers Summary

Register Number	Register Name	Section #
11	SIPO_RST_N	
12	FORCE_PLL_LOCK	
13	RX_PLL_LOCK	
14	RX_PLL_PRELOCK	
15	RTL_IN_CTRL_PI0_CTLE1	
16	ALLOW_RTL_EYEMON_CTRL	
17	ALLOW_RTL_CTLE_CTRL_ADR	
18	ALLOW_RTL_ERRSLCR_OFST_CTL	
19	ALLOW_RTL_CML2CMOS_OFST_CTL	
20	ALLOW_RTL_810_CTL	
21	RX_EYEMON_CTRL	
22	RX_SIPO_10BIT_ADR	
23	COARSE_CAL_CTRL	
24	PI_CAL_CTRL	
25	PI_CAL_DONE_ADR	
26	PI_COARSE_CAL_SAFE_DIST_ADR	
27	DONT_WAIT_IN_PLL_MODE_ADR	
28	PD_STABLE_TIMER_L	
29	PD_STABLE_TIMER_H	
30	PD_SETUP_TIMER_L	
31	PD_SETUP_TIMER_H	
32	PI_CAL_EYEMON_SCAN_THR0_L	
33	PI_CAL_EYEMON_SCAN_THR0_H	
34	PI_CAL_EYEMON_SCAN_THR1_L	
35	PI_CAL_EYEMON_SCAN_THR1_H	
36	FINE_SCAN_WIDTH_ADR	
37	RESET_PI_FSMS_ADR	
38	reserved	
39	RX_DATA_SWIZZLE_EN	
40	EYEDATA_SWIZZLE_EN	
41	reserved	
42	REARNG_EVENODD_RX_DATA	
43	REARNG_EVENODD_EYEDATA	
44	DATA_INV	
45	EMN_DATA_CTRL	
46	Reserved	
47	PI_ROLL_DELAY	
48	RREF_CTRL	
49	SYMB_LOCK_EN_810	
50	SYMB_RELOCK_810	
51	SYMB_LOCK_810	
52	SYMB_LOCK_STABLE_810	
53	MISC_CLK_SEL	
54	TMDS_CLK_LANE_EN	

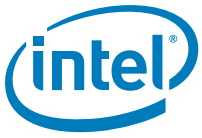


Table 162. 0x800 PHY_DIG_CMN Registers Summary

Register Number	Register Name	Section #
55	EYEMON_ERR_SAMPLE	
56	EYEMON_SCAN_STABLE_TIME_L	
57	EYEMON_SCAN_STABLE_TIME_H	
58	SELECT_CTLE	
59	RESET_CTLE_FSMS	
60	EYE_HEIGHT_THR_L	
61	EYE_HEIGHT_THR_H	
62	FIRST_CTLE_INDEX	
63	LAST_CTLE_INDEX	
64	EXCELLENT_WIDTH_L	
65	EXCELLENT_WIDTH_H	
66	EXCELLENT_HEIGHT_L	
67	EXCELLENT_HEIGHT_H	
68	HALF_EYE_WIDTH_L	
69	HALF_EYE_WIDTH_H	
70..75	Reserved	
76	SCANNING_THR_L	
77	SCANNING_THR_H	
78	CTLE_SELECTED_ADR	
79	CML2CMOS_SHORT	
80	CACHE_CTRL0	
81	CACHE_CTRL1	
82	CACHE_CTRL2	
83	CACHE_CTRL3	
84	TERMINATIONS_CACHE	
85	ALIGN_SYMB_COUNT_L	
86	ALIGN_SYMB_COUNT_M	
87	ALIGN_SYMB_COUNT_H	
88	MEASURE_SYMB_COUNT_L	
89	MEASURE_SYMB_COUNT_M	
90	MEASURE_SYMB_COUNT_H	
91	USE_TWOSCOMP2SIGNED	
92	USE_SIGNLE_RST	
93	PLL_LOCK_TIMER_L	
94	PLL_LOCK_TIMER_H	
95	LOCK_VERIFY_TIMER_L	
96	LOCK_VERIFY_TIMER_H	
97	COUNT810_ERRORS_TIMER_L	
98	COUNT810_ERRORS_TIMER_H	
99	SYMB_RELOCK_TIMER	
100	EYEMON_PHSHIFT_STROBE_TIMER	
101	NOF_ALLOWED_810_ERRROS	
102	USE_810	
103	PI_CAL_EN	

Table 162. 0x800 PHY_DIG_CMN Registers Summary

Register Number	Register Name	Section #
104	PI_PD_EN	
105	PI_PD_OUT	
106	RESERVED_EEPROM_0	
107	RESERVED_EEPROM_1	
108	RESERVED_EEPROM_2	
109	CM_RESERVED_IN	
110	CM_RESERVED_OUT	
111	GP_CMN_REG0	
112	GP_CMN_REG1	
113..223	Reserved	
236..239	Reserved	
252..255	Reserved	
256	CTLE_CFG_00_VAL_L	
257	CTLE_CFG_00_VAL_M	
258	CTLE_CFG_00_VAL_H	
259	CTLE_CFG_01_VAL_L	
260	CTLE_CFG_01_VAL_M	
261	CTLE_CFG_01_VAL_H	
262	CTLE_CFG_02_VAL_L	
263	CTLE_CFG_02_VAL_M	
264	CTLE_CFG_02_VAL_H	
265	CTLE_CFG_03_VAL_L	
266	CTLE_CFG_03_VAL_M	
267	CTLE_CFG_03_VAL_H	
268	CTLE_CFG_04_VAL_L	
269	CTLE_CFG_04_VAL_M	
270	CTLE_CFG_04_VAL_H	
271	CTLE_CFG_05_VAL_L	
272	CTLE_CFG_05_VAL_M	
273	CTLE_CFG_05_VAL_H	
274	CTLE_CFG_06_VAL_L	
275	CTLE_CFG_06_VAL_M	
276	CTLE_CFG_06_VAL_H	
277	CTLE_CFG_07_VAL_L	
278	CTLE_CFG_07_VAL_M	
279	CTLE_CFG_07_VAL_H	
280	CTLE_CFG_08_VAL_L	
281	CTLE_CFG_08_VAL_M	
282	CTLE_CFG_08_VAL_H	
283	CTLE_CFG_09_VAL_L	
284	CTLE_CFG_09_VAL_M	
285	CTLE_CFG_09_VAL_H	
286	CTLE_CFG_0A_VAL_L	
287	CTLE_CFG_0A_VAL_M	

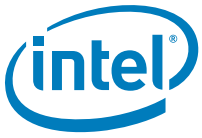


Table 162. 0x800 PHY_DIG_CMN Registers Summary

Register Number	Register Name	Section #
288	CTLE_CFG_0A_VAL_H	
289	CTLE_CFG_0B_VAL_L	
290	CTLE_CFG_0B_VAL_M	
291	CTLE_CFG_0B_VAL_H	
292	CTLE_CFG_0C_VAL_L	
293	CTLE_CFG_0C_VAL_M	
294	CTLE_CFG_0C_VAL_H	
295	CTLE_CFG_0D_VAL_L	
296	CTLE_CFG_0D_VAL_M	
297	CTLE_CFG_0D_VAL_H	
298	CTLE_CFG_0E_VAL_L	
299	CTLE_CFG_0E_VAL_M	
300	CTLE_CFG_0E_VAL_H	
301	CTLE_CFG_0F_VAL_L	
302	CTLE_CFG_0F_VAL_M	
303	CTLE_CFG_0F_VAL_H	
304	CTLE_CFG_10_VAL_L	
305	CTLE_CFG_10_VAL_M	
306	CTLE_CFG_10_VAL_H	
307	CTLE_CFG_11_VAL_L	
308	CTLE_CFG_11_VAL_M	
309	CTLE_CFG_11_VAL_H	
310	CTLE_CFG_12_VAL_L	
311	CTLE_CFG_12_VAL_M	
312	CTLE_CFG_12_VAL_H	
313	CTLE_CFG_13_VAL_L	
314	CTLE_CFG_13_VAL_M	
315	CTLE_CFG_13_VAL_H	
316	CTLE_CFG_14_VAL_L	
317	CTLE_CFG_14_VAL_M	
318	CTLE_CFG_14_VAL_H	
319	CTLE_CFG_15_VAL_L	
320	CTLE_CFG_15_VAL_M	
321	CTLE_CFG_15_VAL_H	
322	CTLE_CFG_16_VAL_L	
323	CTLE_CFG_16_VAL_M	
324	CTLE_CFG_16_VAL_H	
325	CTLE_CFG_17_VAL_L	
326	CTLE_CFG_17_VAL_M	
327	CTLE_CFG_17_VAL_H	
328	CTLE_CFG_18_VAL_L	
329	CTLE_CFG_18_VAL_M	
330	CTLE_CFG_18_VAL_H	
331	CTLE_CFG_19_VAL_L	

Table 162. 0x800 PHY_DIG_CMN Registers Summary

Register Number	Register Name	Section #
332	CTLE_CFG_19_VAL_M	
333	CTLE_CFG_19_VAL_H	
334	CTLE_CFG_1A_VAL_L	
335	CTLE_CFG_1A_VAL_M	
336	CTLE_CFG_1A_VAL_H	
337	CTLE_CFG_1B_VAL_L	
338	CTLE_CFG_1B_VAL_M	
339	CTLE_CFG_1B_VAL_H	
340	CTLE_CFG_1C_VAL_L	
341	CTLE_CFG_1C_VAL_M	
342	CTLE_CFG_1C_VAL_H	
343	CTLE_CFG_1D_VAL_L	
344	CTLE_CFG_1D_VAL_M	
345	CTLE_CFG_1D_VAL_H	
346	CTLE_CFG_1E_VAL_L	
347	CTLE_CFG_1E_VAL_M	
348	CTLE_CFG_1E_VAL_H	
349	CTLE_CFG_1F_VAL_L	
350	CTLE_CFG_1F_VAL_M	
351	CTLE_CFG_1F_VAL_H	

4.6.1.8.1 AUX_CTRL

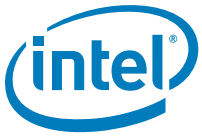
Offset	Bit(s)	Field Name	Description	Type	Default Value
0	7:2	reserved		RO	0
0	1:0	aux_power_state	Power state of the AUX PHY: 00 - Active 01 - Power Down 10/11 - reserved	RW	0

4.6.1.8.2 RX_MODE

Offset	Bit(s)	Field Name	Description	Type	Default Value
1	7	bypass_rx_mode	Bypass for the mode indication towards the PHY	RW	0
1	6:1	reserved		RO	0
1	0	rx_mode	DP or HDMI indication towards the PHY. Unless bypassed, it reflects the mode the SNK is operating in: 1 - DP 0 - HDMI	RW	0

4.6.1.8.3 DP_RATE

Offset	Bit(s)	Field Name	Description	Type	Default Value
2	7:2	reserved		RO	0



2	1:0	dp_rate	DP data rate settings: 00 - 1.62 Gbps 01 - 2.7 Gbps 10 - 5.4 Gbps 11 - reserved	RW	0

4.6.1.8.4 REFCLK_SEL

Offset	Bit(s)	Field Name	Description	Type	Default Value
3	7:4	reserved		RO	0
3	3:0	refclk_sel	Per lane reference clock select for the PHY: 0 - 25Mhz clock (crystal) for DP mode 1 - TMDS clock for HDMI mode	RW	0

4.6.1.8.5 RX_EN

Offset	Bit(s)	Field Name	Description	Type	Default Value
4	7	rx3_en_b	Per lane inverted lane enable indication. This is the enable indication as goes to physical lane 3. Active low.	RW	0
4	6	rx2_en_b	Per lane inverted lane enable indication. This is the enable indication as goes to physical lane 2. Active low.	RW	0
4	5	rx1_en_b	Per lane inverted lane enable indication. This is the enable indication as goes to physical lane 1. Active low.	RW	0
4	4	rx0_en_b	Per lane inverted lane enable indication. This is the enable indication as goes to physical lane 0. Active low.	RW	0
4	3:0	rx_en	Per lane lane enable indication towards the PHY. This is the enable indication arranged by logical lanes.	RW	0

4.6.1.8.6 CM_AMON_SEL

Offset	Bit(s)	Field Name	Description	Type	Default Value
5	7:0	cm_amon_sel	AMON selector for common block	RW	0

4.6.1.8.7 CM_CTRL

Offset	Bit(s)	Field Name	Description	Type	Default Value
6	7:4	reserved		RO	0
6	3	cm_cal_rdy_h	Rx Termination calibration ready indication	RW	0
6	2	cm_restune_bypass	Bypass Rx Termination calibration settings	RW	0
6	1	cm_cal_start	Start Rx Termination calibration	RW	0
6	0	cm_en	Per lane enable indication towards the PHY. This is the enable indication arranged by logical lanes	RW	0

4.6.1.8.8 CM_BG_BIASTUNE

Offset	Bit(s)	Field Name	Description	Type	Default Value
7	7:6	reserved		RO	0
7	5:0	cm_bg_biastune	Fine-tune local BandGap reference	RW	0

4.6.1.8.9 CM_RESTUNE_SET

Offset	Bit(s)	Field Name	Description	Type	Default Value
8	7:5	reserved		RO	0
8	4:0	cm_restune_set	RX termination resistor settings in bypass mode	RW	0

4.6.1.8.10 CM_RESTUNE_MON

Offset	Bit(s)	Field Name	Description	Type	Default Value
9	7:5	reserved		RO	0
9	4:0	cm_restune_mon	RX termination settings monitor	RW	0

4.6.1.8.11 RX_RST_N

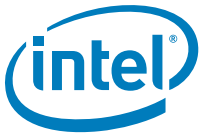
Offset	Bit(s)	Field Name	Description	Type	Default Value
10	7	rx3_rst_b	Per lane inverted lane reset indication. This is the reset indication as goes to physical lane 3. Active low.	RW	0
10	6	rx2_rst_b	Per lane inverted lane reset indication. This is the reset indication as goes to physical lane 2. Active low.	RW	0
10	5	rx1_rst_b	Per lane inverted lane reset indication. This is the reset indication as goes to physical lane 1. Active low.	RW	0
10	4	rx0_rst_b	Per lane inverted lane reset indication. This is the reset indication as goes to physical lane 0. Active low.	RW	0
10	3:0	rx_rst_n	Per lane lane reset indication towards the PHY. This is the reset indication arranged by logical lanes. Active low.	RW	0

4.6.1.8.12 SIPO_RST_N

Offset	Bit(s)	Field Name	Description	Type	Default Value
11	7	rx3_sipo_rst_b	Per lane inverted SIPO reset indication. This is the reset indication as goes to physical lane 3. Active low.	RW	0
11	6	rx2_sipo_rst_b	Per lane inverted SIPO reset indication. This is the reset indication as goes to physical lane 2. Active low.	RW	0
11	5	rx1_sipo_rst_b	Per lane inverted SIPO reset indication. This is the reset indication as goes to physical lane 1. Active low.	RW	0
11	4	rx0_sipo_rst_b	Per lane inverted SIPO reset indication. This is the reset indication as goes to physical lane 0. Active low.	RW	0
11	3:0	sipo_rst_n	Per lane SIPO reset indication towards the PHY. This is the reset indication arranged by logical lanes. Active low.	RW	0

4.6.1.8.13 FORCE_PLL_LOCK

Offset	Bit(s)	Field Name	Description	Type	Default Value
12	7:4	pll_lock_force_en	Per labe enable indication for pll_lock	RW	0
12	3:0	pll_lock_force_val	Per lane pll_lock value when pll_lock_force is enabled	RW	0



4.6.1.8.14 RX_PLL_LOCK

Offset	Bit(s)	Field Name	Description	Type	Default Value
13	7:4	rx_pll_lock_noswap	Per lane pll_lock value. This is arranged in physical order	RO	0
13	3:0	rx_pll_lock_swapped	Per lane pll_lock value. This is arranged in logical order	RO	0

4.6.1.8.15 RX_PLL_PRELOCK

Offset	Bit(s)	Field Name	Description	Type	Default Value
14	7:4	rx_pll_prelock_noswap	Per lane pll_prelock value. This is arranged in physical order	RO	0
14	3:0	rx_pll_prelock_swapped	Per lane pll_prelock value. This is arranged in logical order	RO	0

4.6.1.8.16 RTL_IN_CTRL_PI0_CTLE1

Offset	Bit(s)	Field Name	Description	Type	Default Value
15	7:4	reserved		RO	0
15	3:0	rtl_in_control_pi0_ctle1	Per lane switch the control over eyemon and PHY related signals between the CTLE and PI logic: 0 - PI logic 1 - CTLE selection logic	RW	0

4.6.1.8.17 ALLOW_RTL_EYEMON_CTRL

Offset	Bit(s)	Field Name	Description	Type	Default Value
16	7:4	allow_rtl_eyemon_clkph_ctrl	Per lane switch the control over pi clock phase between FW and RTL: 0 - FW 1 - RTL	RW	0xF
16	3:0	allow_rtl_eyemon_vref_ctrl	Per lane switch the control over eyemon_vref between FW and RTL: 0 - FW 1 - RTL	RW	0xF

4.6.1.8.18 ALLOW_RTL_CTLE_CTRL

Offset	Bit(s)	Field Name	Description	Type	Default Value
17	7:4	allow_rtl_pll_mode_byp	Per lane switch the control over pll mode between FW and RTL: 0 - FW 1 - RTL	RW	0
17	3:0	allow_rtl_ctle_ctrl	Per lane switch the control over CTLE parameters between FW and RTL: 0 - FW 1 - RTL	RW	0xF

4.6.1.8.19 ALLOW_RTL_ERRSLCR_OFST_CTL

Offset	Bit(s)	Field Name	Description	Type	Default Value
18	7:4	reserved		RO	0

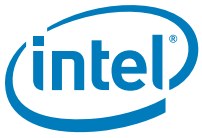
18	3:0	allow_rtl_errslicer_offset_ctrl	Per lane switch the control over error slicer offset between FW and RTL: 0 - FW 1 - RTL	RW	0

4.6.1.8.20 ALLOW_RTL_CML2CMOS_OFST_CTL

Offset	Bit(s)	Field Name	Description	Type	Default Value
19	7:4	allow_rtl_cml2cmos_stg2_offset_ctrl	Per lane switch the control over CML2CMOS stage 2 offset between FW and RTL: 0 - FW 1 - RTL	RW	0
19	3:0	allow_rtl_cml2cmos_stg1_offset_ctrl	Per lane switch the control over CML2CMOS stage 1 offset between FW and RTL: 0 - FW 1 - RTL	RW	0

4.6.1.8.21 ALLOW_RTL_810_CTL

Offset	Bit(s)	Field Name	Description	Type	Default Value
20	7:2	reserved		RO	0
20	1	allow_rtl_symb_lock_en810_ctrl	Switch the control over symbol lock enable between FW and RTL: 0 - FW 1 - RTL	RW	1
20	0	allow_rtl_symb_relock810_ctrl	Switch the control over symbol re-lock between FW and RTL: 0 - FW 1 - RTL	RW	1



4.6.1.8.22 RX_EYEMON_CTRL

Offset	Bit(s)	Field Name	Description	Type	Default Value
21	7	eyemon_wr_all_lanes	When set, writing to the following lane 0 registers writes the same value to all lanes: EYEMON_SCAN_CTRL0 EYEMON_SCAN_SEL0 EYEMON_GO0 EYEMON_SRCH_STRT_VAL_LCK0 EYEMON_ALIGN_FORCE0 EYEMON_ALIGN_FORCE_SEL0 EYEMON_MODE0 EYEMON_MASK_SEL0 EYEMON_MASK_SHIFT0 EYEMON_MASK_SHIFT0 EYEMON_SYMBOL_COUNT_0L EYEMON_SYMBOL_COUNT_0M EYEMON_SYMBOL_COUNT_0H EYEMON_SCAN_THR0_0L EYEMON_SCAN_THR0_0H EYEMON_SCAN_THR1_1L EYEMON_SCAN_THR1_0H EYEMON_SCAN_START_VAL_0L EYEMON_SCAN_START_VAL_0H EYEMON_SCAN_END_VAL_0L EYEMON_SCAN_END_VAL_0H EYEMON_SCAN_STEP_0	RW	0
21	6	reserved		RO	0
21	5:4	eyemon_input_delay	EMN block synchronization setting. By default all 4*DW optional bit alignments are scanned	RW	0
21	3:0	rx_eyemon_en	Enablethe PHY eyemon logic	RW	0

4.6.1.8.23 RX_SIPO_10BIT

Offset	Bit(s)	Field Name	Description	Type	Default Value
22	7:4	reserved		RO	0
22	3:0	rx_sipo_10bit	When set, the recovered serial data from the PHY is mapped to only the 10 odd bits of the parallel data bus (rx_data[19,17,15..3,1]). The even bits are not used. This mode is used in DP modes 1.62 and 2.7. The parallel data remains aligned to parclk in both modes	RW	0

4.6.1.8.24 COARSE_CAL_CTRL

Offset	Bit(s)	Field Name	Description	Type	Default Value
23	7:4	skip_coarse_cal	Disables the coarse calibration process when doing automatic (RTL driven) PI calibration	RW	0
23	3:0	start_coarse_cal_fw	Allows to starts the coarse PI calibration process manually	RW	0

4.6.1.8.25 PI_CAL_CTRL

Offset	Bit(s)	Field Name	Description	Type	Default Value
24	7	reserved	reserved	RO	0
24	6	look_for_10	When set, the coarse calibration will wait for a 0->1 transition on the Phase Detecor output	RW	0
24	5	look_for_01	When set, the coarse calibration will wait for a 0->1 transition on the Phase Detecor output	RW	1
24	4	phshift_default_dir	Default direction from which to start the PI calibration	RW	0
24	3:0	start_pi_cal	Start command for the automatic PI calibration process	RW	0

4.6.1.8.26 PI_CAL_DONE

Offset	Bit(s)	Field Name	Description	Type	Default Value
25	7:4	pi_cal_done	Per lane indication that the PI calibration process is over	RO	0
25	3:0	coarse_cal_done	Per lane indication that the coarse calibration of the PI is over	RO	0

4.6.1.8.27 PI_COARSE_CAL_SAFE_DIST

Offset	Bit(s)	Field Name	Description	Type	Default Value
26	7:0	pi_coarse_cal_safe_dist	The number of PI steps to roll after coarse PI calibration before starting the fine PI calibration to ensure the optimal point is detected	RW	0x14

4.6.1.8.28 DONT_WAIT_IN_PLL_MODE

Offset	Bit(s)	Field Name	Description	Type	Default Value
27	7:1	reserved	reserved	RO	0
27	0	dont_wait_in_pll_mode	Disables the delay used to ensure the PLL is locked during the CTLE selection process	RW	0

4.6.1.8.29 PD_STABLE_TIMER_L

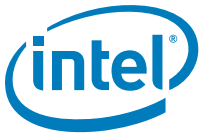
Offset	Bit(s)	Field Name	Description	Type	Default Value
28	7:0	pd_stable_timer[7:0]	Low 8bits of the timeout default used to ensure the Phase Detector output is stable	RW	0xA

4.6.1.8.30 PD_STABLE_TIMER_H

Offset	Bit(s)	Field Name	Description	Type	Default Value
29	7:0	pd_stable_timer[15:8]	High 8bits of the timeout default used to ensure the Phase Detector output is stable	RW	0

4.6.1.8.31 PD_SETUP_TIMER_L

Offset	Bit(s)	Field Name	Description	Type	Default Value
30	7:0	pd_stable_timer[7:0]	Low 8bits of the timeout default used to ensure the Phase Detector output is valid	RW	0xA



4.6.1.8.32 PD_SETUP_TIMER_H

Offset	Bit(s)	Field Name	Description	Type	Default Value
31	7:0	pd_stable_timer[15:8]	High 8bits of the timeout default used to ensure the Phase Detector output is valid	RW	0x0

4.6.1.8.33 PI_CAL_EYEMON_SCAN_THR0_L

Offset	Bit(s)	Field Name	Description	Type	Default Value
32	7:0	pi_cal_eyemon_scan_thr0[7:0]	Low 8bits of the low threshold value used when using the scan mode in the eyemon during PI calibration	RW	0xA

4.6.1.8.34 PI_CAL_EYEMON_SCAN_THR0_H

Offset	Bit(s)	Field Name	Description	Type	Default Value
33	7:0	pi_cal_eyemon_scan_thr0[15:8]	High 8bits of the low threshold value used when using the scan mode in the eyemon during PI calibration	RW	0x0

4.6.1.8.35 PI_CAL_EYEMON_SCAN_THR1_L

Offset	Bit(s)	Field Name	Description	Type	Default Value
34	7:0	pi_cal_eyemon_scan_thr1[7:0]	Low 8bits of the high threshold value used when using the scan mode in the eyemon during PI calibration	RW	0xA

4.6.1.8.36 PI_CAL_EYEMON_SCAN_THR1_H

Offset	Bit(s)	Field Name	Description	Type	Default Value
35	7:0	pi_cal_eyemon_scan_thr1[15:8]	High 8bits of the high threshold value used when using the scan mode in the eyemon during PI calibration	RW	0x0

4.6.1.8.37 FINE_SCAN_WIDTH

Offset	Bit(s)	Field Name	Description	Type	Default Value
36	7:0	fine_scan_width	The width of the scan done during the fine stage of the PI calibration process. denoted in PI steps	RW	0xA

4.6.1.8.38 RESET_PI_FSMS

Offset	Bit(s)	Field Name	Description	Type	Default Value
37	7:4	rest_pi_fsms[7:4]	Per lane reset indication to the PI coarse state FSM	RW	0x0
37	3:0	rest_pi_fsms[3:0]	Per lane reset indication to the PI main state FSM	RW	0x0

4.6.1.8.39 RX_DATA_SWIZZLE_EN

Offset	Bit(s)	Field Name	Description	Type	Default Value
39	7:4	rx_data_swizzle20_en	Per lane indication to swizzle the 20bit rx_data: {19,18,17...2,1,0} -> {0,1,2...17,18,19}	RW	0x0
39	3:0	rx_data_swizzle10_en	Per lane indication to swizzle the 20bit rx_data 10bit at a time: {19,18..,11,10,9,8...1,0} -> {10,11...18,19,0,1..9,10}	RW	0x0

4.6.1.8.40 EYEDATA_SWIZZLE_EN

Offset	Bit(s)	Field Name	Description	Type	Default Value
40	7:4	eyedata_swizzle20_en	Per lane indication to swizzle the 20bit eye_data: {19,18,17...2,1,0} -> {0,1,2...17,18,19}	RW	0x0
40	3:0	eyedata_swizzle10_en	Per lane indication to swizzle the 20bit eye_data 10bit at a time: {19,18..,11,10,9,8...1,0} -> {10,11...18,19,0,1..9,10}	RW	0x0

4.6.1.8.41 REARNG_EVENODD_RX_DATA

Offset	Bit(s)	Field Name	Description	Type	Default Value
42	7:6	rearrange_evenodd_rx_data[3]	When set, the incoming 20bit rx_data on lane 3 will be compressed to 10bits. 0 - no compression 1 - odd bits (19,17,15..5,3,1)are moved to bits [9:0] 2 - reserved 3 - even bits (18,16,14..4,2,0) are moved to bits [9:0]	RW	0x0
42	5:4	rearrange_evenodd_rx_data[2]	When set, the incoming 20bit rx_data on lane 2 will be compressed to 10bits. 0 - no compression 1 - odd bits (19,17,15..5,3,1)are moved to bits [9:0] 2 - reserved 3 - even bits (18,16,14..4,2,0) are moved to bits [9:0]	RW	0x0
42	3:2	rearrange_evenodd_rx_data[1]	When set, the incoming 20bit rx_data on lane 1 will be compressed to 10bits. 0 - no compression 1 - odd bits (19,17,15..5,3,1)are moved to bits [9:0] 2 - reserved 3 - even bits (18,16,14..4,2,0) are moved to bits [9:0]	RW	0x0
42	1:0	rearrange_evenodd_rx_data[0]	When set, the incoming 20bit rx_data on lane 0 will be compressed to 10bits. 0 - no compression 1 - odd bits (19,17,15..5,3,1)are moved to bits [9:0] 2 - reserved 3 - even bits (18,16,14..4,2,0) are moved to bits [9:0]	RW	0x0

4.6.1.8.42 REARNG_EVENODD_EYEDATA

Offset	Bit(s)	Field Name	Description	Type	Default Value
43	7:6	rearrange_evenodd_eyedata[3]	When set, the incoming 20bit eyedata on lane 3 will be compressed to 10bits. 0 - no compression 1 - odd bits (19,17,15..5,3,1)are moved to bits [9:0] 2 - reserved 3 - even bits (18,16,14..4,2,0) are moved to bits [9:0]	RW	0x0
43	5:4	rearrange_evenodd_eyedata[2]	When set, the incoming 20bit eyedata on lane 2 will be compressed to 10bits. 0 - no compression 1 - odd bits (19,17,15..5,3,1)are moved to bits [9:0] 2 - reserved 3 - even bits (18,16,14..4,2,0) are moved to bits [9:0]	RW	0x0
43	3:2	rearrange_evenodd_eyedata[1]	When set, the incoming 20bit eyedata on lane 1 will be compressed to 10bits. 0 - no compression 1 - odd bits (19,17,15..5,3,1)are moved to bits [9:0] 2 - reserved 3 - even bits (18,16,14..4,2,0) are moved to bits [9:0]	RW	0x0
43	1:0	rearrange_evenodd_eyedata[0]	When set, the incoming 20bit eyedata on lane 0 will be compressed to 10bits. 0 - no compression 1 - odd bits (19,17,15..5,3,1)are moved to bits [9:0] 2 - reserved 3 - even bits (18,16,14..4,2,0) are moved to bits [9:0]	RW	0x0

4.6.1.8.43 DATA_INV

Offset	Bit(s)	Field Name	Description	Type	Default Value
44	7:4	eyedata_inv	Per lane indication to invert the 20bit eye_data	RW	0x0
44	3:0	rx_data_inv	Per lane indication to invert the 20bit rx_data	RW	0x0

4.6.2 Transmitter

The display port Transmitter uses a 13 bit address space for its internal registers access.

This address space is divided into 5 separate banks defined in the following list. When accessed through Jtag "by 8051", that's the addresses that should be used (plus 3 MSbits (16 bits in total) that identify the accessed port - 0/1/2/3/4 for src0/snk0/snk1/src_pa/src_pb, respectively). When accessed by a target access (indirectly through DP Vendor capability space) the below addresses should be logically OR'ed with 0xC000, e.g. the base address of Bank 1 is 0xC200.

0x200 Bank 1 -- Framer -- Framer of Display Port, receive

0x400 Bank2 -- Reserved

0x600 Bank 3 -- Physical_Layer -- Phy of Display Port, receive

0x800 Bank4 - Misc2

0xA00 Bank 5 -- Auxiliary -- Auxiliary of Display Port, receive

0xC00 Bank 6 -- MISC -- hpd, misc registers, configuration

0xE00 Bank 7 -- Analog_if

0x1600 Bank 11 -- Phy Digital Lane

The following sections define the registers used at each bank.

The real address of a register is the register number + bank offset.

4.6.2.1 Bank 1 -- Framer -- Framer of Display Port, transmit

Table 163 is a summary of the Analog registers without registers description. The detailed description of the register list is given in the following sections. The registers marked with (*) exist in all of the Sources (0/A/B), while the others only in Source 0.

Table 163. 0x200 Framer Registers Summary

Register Number	Register Name	Section #
0	TX FRAMER CONFIG REG (*)	"Register 1h -- TX FRAMER STAT REG -- status register" on page 456
2	TX FRAMER BLANK STUFF REG (*)	"Register 2h -- TX FRAMER BLANK STUFF REG -- transmitted pattern during blanking period (should be configured while tx framer is disabled)" on
8	TX FRAMER BS TIMER LSB REG (*)	"Register 8h -- TX FRAMER BS TIMER LSB REG -- ls byte of bs set no-video timer (should be configured while tx framer is disabled)" on
9	TX FRAMER BS TIMER MSB REG (*)	"Register 9h -- TX FRAMER BS TIMER MSB REG -- ms byte of bs set no-video timer (should be configured while tx framer is disabled)" on
10	TX FRAMER SR TIMER LSB REG (*)	"Register Ah -- TX FRAMER SR TIMER LSB REG -- ls byte of sr no-video counter (should be configured while tx framer is disabled)" on

Table 163. 0x200 Framer Registers Summary

Register Number	Register Name	Section #
11	TX FRAMER SR TIMER MSB REG (*)	"Register Bh -- TX FRAMER SR TIMER MSB REG -- ms byte of sr no-video counter (should be configured while tx framer is disabled)" on
12	TX FRAMER NORMAL IDLE BS PATTERN (*)	"Register Bh -- TX FRAMER SR TIMER MSB REG -- ms byte of sr no-video counter (should be configured while tx framer is disabled)" on

4.6.2.1.1 Register 1h -- TX FRAMER STAT REG -- status register

Address Offset	Name	Description	Mode	Default
1.7:1	Reserved			
1.0	tx_framer_fifo_overflow	fifo overflow indication (severe error indication). should always equal '0' during operation. (if asserted, write '0' for de-assertion, however, value will only be affected if the problem does not persist)	RO	0

4.6.2.1.2 Register 2h -- TX FRAMER BLANK STUFF REG -- transmitted pattern during blanking period (should be configured while tx framer is disabled)

Address Offset	Name	Description	Mode	Default
2.7:0	tx_framer_blank_stuff_reg		RW	0h

4.6.2.1.3 Register 8h -- TX FRAMER BS TIMER LSB REG -- ls byte of bs set no-video timer (should be configured while tx framer is disabled)

Address Offset	Name	Description	Mode	Default
8.7:0	tx_framer_bs_timer_lsb_reg		RW	0h

4.6.2.1.4 Register 9h -- TX FRAMER BS TIMER MSB REG -- ms byte of bs set no-video timer (should be configured while tx framer is disabled)

Address Offset	Name	Description	Mode	Default
9.7:0	tx_framer_bs_timer_msb_reg		RW	20h

4.6.2.1.5 Register Ah -- TX FRAMER SR TIMER LSB REG -- ls byte of sr no-video counter (should be configured while tx framer is disabled)

Address Offset	Name	Description	Mode	Default
10.7:0	tx_framer_sr_timer_lsb_reg		RW	0h

4.6.2.1.6 Register Bh -- TX FRAMER SR TIMER MSB REG -- ms byte of sr no-video counter (should be configured while tx framer is disabled)

Address Offset	Name	Description	Mode	Default
11.7:4	Reserved			
11.3:0	tx_framer_sr_timer_msb_reg		RW	2h

4.6.2.1.7 Register Ch -- TX_FRAMER_NORMAL_IDLE_BS_PATTERN_REG_ADDR-Pattern sent right after BS (periodically) while Source still doesn't get any data from the Sink

Address Offset	Name	Description	Mode	Default
11.7:0	tx_framer_normal_idle_bs_pattern_reg[7:0]		RW	9h

4.6.2.2 Bank 3 -- Physical_Layer -- Phy of Display Port, transmit

Table 164 is a summary of the PHY registers without registers description. The detailed description of the register list is given in the following sections.

Table 164. 0x600 PHY Layer Register Summary

Register Number	Register Name	Section #
0	PHY_CONFIG_0	"Register 0h -- PHY_CONFIG_0" on page 457
1	PHY_CONFIG_1	"Register 1h -- PHY_CONFIG_1" on page 457
2	PHY_CONFIG_2	"Register 2h -- PHY_CONFIG_2" on page 457
3	PHY_CONFIG_3	"Register 3h -- PHY_CONFIG_3" on page 457

4.6.2.2.1 Register 0h -- PHY_CONFIG_0

Address offset	Name	Description	Mode	Default
0.7	Reserved			
0.6	encoder_bypass	encoder 8/10 bypass 1= bypass 0=normal	RW	0h
0.5	disp_polarity	select init diparity when disp_init is high 1= positive disp 0= negative disp	RW	0h
0.4	skew_bypass	1 = bypass skew block 0 = normal mode	RW	0h
0.3:1	Reserved			
0.0	scrambler_bypass	1 = scramble bypass 0 = normal mode	RW	0h

4.6.2.2.2 Register 1h -- PHY_CONFIG_1

Address offset	Name	Description	Mode	Default
1.7:0	Reserved			

4.6.2.2.3 Register 2h -- PHY_CONFIG_2

Address offset	Name	Description	Mode	Default
2.7:0	Reserved			

4.6.2.2.4 Register 3h -- PHY_CONFIG_3

Address offset	Name	Description	Mode	Default

3.7:0	Reserved			

4.6.2.3 Bank 4 - Miscellaneous-2

Table 165 provides a summary of the Misc2 registers without registers description. The detailed description of the register list is given in the following sections.

Table 165. 0x800 Misc2 Registers Summary

Register Number	Register Name	Section #
0	MODE	"Mode" on page 459
1	IDENTITY	"Identity" on page 460
2	STATUS	"Status" on page 460
4	HDP_CTRL_0	"HDP_CTRL_0" on page 460
5	HDP_CTRL_1	"HDP_CTRL_1" on page 460
6	HDP_CTRL_2	"HDP_CTRL_2" on page 460
7	HDP_CTRL_3	"HDP_CTRL_3" on page 461
8	GENREG0	"GENREG 0" on page 461
9	GENREG1	"GENREG 1" on page 461
10	GENREG2	"GENREG 2" on page 461
11	GENREG3	"GENREG 3" on page 461
15	CAR_CONTROL	"CAR CTRL" on page 461
16	TAR_CTRL_0	"TAR_CTRL_0" on page 462
17	TAR_CTRL_1	"TAR_CTRL_1" on page 462
18	TAR_CTRL_2	"TAR_CTRL_2" on page 462
19	TAR_CTRL_3	"TAR_CTRL_3" on page 462
20	TAR_WR_DATA_0	"TAR_WR_DATA 0" on page 462
21	TAR_WR_DATA_1	"TAR_WR_DATA 1" on page 462
22	TAR_WR_DATA_2	"TAR_WR_DATA 2" on page 463
23	TAR_WR_DATA_3	"TAR_WR_DATA 3" on page 463
24	TAR_RD_DATA_0	"TAR_RD_DATA 0" on page 463
25	TAR_RD_DATA_1	"TAR_ RD _DATA 1" on page 463
26	TAR_RD_DATA_2	"TAR_ RD _DATA 2" on page 463
27	TAR_RD_DATA_3	"TAR_ RD _DATA 3" on page 463
32	EE_CTRL	"EE_CTRL" on page 463
33	EE_ADDR_0	"EE_ADDR 0" on page 463
34	EE_ADDR_1	"EE_ADDR 1" on page 463
35	EE_RD_DATA_0	"EE_RD_DATA 0" on page 463
36	EE_RD_DATA_1	"EE_ RD _DATA 1" on page 464
37	EE_RD_DATA_2	"EE_ RD _DATA 2" on page 464
38	EE_RD_DATA_3	"EE_ RD _DATA 3" on page 464
44	EE2TAR_LOAD_DONE	"EE2TAR_LOAD_DONE" on page 464
45	SWAP_BYP_CTRL	"SWAP_BYP_CTRL" on page 464
46	HDP_SWAP_BYPASS	"HDP_SWAP_BYPASS" on page 464
47	PHY_PORT_STATUS	"PHY_PORT_STATUS" on page 464

Table 165. 0x800 Misc2 Registers Summary

Register Number	Register Name	Section #
48	SELF_BASE_ADDR_LO	"SELF_BASE_ADDR_LO" on page 465
49	SELF_BASE_ADDR_HI	"SELF_BASE_ADDR_HI" on page 465
52	PRTN_BASE_ADDR_LO	"PRTN_BASE_ADDR_LO" on page 465
53	PRTN_BASE_ADDR_HI	"PRTN_BASE_ADDR_HI" on page 465
54	PRTN_PORT_ID	"PRTN_PORT_ID" on page 465
56	ANA_ADDR_IDX_LO	"ANA_ADDR_IDX_LO" on page 465
57	ANA_ADDR_IDX_HI	"ANA_ADDR_IDX_HI" on page 465
58	ANA_DATA_IDX_LO	"ANA_DATA_IDX_LO" on page 465
59	ANA_DATA_IDX_HI	"ANA_DATA_IDX_HI" on page 466
60	PRTN_ANA_ADDR_IDX_LO	"PRTN_ANA_ADDR_IDX_LO" on page 466
61	PRTN_ANA_ADDR_IDX_HI	"PRTN_ANA_ADDR_IDX_HI" on page 466
62	PRTN_ANA_DATA_IDX_LO	"PRTN_ANA_DATA_IDX_LO" on page 466
63	PRTN_ANA_DATA_IDX_HI	"PRTN_ANA_DATA_IDX_HI" on page 466
72	EE_GP_CFG0	"EE_GP_CFG0" on page 466
73	EE_GP_CFG1	"EE_GP_CFG1" on page 466
74	EE_GP_CFG2	"EE_GP_CFG2" on page 467
75	EE_GP_CFG3	"EE_GP_CFG3" on page 467
76	EE_REGION_ADDR0	"EE_REGION_ADDR0" on page 467
77	EE_REGION_ADDR1	"EE_REGION_ADDR1" on page 467
78	EE_REGION_SIZE	"EE_REGION_SIZE" on page 467
80	DFT	"DFT" on page 467
81	DFT2	"DFT2" on page 467
112	TST_PTTRN_CTRL_0	"TST_PTTRN_CTRL_0" on page 467
113	TST_PTTRN_CTRL_1	"TST_PTTRN_CTRL_1" on page 467
114	TST_PTTRN_CTRL_2	"TST_PTTRN_CTRL_2" on page 468
115	TST_PTTRN_K	"TST_PTTRN_K" on page 468
116	TST_PTTRN_BS_0	"TST_PTTRN_BS_0" on page 468
117	TST_PTTRN_BS_1	"TST_PTTRN_BS_1" on page 468
118	TST_PTTRN_BS_2	"TST_PTTRN_BS_2" on page 468
119	TST_PTTRN_BS_3	"TST_PTTRN_BS_3" on page 468
120	TST_PTTRN_SR_0	"TST_PTTRN_SR_0" on page 468
121	TST_PTTRN_SR_1	"TST_PTTRN_SR_1" on page 468
122	TST_PTTRN_SR_2	"TST_PTTRN_SR_2" on page 469
123	TST_PTTRN_SR_3	"TST_PTTRN_SR_3" on page 469
124	TST_PTTRN_BS_RATIO_0	"TST_PTTRN_BS_RATIO_0" on page 469
125	TST_PTTRN_BS_RATIO_1	"TST_PTTRN_BS_RATIO_1" on page 469
126	TST_PTTRN_SR_RATIO_0	"TST_PTTRN_SR_RATIO_0" on page 469
127	TST_PTTRN_SR_RATIO_1	"TST_PTTRN_SR_RATIO_1" on page 469

4.6.2.3.1 Mode

Offset	Bit(s)	Field Name	Description	Type	Default Value
0	7	Redriv_en	Current redriver/tunneling mode: 0 – Tunneling (Source 0) 1 – Redriver (Source A/B)	RO	0

0	6:1	reserved	Reserved	RO	0
0	0	HDMI1_DP0	Current HDP mode: 0 – DP 1 – HDMI (not relevant for Source 0)**HDP In/Out bypass mode** HDP IN -> OUT HDMI bypass enable	RO	0

4.6.2.3.2 Identity

Offset	Bit(s)	Field Name	Description	Type	Default Value
1	7	Redriv_en	Current mode: 0 – Tunneling (Source 0) 1 – Redriver (Source A/B)	RO	0
1	6:1	Redriv_partner	Current partner. (valid only in redriver mode): 0 – Sink 0 1 – Sink 1	RO	0
1	0	Port_ID	CIO Port ID of this Sink.	RO	0

4.6.2.3.3 Status

Offset	Bit(s)	Field Name	Description	Type	Default Value
2	7	tx_pllcal_done	Tx PLL locked	RO	0
2	6:2	reserved	reserved	RO	0
2	1	data_in_valid	Sink is sending data. (Bit that passes through crux sync FIFO)	RO	0
2	0	dp_phy_data_valid	Sink is sending data. (Direct bit from the Sink FW)	RO	0

4.6.2.3.4 HDP_CTRL_0

Offset	Bit(s)	Field Name	Description	Type	Default Value
4	7:3	reserved	reserved	RO	0
4	2:0	DP_state	0 – Pre link training 1 – TPS1 2 – TPS2 4 – Post link training 7 - PRBS	RO	0

4.6.2.3.5 HDP_CTRL_1

Offset	Bit(s)	Field Name	Description	Type	Default Value
5	7:2	reserved	reserved	RO	0
5	1	aux_extra_info_dis	Enable extra info sent between dp_in and dp_out along with AUX packet. (used to correspond responses to requests and to transfer GTC indication)	RW	1
5	0	Link_init	Initiate link drop on Sink side. (similar to adapter error detection in DP_Out)	RO	0

4.6.2.3.6 HDP_CTRL_2

Offset	Bit(s)	Field Name	Description	Type	Default Value
6	7:2	reserved	reserved	RO	0

6	1	LL_bypass	Bypass Link Layer. Rx Phy data (10b per lane) received in Sink is bypassing Link Layer logic and driven to Tx Phy. (it is only synchronized to the common rx_clk in the Sink and then to tx_clk in the Source)	R/W	0
6	0	Leg_Phy_en	Legacy logic is used when this bit is set.	R/W	1

4.6.2.3.7 HDP_CTRL_3

Offset	Bit(s)	Field Name	Description	Type	Default Value
6	7:3	reserved	reserved	RO	0
6	2	gtc_freq_off_restart	GTC Freq offset calculation restart		
6	1	gtc_init_n	Digital reset of GTC Calc unit		
6	0	cable_plug	Indication for the Phy that HPD was recognized.	R/W	0

4.6.2.3.8 GENREG 0

Offset	Bit(s)	Field Name	Description	Type	Default Value
8	7:0	gp_reg0	General purpose register	R/W	0

4.6.2.3.9 GENREG 1

Offset	Bit(s)	Field Name	Description	Type	Default Value
9	7:0	gp_reg1	General purpose register	R/W	0

4.6.2.3.10 GENREG 2

Offset	Bit(s)	Field Name	Description	Type	Default Value
10	7:0	gp_reg2	General purpose register	R/W	0

4.6.2.3.11 GENREG 3

Offset	Bit(s)	Field Name	Description	Type	Default Value
11	7:0	gp_reg3	General purpose register	R/W	0

4.6.2.3.12 CAR CTRL

Offset	Bit(s)	Field Name	Description	Type	Default Value
15	7	frc_uctl_rst	When set to '1', holds 8051 in reset (otherwise it is according to src_tx_clk_stable indication)	R/W	0
15	6	reserved		RO	0
15	5	frc_hdp_out_ll_clk_en	When set to '1' it ungates HDP clock in the crux.	R/W	0
15	4	frc_hd_out_ll_clk_en	When set to '1' it ungates HDMI clock in the Source**HDP In/Out bypass mode** HDP IN -> OUT HDMI bypass enable	R/W	0
15	3	frc_adpt_out_en	When set to '1' it ungates DP clock in DP_Out adapter	R/W	0
15	2	frc_cmn_dp_out_en	When set to '1' it ungates DP clock in the Source	R/W	0

15	1	frc_src_tx_clk_gate_ctl	When set to '1' it controls the gating of tx_clk. (otherwise it is according to src_tx_clk_stable indication)	R/W	0
15	0	frc_src_tx_clk_gate_val	When frc_src_tx_clk_gate_ctl is '1' tx_clk is gated or not according to this value.	R/W	0

4.6.2.3.13 TAR_CTRL_0

Offset	Bit(s)	Field Name	Description	Type	Default Value
16	7:0	hdp_tar_dw_index[7:0]	The lower byte of tar_dw_index used when the Sink is mastering the target access.	R/W	0

4.6.2.3.14 TAR_CTRL_1

Offset	Bit(s)	Field Name	Description	Type	Default Value
17	7:5	reserved	reserved	RO	0
17	4:0	hdp_tar_dw_index[12:8]	The upper 5 bits of tar_dw_index used when the Sink is mastering the target access.	R/W	0

4.6.2.3.15 TAR_CTRL_2

Offset	Bit(s)	Field Name	Description	Type	Default Value
18	7:6	hdp_tar_cs[1:0]	tar_cs[1:0] used when the Sink is mastering the target access.	R/W	0
18	5:0	hdp_tar_port[5:0]	tar_port[5:0] used when the Sink is mastering the target access.	R/W	0

4.6.2.3.16 TAR_CTRL_3

Offset	Bit(s)	Field Name	Description	Type	Default Value
19	7	hdp_tar_valid	Setting to '1' activates HDP master target access. Self cleared when the access completes.	R/W	0
19	6:3	reserved	reserved	RO	0
19	2	hdp_pcie_sw_regs_access	pcie_sw_regs_access used when the Sink is mastering the target access.		
19	1	hdp_cio_sw_regs_access	cio_sw_regs_access used when the Sink is mastering the target access.		
19	0	hdp_tar_wr1_rd0	tar_wr1_rd0 used when the Sink is mastering the target access.	R/W	0

4.6.2.3.17 TAR_WR_DATA 0

Offset	Bit(s)	Field Name	Description	Type	Default Value
20	7:0	hdp_tar_wr_data[7:0]	tar_wr_data[7:0] used when the Sink is mastering the target access.	R/W	0

4.6.2.3.18 TAR_WR_DATA 1

Offset	Bit(s)	Field Name	Description	Type	Default Value
21	7:0	hdp_tar_wr_data[15:8]	tar_wr_data[15:8] used when the Sink is mastering the target access.	R/W	0

4.6.2.3.19 TAR_WR_DATA 2

Offset	Bit(s)	Field Name	Description	Type	Default Value
22	7:0	hdp_tar_wr_data[23:16]	tar_wr_data[23:16] used when the Sink is mastering the target access.	R/W	0

4.6.2.3.20 TAR_WR_DATA 3

Offset	Bit(s)	Field Name	Description	Type	Default Value
23	7:0	hdp_tar_wr_data[31:24]	tar_wr_data[31:24] used when the Sink is mastering the target access.	R/W	0

4.6.2.3.21 TAR_RD_DATA 0

Offset	Bit(s)	Field Name	Description	Type	Default Value
24	7:0	tar_hdp_rd_data_latched[7:0]	Latches tar_ rd_data[7:0] when read access by HDP is accomplished.	RO	0

4.6.2.3.22 TAR_ RD _DATA 1

Offset	Bit(s)	Field Name	Description	Type	Default Value
25	7:0	tar_hdp_rd_data_latched [15:8]	Latches tar_ rd_data[15:8] when read access by HDP is accomplished.	RO	0

4.6.2.3.23 TAR_ RD _DATA 2

Offset	Bit(s)	Field Name	Description	Type	Default Value
26	7:0	tar_hdp_rd_data_latched [23:16]	Latches tar_ rd_data[23:16] when read access by HDP is accomplished.	RO	0

4.6.2.3.24 TAR_ RD _DATA 3

Offset	Bit(s)	Field Name	Description	Type	Default Value
27	7:0	tar_hdp_rd_data_latched [31:24]	Latches tar_ rd_data[31:24] when read access by HDP is accomplished.	RO	0

4.6.2.3.25 EE_CTRL

Offset	Bit(s)	Field Name	Description	Type	Default Value
32	7	hdp_ee_rd	When set, HDP FLASH access is initiated.	R/W	0
32	6:0	reserved	reserved	RO	0

4.6.2.3.26 EE_ADDR 0

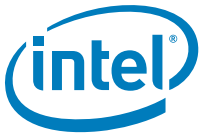
Offset	Bit(s)	Field Name	Description	Type	Default Value
33	7:0	hdp_ee_rd_addr[7:0]	HDP FLASH address low.	R/W	0

4.6.2.3.27 EE_ADDR 1

Offset	Bit(s)	Field Name	Description	Type	Default Value
34	7:0	hdp_ee_rd_addr[15:8]	HDP FLASH address high.	R/W	0

4.6.2.3.28 EE_RD_DATA 0

Offset	Bit(s)	Field Name	Description	Type	Default Value
35	7:0	ee_hdp_data_latched[7:0]	Latches ee_data[7:0] when read access by HDP is accomplished.	RO	0



4.6.2.3.29 EE_ RD _DATA 1

Offset	Bit(s)	Field Name	Description	Type	Default Value
36	7:0	ee_hdp_data_latched[15:0]	Latches ee_data[15:8] when read access by HDP is accomplished.	RO	0

4.6.2.3.30 EE_ RD _DATA 2

Offset	Bit(s)	Field Name	Description	Type	Default Value
37	7:0	ee_hdp_data_latched[23:16]	Latches ee_data[23:16] when read access by HDP is accomplished.	RO	0

4.6.2.3.31 EE_ RD _DATA 3

Offset	Bit(s)	Field Name	Description	Type	Default Value
38	7:0	ee_hdp_data_latched[31:24]	Latches ee_data[31:24] when read access by HDP is accomplished.	RO	0

4.6.2.3.32 EE2TAR_LOAD_DONE

Offset	Bit(s)	Field Name	Description	Type	Default Value
44	7:1	reserved		RO	0
44	0	ee_to_tar_dp_domain_done	Indicates that the ee2tar section of the dp domain has been completed	RO	0

4.6.2.3.33 SWAP_BYP_CTRL

Offset	Bit(s)	Field Name	Description	Type	Default Value
45	7:3	reserved		RO	0
45	2	swap_lanes_byp	The value to force to when bypassing the inverted cable detection mechanism	RW	0
45	1	bypass_swap_lanes	Bypass indication for the mechanism detecting a cable inserted upside down	RW	0
45	0	bypass_swap	When asserted, the final swap decision for the whole HDP block is taken based on HDP_SWAP_BYPASS register	RW	0

4.6.2.3.34 HDP_SWAP_BYPASS

Offset	Bit(s)	Field Name	Description	Type	Default Value
46	7:0	hdp_swap_byp	The swap to use when bypass_swap bit is asserted in SWAP_BYP_CTRL	RW	0

4.6.2.3.35 PHY_PORT_STATUS

Offset	Bit(s)	Field Name	Description	Type	Default Value
47	7:0	reserved			0
47	4	dptx3_is_active	Active indication from SRC_PA/_PB PHY control logic	RO	0
47	3	dptx2_is_active	Active indication from SRC_PA/_PB PHY control logic	RO	0
47	2	dptx1_is_active	Active indication from SRC_PA/_PB PHY control logic	RO	0
47	1	dptx0_is_active	Active indication from SRC_PA/_PB PHY control logic	RO	0
47	0	phy_dp_port_init_done	Initialization done indication from SRC_PA/_PB PHY control logic	RO	0

4.6.2.3.36 SELF_BASE_ADDR_LO

Offset	Bit(s)	Field Name	Description	Type	Default Value
48	7:0	self_base_addr[7:0]	The offset to its own vendor register space in the Port configuration space.	RO	0

4.6.2.3.37 SELF_BASE_ADDR_HI

Offset	Bit(s)	Field Name	Description	Type	Default Value
49	7:4	reserved	reserved	RO	0
49	3:0	self_base_addr[12:8]	The offset to its own vendor register space in the Port configuration space.	RO	0

4.6.2.3.38 PRTN_BASE_ADDR_LO

Offset	Bit(s)	Field Name	Description	Type	Default Value
52	7:0	partner_base_addr[7:0]	The offset to the partner's vendor register space in the Port configuration space.	RO	0

4.6.2.3.39 PRTN_BASE_ADDR_HI

Offset	Bit(s)	Field Name	Description	Type	Default Value
53	7:4	reserved	reserved	RO	0
53	3:0	partner_base_addr[12:8]	The offset to the partner's vendor register space in the Port configuration space.	RO	0

4.6.2.3.40 PRTN_PORT_ID

Offset	Bit(s)	Field Name	Description	Type	Default Value
54	7:6	reserved	reserved	RO	0
54	5:0	partner_port_id	The partner's Port ID.	RO	0

4.6.2.3.41 ANA_ADDR_IDX_LO

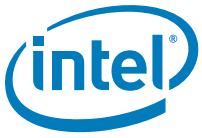
Offset	Bit(s)	Field Name	Description	Type	Default Value
56	7:0	ana_addr_index[7:0]	The address of the register that contains the offset in the analog register space. (for indirect access into the analog register space)	RO	0

4.6.2.3.42 ANA_ADDR_IDX_HI

Offset	Bit(s)	Field Name	Description	Type	Default Value
57	7:4	reserved	reserved	RO	0
57	3:0	ana_addr_index[12:8]	The address of the register that contains the offset in the analog register space. (for indirect access into the analog register space)	RO	0

4.6.2.3.43 ANA_DATA_IDX_LO

Offset	Bit(s)	Field Name	Description	Type	Default Value
58	7:0	ana_data_index[7:0]	The address of the register that contains the data of the analog register space. (for indirect access into the analog register space)	RO	0



4.6.2.3.44 ANA_DATA_IDX_HI

Offset	Bit(s)	Field Name	Description	Type	Default Value
59	7:4	reserved	reserved	RO	0
59	3:0	ana_data_index[12:8]	The address of the register that contains the data of the analog register space. (for indirect access into the analog register space)	RO	0

4.6.2.3.45 PRTN_ANA_ADDR_IDX_LO

Offset	Bit(s)	Field Name	Description	Type	Default Value
60	7:0	partner_ana_addr_index[7:0]	The address of the register that contains the offset in the partner's analog register space. (for indirect access into the partner's analog register space)	RO	0

4.6.2.3.46 PRTN_ANA_ADDR_IDX_HI

Offset	Bit(s)	Field Name	Description	Type	Default Value
61	7:4	reserved	reserved	RO	0
61	3:0	partner_ana_addr_index[12:8]	The address of the register that contains the offset in the partner's analog register space. (for indirect access into the partner's analog register space)	RO	0

4.6.2.3.47 PRTN_ANA_DATA_IDX_LO

Offset	Bit(s)	Field Name	Description	Type	Default Value
62	7:0	partner_ana_data_index[7:0]	The address of the register that contains the data of the partner's analog register space. (for indirect access into the partner's analog register space)	RO	0

4.6.2.3.48 PRTN_ANA_DATA_IDX_HI

Offset	Bit(s)	Field Name	Description	Type	Default Value
63	7:4	reserved	reserved	RO	0
63	3:0	partner_ana_data_index[12:8]	The address of the register that contains the data of the partner's analog register space. (for indirect access into the partner's analog register space)	RO	0

4.6.2.3.49 EE_GP_CFG0

Offset	Bit(s)	Field Name	Description	Type	Default Value
72	7:0	EE_GP_CFG0	ee_hdp_in_gp_cfg0	RO	from flash address 0x8e

4.6.2.3.50 EE_GP_CFG1

Offset	Bit(s)	Field Name	Description	Type	Default Value
73	7:0	EE_GP_CFG1	ee_hdp_in_gp_cfg1	RO	0

4.6.2.3.51 EE_GP_CFG2

Offset	Bit(s)	Field Name	Description	Type	Default Value
74	7:0	EE_GP_CFG2	ee_hdp_in_gp_cfg2	RO	0

4.6.2.3.52 EE_GP_CFG3

Offset	Bit(s)	Field Name	Description	Type	Default Value
75	0		forces DP_OUT FW to an eternal loop before waiting for HPD. Can be released by writing register 0xCC93 to value > 2 ([2:1] cause eternal loop in other places)		
75	7:1	EE_GP_CFG3	ee_hdp_out_gp_cfg3	RO	0

4.6.2.3.53 EE_REGION_ADDR0

Offset	Bit(s)	Field Name	Description	Type	Default Value
76	7:0	EE_REGION_ADDR0	ee_hdp_in_region_addr0	RO	0

4.6.2.3.54 EE_REGION_ADDR1

Offset	Bit(s)	Field Name	Description	Type	Default Value
77	7:0	EE_REGION_ADDR1	ee_hdp_in_region_addr1	RO	0

4.6.2.3.55 EE_REGION_SIZE

Offset	Bit(s)	Field Name	Description	Type	Default Value
78	7:0	EE_REGION_SIZE	ee_hdp_in_region_size	RO	0

4.6.2.3.56 DFT

Offset	Bit(s)	Field Name	Description	Type	Default Value
80	7:2	reserved	reserved	RO	0
80	2	fast_count	Speed up various timers. (for simulation only)	R/W	0
80	1	quick_link	Speed up link establishment. (for simulation only)	R/W	0

4.6.2.3.57 DFT2

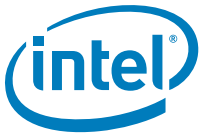
Offset	Bit(s)	Field Name	Description	Type	Default Value
81	7:0	printf	FW uses this register to printf its current location.	RO	0

4.6.2.3.58 TST_PTTRN_CTRL_0

Offset	Bit(s)	Field Name	Description	Type	Default Value
112	7:4	PRBS_EN	Enable (per lane) sending PRBS7	R/W	0
112	3:0	IDLE_PATTERN_EN	Enable (per lane) sending Idle pattern	R/W	0

4.6.2.3.59 TST_PTTRN_CTRL_1

Offset	Bit(s)	Field Name	Description	Type	Default Value
113	7:4	reserved		RO	0
113	3:0	TST_80bit_PTTRN_EN	Enable (per lane) sending 80bit pattern	R/W	0



4.6.2.3.60 TST_PTTRN_CTRL_2

Offset	Bit(s)	Field Name	Description	Type	Default Value
114	7:3	reserved		RO	0
114	2	IDLE_PTTRN_START_ANY_DISP	If set, Idle pattern starts being sent on any disparity, otherwise the first symbol of this pattern is sent on negative disparity	R/W	0
114	1	IDLE_PTTRN_DISP_RST_EN	If set, disparity will be reset in the beginning of Idle pattern sending	R/W	0
114	0	IDLE_PTTRN_ENHANCED	SR/BS sequence length: 0 – 1 byte 1 – 4 bytes	R/W	1

4.6.2.3.61 TST_PTTRN_K

Offset	Bit(s)	Field Name	Description	Type	Default Value
115	7:4	IDLE_PTTRN_SR_K	Per TST_PTTRN_SR_x: (0 ≤x ≤3) 0 – data symbol 1 – k-symbol	R/W	0xF
115	3:0	IDLE_PTTRN_BS_K	Per TST_PTTRN_BS_x: (0 ≤x ≤3) 0 – data symbol 1 – k-symbol	R/W	0xF

4.6.2.3.62 TST_PTTRN_BS_0

Offset	Bit(s)	Field Name	Description	Type	Default Value
116	7:0	IDLE_PTTRN_BS_0	8b representation of the 1st BS symbol	R/W	0xBC

4.6.2.3.63 TST_PTTRN_BS_1

Offset	Bit(s)	Field Name	Description	Type	Default Value
117	7:0	IDLE_PTTRN_BS_1	8b representation of the 2nd BS symbol	R/W	0x7C

4.6.2.3.64 TST_PTTRN_BS_2

Offset	Bit(s)	Field Name	Description	Type	Default Value
118	7:0	IDLE_PTTRN_BS_2	8b representation of the 3rd BS symbol	R/W	0x7C

4.6.2.3.65 TST_PTTRN_BS_3

Offset	Bit(s)	Field Name	Description	Type	Default Value
119	7:0	IDLE_PTTRN_BS_3	8b representation of the 4th BS symbol	R/W	0xBC

4.6.2.3.66 TST_PTTRN_SR_0

Offset	Bit(s)	Field Name	Description	Type	Default Value
120	7:0	IDLE_PTTRN_BS_0	8b representation of the 1st SR symbol	R/W	0x1C

4.6.2.3.67 TST_PTTRN_SR_1

Offset	Bit(s)	Field Name	Description	Type	Default Value
121	7:0	IDLE_PTTRN_BS_1	8b representation of the 2nd SR symbol	R/W	0x7C

4.6.2.3.68 TST_PTTRN_SR_2

Offset	Bit(s)	Field Name	Description	Type	Default Value
122	7:0	IDLE_PTTRN_BS_2	8b representation of the 3rd SR symbol	R/W	0x7C

4.6.2.3.69 TST_PTTRN_SR_3

Offset	Bit(s)	Field Name	Description	Type	Default Value
123	7:0	IDLE_PTTRN_BS_3	8b representation of the 4th SR symbol	R/W	0x1C

4.6.2.3.70 TST_PTTRN_BS_RATIO_0

Offset	Bit(s)	Field Name	Description	Type	Default Value
124	7:0	IDLE_PTTRN_BS_RATIO_LO	Number of cycles between the first symbol of one BS sequence and the first symbol of the next BS sequence. (Low byte)	R/W	0x0

4.6.2.3.71 TST_PTTRN_BS_RATIO_1

Offset	Bit(s)	Field Name	Description	Type	Default Value
125	7:0	IDLE_PTTRN_BS_RATIO_HI	Number of cycles between the first symbol of one BS sequence and the first symbol of the next BS sequence. (High byte)	R/W	0x20

4.6.2.3.72 TST_PTTRN_SR_RATIO_0

Offset	Bit(s)	Field Name	Description	Type	Default Value
126	7:0	IDLE_PTTRN_SR_RATIO_LO	Once in a while BS sequence is substituted by SR sequence. This field defines the number of BS sequences between any two SR sequences. (Low byte)	R/W	0xFF

4.6.2.3.73 TST_PTTRN_SR_RATIO_1

Offset	Bit(s)	Field Name	Description	Type	Default Value
127	7:0	IDLE_PTTRN_SR_RATIO_HI	Once in a while BS sequence is substituted by SR sequence. This field defines the number of BS sequences between any two SR sequences. (High byte)	R/W	0x1

4.6.2.4 Bank 5 -- Auxiliary -- Auxiliary of Display Port, Transmit

Table 166 is a summary of the AUX registers without registers description. The detailed description of the register list is given in the following sections.

Table 166. 0xA00 AUX Channel Register Summary

Register Number	Register Name	Section #
0	HOST_CONTROL	"Register 0h -- HOST_CONTROL -- control bits" on page 476

Table 166. 0xA00 AUX Channel Register Summary

Register Number	Register Name	Section #
1	SWAP_CONTROL	"Register 1h -- SWAP_CONTROL -- control the bit ordering of transmit & receive" on page 476
8	SEND_INTERNAL_TRANSACTION	"Register 8h -- SEND_INTERNAL_TRANSACTION -- send internal transaction by AUX_TX" on page 476
9	SEND_EXTERNAL_TRANSACTION	"Register 9h -- SEND_EXTERNAL_TRANSACTION -- send external transaction by AUX_TX" on page 476
10	SEND_NACK_TRANSACTION	"Register Ah -- SEND_NACK_TRANSACTION -- send nack transaction by AUX_TX" on page 476
11	SEND_TO_ADAPTER	"Register Bh -- SEND_TO_ADAPTER -- forward the receive transaction to the adapter" on page 476
12	CLEAR_RX	"Register Ch -- CLEAR_RX -- Clear all rx bits" on page 477
13	CLEAR_EXTERNAL	"Register Dh -- CLEAR_EXTERNAL -- Clear all external bits" on page 477
14	CLEAR_TIMER	"Register Eh -- CLEAR_TIMER -- Clear timer expire bits" on page 477
15	RESET_DP_AUX_SW	"Register Fh -- RESET_DP_AUX_SW -- S/W reset of the DP_AUX" on page 477
16	DIVIDE_2M	"Register 10h -- DIVIDE_2M -- the ratio between sys_clk and 2MHz" on page 477
17	TX_PREACHARGE _LENGTH	"Register 11h -- TX_PREACHARGE _LENGTH -- length of precharge field" on page 477
20	FREQUENCY_1M_MAX	"Register 14h -- FREQUENCY_1M_MAX -- maximum legal frequency receiving from the line" on page 477
21	FREQUENCY_1M_MIN	"Register 15h -- FREQUENCY_1M_MIN -- minimum legal frequency receiving from the line" on page 477
22	RX_PRE _MIN	"Register 16h -- RX_PRE _MIN -- minimum length of preamble during receive" on page 478
23	RX_PRE_MAX	"Register 17h -- RX_PRE_MAX -- maximum length of preamble during receive" on page 478
24	TIMER_PRESET_DP_IN_HIGH	"Register 18h -- TIMER_PRESET_DP_IN_HIGH -- The preset value (HIGH part) of the timer in DP_IN mode" on page 478
25	TIMER_PRESET_DP_IN_LOW	"Register 19h -- TIMER_PRESET_DP_IN_LOW -- The preset value (LOW part) of the timer in DP_IN mode" on page 478
26	TIMER_PRESET_DP_OUT_HIGH	"Register 1Ah -- TIMER_PRESET_DP_OUT_HIGH -- The preset value (HIGH part) of the timer in DP_OUT mode" on page 478
27	TIMER_PRESET_DP_OUT_LOW	"Register 1Bh -- TIMER_PRESET_DP_OUT_LOW -- The preset value LOW part) of the timer in DP_OUT mode" on page 478
28	NACK_FORMAT	"Register 1Ch -- NACK_FORMAT -- "nack" or "defer" pattern for transmit" on page 479
32	INTERNAL_TRANSACTION_LENGTH	"Register 20h -- INTERNAL_TRANSACTION_LENGTH -- length of the internal transaction" on page 479
33	INTERNAL_DATA_00A	"Register 21h -- INTERNAL_DATA_00A -- Internal Transaction bits(7:4) of byte 0" on page 479

Table 166. 0xA00 AUX Channel Register Summary

Register Number	Register Name	Section #
34	INTERNAL_DATA_00B	"Register 22h -- INTERNAL_DATA_00B -- Internal Transaction bits(3:0) of byte 0" on page 479
35	INTERNAL_DATA_01	"Register 23h -- INTERNAL_DATA_01 -- Internal Transaction byte 01" on page 479
36	INTERNAL_DATA_02	"Register 24h -- INTERNAL_DATA_02 -- Internal Transaction byte 02" on page 479
37	INTERNAL_DATA_03	"Register 25h -- INTERNAL_DATA_03 -- Internal Transaction byte 03" on page 479
38	INTERNAL_DATA_04	"Register 26h -- INTERNAL_DATA_04 -- Internal Transaction byte 04" on page 479
39	INTERNAL_DATA_05	"Register 27h -- INTERNAL_DATA_05 -- Internal Transaction byte 05" on page 479
40	INTERNAL_DATA_06	"Register 28h -- INTERNAL_DATA_06 -- Internal Transaction byte 06" on page 479
41	INTERNAL_DATA_07	"Register 29h -- INTERNAL_DATA_07 -- Internal Transaction byte 07" on page 480
42	INTERNAL_DATA_08	"Register 2Ah -- INTERNAL_DATA_08 -- Internal Transaction byte 08" on page 480
43	INTERNAL_DATA_09	"Register 2Bh -- INTERNAL_DATA_09 -- Internal Transaction byte 09" on page 480
44	INTERNAL_DATA_10	"Register 2Ch -- INTERNAL_DATA_10 -- Internal Transaction byte 10" on page 480
45	INTERNAL_DATA_11	"Register 2Dh -- INTERNAL_DATA_11 -- Internal Transaction byte 11" on page 480
46	INTERNAL_DATA_12	"Register 2Eh -- INTERNAL_DATA_12 -- Internal Transaction byte 12" on page 480
47	INTERNAL_DATA_13	"Register 2Fh -- INTERNAL_DATA_13 -- Internal Transaction byte 13" on page 480
48	INTERNAL_DATA_14	"Register 30h -- INTERNAL_DATA_14 -- Internal Transaction byte 14" on page 480
49	INTERNAL_DATA_15	"Register 31h -- INTERNAL_DATA_15 -- Internal Transaction byte 15" on page 480
50	INTERNAL_DATA_16	"Register 32h -- INTERNAL_DATA_16 -- Internal Transaction byte 16" on page 480
51	INTERNAL_DATA_17	"Register 33h -- INTERNAL_DATA_17 -- Internal Transaction byte 17" on page 481
52	INTERNAL_DATA_18	"Register 34h -- INTERNAL_DATA_18 -- Internal Transaction byte 18" on page 481
53	INTERNAL_DATA_19	"Register 35h -- INTERNAL_DATA_19 -- Internal Transaction byte 19" on page 481
64	AUX_STATUS	"Register 40h -- AUX_STATUS -- status bits" on page 481
65	AUX_RX_STATUS	"Register 41h -- AUX_RX_STATUS -- Status bits of the receive transaction" on page 481
66	EXTERNAL_TRANSACTION_READY	"Register 42h -- EXTERNAL_TRANSACTION_READY" on page 482

Table 166. 0xA00 AUX Channel Register Summary

Register Number	Register Name	Section #
67	EXTERNAL_STATUS	"Register 43h -- EXTERNAL_STATUS -- Status bits of the external transaction" on page 482
68	AUX_TX_STATUS	"Register 44h -- AUX_TX_STATUS -- status Bit of Transmit Transaction" on page 482
69	TIMER_STATUS	"Register 45h -- TIMER_STATUS -- Status Bits of the Timer" on page 482
90	AUX_POWER_STATE	"Register 5Ah -- AUX_POWER_STATE AUX Phy power state. Register length - 2 bits" on page 482
96	RECEIVE_TRANSACTION_LENGTH	"Register 60h -- RECEIVE_TRANSACTION_LENGTH -- the length of the receive transaction" on page 482
97	RECEIVE_DATA_00A	"Register 61h -- RECEIVE_DATA_00A -- Receive Transaction bits(7:4) of byte 00" on page 483
98	RECEIVE_DATA_00B	"Register 62h -- RECEIVE_DATA_00B -- Receive Transaction bits(3:0) of byte 00" on page 483
99	RECEIVE_DATA_01	"Register 63h -- RECEIVE_DATA_01 -- Receive Transaction byte 01" on page 483
100	RECEIVE_DATA_02	"Register 64h -- RECEIVE_DATA_02 -- Receive Transaction byte 02" on page 483
101	RECEIVE_DATA_03	"Register 65h -- RECEIVE_DATA_03 -- Receive Transaction byte 03" on page 483
102	RECEIVE_DATA_04	"Register 66h -- RECEIVE_DATA_04 -- Receive Transaction byte 04" on page 483
103	RECEIVE_DATA_05	"Register 67h -- RECEIVE_DATA_05 -- Receive Transaction byte 05" on page 483
104	RECEIVE_DATA_06	"Register 68h -- RECEIVE_DATA_06 -- Receive Transaction byte 06" on page 483
105	RECEIVE_DATA_07	"Register 69h -- RECEIVE_DATA_07 -- Receive Transaction byte 07" on page 483
106	RECEIVE_DATA_08	"Register 6Ah -- RECEIVE_DATA_08 -- Receive Transaction byte 08" on page 484
107	RECEIVE_DATA_09	"Register 6Bh -- RECEIVE_DATA_09 -- Receive Transaction byte 09" on page 484
108	RECEIVE_DATA_10	"Register 6Ch -- RECEIVE_DATA_10 -- Receive Transaction byte 10" on page 484
109	RECEIVE_DATA_11	"Register 6Dh -- RECEIVE_DATA_11 -- Receive Transaction byte 11" on page 484
110	RECEIVE_DATA_12	"Register 6Eh -- RECEIVE_DATA_12 -- Receive Transaction byte 12" on page 484
111	RECEIVE_DATA_13	"Register 6Fh -- RECEIVE_DATA_13 -- Receive Transaction byte 13" on page 484
112	RECEIVE_DATA_14	"Register 70h -- RECEIVE_DATA_14 -- Receive Transaction byte 14" on page 484
113	RECEIVE_DATA_15	"Register 71h -- RECEIVE_DATA_15 -- Receive Transaction byte 15" on page 484
114	RECEIVE_DATA_16	"Register 72h -- RECEIVE_DATA_16 -- Receive Transaction byte 16" on page 484

Table 166. 0xA00 AUX Channel Register Summary

Register Number	Register Name	Section #
115	RECEIVE_DATA_17	"Register 73h -- RECEIVE_DATA_17 -- Receive Transaction byte 17" on page 484
116	RECEIVE_DATA_18	"Register 74h -- RECEIVE_DATA_18 -- Receive Transaction byte 18" on page 485
117	RECEIVE_DATA_19	"Register 75h -- RECEIVE_DATA_19 -- Receive Transaction byte 19" on page 485
120	RECEIVE_LAST_TRANSACTION_LENGTH	"Register 78h -- RECEIVE_LAST_TRANSACTION_LENGTH -- the length of the receive transaction" on page 485
121	RECEIVE_LAST_DATA_LENGTH	"Register 79h -- RECEIVE_LAST_DATA_LENGTH -- Receive Transaction byte 03" on page 485
128	EXTERNAL_TRANSACTION_LENGTH	"Register 80h -- EXTERNAL_TRANSACTION_LENGTH -- the length of the external transaction" on page 485
129	EXTERNAL_DATA_00A	"Register 75h -- RECEIVE_DATA_19 -- Receive Transaction byte 19" on page 485
130	EXTERNAL_DATA_00B	"Register 75h -- RECEIVE_DATA_19 -- Receive Transaction byte 19" on page 485
131	EXTERNAL_DATA_01	"Register 83h -- EXTERNAL_DATA_01 -- External Transaction byte 01" on page 485
132	EXTERNAL_DATA_02	"Register 84h -- EXTERNAL_DATA_02 -- External Transaction byte 02" on page 485
133	EXTERNAL_DATA_03	"Register 85h -- EXTERNAL_DATA_03 -- External Transaction byte 03" on page 486
134	EXTERNAL_DATA_04	"Register 86h -- EXTERNAL_DATA_04 -- External Transaction byte 04" on page 486
135	EXTERNAL_DATA_05	"Register 87h -- EXTERNAL_DATA_05 -- External Transaction byte 05" on page 486
136	EXTERNAL_DATA_06	"Register 88h -- EXTERNAL_DATA_06 -- External Transaction byte 06" on page 486
137	EXTERNAL_DATA_07	"Register 89h -- EXTERNAL_DATA_07 -- External Transaction byte 07" on page 486
138	EXTERNAL_DATA_08	"Register 8Ah -- EXTERNAL_DATA_08 -- External Transaction byte 08" on page 486
139	EXTERNAL_DATA_09	"Register 8Bh -- EXTERNAL_DATA_09 -- External Transaction byte 09" on page 486
140	EXTERNAL_DATA_10	"Register 8Ch -- EXTERNAL_DATA_10 -- External Transaction byte 10" on page 486
141	EXTERNAL_DATA_11	"Register 8Dh -- EXTERNAL_DATA_11 -- External Transaction byte 11" on page 486
142	EXTERNAL_DATA_12	"Register 8Eh -- EXTERNAL_DATA_12 -- External Transaction byte 12" on page 486
143	EXTERNAL_DATA_13	"Register 8Fh -- EXTERNAL_DATA_13 -- External Transaction byte 13" on page 487
144	EXTERNAL_DATA_14	"Register 90h -- EXTERNAL_DATA_14 -- External Transaction byte 14" on page 487

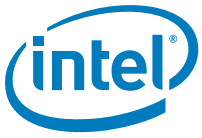


Table 166. 0xA00 AUX Channel Register Summary

Register Number	Register Name	Section #
145	EXTERNAL_DATA_15	"Register 91h -- EXTERNAL_DATA_15 -- External Transaction byte 15" on page 487
146	EXTERNAL_DATA_16	"Register 92h -- EXTERNAL_DATA_16 -- External Transaction byte 16" on page 487
147	EXTERNAL_DATA_17	"Register 93h -- EXTERNAL_DATA_17 -- External Transaction byte 17" on page 487
148	EXTERNAL_DATA_18	"Register 94h -- EXTERNAL_DATA_18 -- External Transaction byte 18" on page 487
149	EXTERNAL_DATA_19	"Register 95h -- EXTERNAL_DATA_19 -- External Transaction byte 19" on page 487
256	RX_DONE_ALL	"Register 100h -- RX_DONE_ALL -- counter rx_done" on page 487
257	RX_DONE_OK	"Register 101h -- RX_DONE_OK -- counter no error rx_done" on page 487
258	RX_DONE_LAST_EQUAL	"Register 102h -- RX_DONE_LAST_EQUAL -- counter rx_done with last_equal" on page 487
259	RX_DONE_ERRORS	"Register 103h -- RX_DONE_ERRORS -- counter rx_done with any error" on page 488
260	RX_DONE_ERROR_CORRUPTED	"Register 104h -- RX_DONE_ERROR_CORRUPTED -- counter corrupted_data errors" on page 488
261	RX_DONE_ERROR_LONG_DATA	"Register 105h -- RX_DONE_ERROR_LONG_DATA -- counter long_data errors" on page 488
262	RX_DONE_ERROR_LONG_PREAMBLE	"Register 106h -- RX_DONE_ERROR_LONG_PREAMBLE -- counter long_preamble errors" on page 488
263	RX_DONE_ERROR_CYCLE_TIME	"Register 107h -- RX_DONE_ERROR_CYCLE_TIME -- counter cycle_time errors" on page 488
272	TX_DONE_ALL	"Register 110h -- TX_DONE_ALL -- counter tx_done" on page 488
273	TX_DONE_NACK	"Register 111h -- TX_DONE_NACK -- counter tx_nack" on page 488
274	TX_DONE_INTERNAL	"Register 112h -- TX_DONE_INTERNAL -- counter tx_internal" on page 488
275	TX_DONE_EXTERNAL	"Register 113h -- TX_DONE_EXTERNAL -- counter tx_external" on page 488
280	EXPIRE_GLOBAL	"Register 118h -- EXPIRE_GLOBAL -- counter expire_global" on page 489
281	EXPIRE_INTERNAL	"Register 119h -- EXPIRE_INTERNAL -- counter expire_internal" on page 489
282	EXPIRE_EXTERNAL	"Register 11Ah -- EXPIRE_EXTERNAL -- counter expire_external" on page 489
288	ADAPTER_OUT	"Register 120h -- ADAPTER_OUT -- counter adapter_out" on page 489
289	ADAPTER_IN	"Register 121h -- ADAPTER_IN -- counter adapter_in" on page 489
290	ADAPTER_IN_EQUAL	"Register 122h -- ADAPTER_IN_EQUAL -- counter adapter_in_equal" on page 489

Table 166. 0xA00 AUX Channel Register Summary

Register Number	Register Name	Section #
291	ADAPTER_IN_LOAST_NEW	"Register 123h -- ADAPTER_IN_LOAST_NEW -- counter adapter_in_lost_new" on page 489
292	ADAPTER_IN_LOAST_PREVIOUS	"Register 124h -- ADAPTER_IN_LOAST_PREVIOUS -- counter adapter_in_lost_previous" on page 489
296	TX_STATE	"Register 128h -- TX_STATE" on page 489
297	TX_DATA	"Register 129h -- TX_DATA" on page 489
298	TX_COUNTER	"Register 12Ah -- TX_COUNTER" on page 490
304	RX_MAIN_STATE	"Register 130h -- RX_MAIN_STATE" on page 490
305	RX_PREAMBLE_STATE	"Register 131h -- RX_PREAMBLE_STATE" on page 491
306	RX_HHLL_STATE	"Register 132h -- RX_HHLL_STATE" on page 491
307	RX_DATA_STATE	"Register 133h -- RX_DATA_STATE" on page 491
308	RX_BYTE_COUNTER	"Register 134h -- RX_BYTE_COUNTER" on page 491
309	RX_SHIFT_REG	"Register 135h -- RX_SHIFT_REG" on page 491
310	RX_PREAMBLE_COUNTER	"Register 136h -- RX_PREAMBLE_COUNTER" on page 491
311	RX_CYCLE_COUNTER_LOW	"Register 137h -- RX_CYCLE_COUNTER_LOW" on page 491
312	RX_CYCLE_COUNTER_HIGH	"Register 138h -- RX_CYCLE_COUNTER_HIGH" on page 491
313	RX_LAST_CYCLE	"Register 139h -- RX_LAST_CYCLE" on page 491
314	RX_SUM_CYCLE_LOW	"Register 13Ah -- RX_SUM_CYCLE_LOW" on page 492
315	RX_SUM_CYCLE_HIGH	"Register 13Bh -- RX_SUM_CYCLE_HIGH" on page 492
316	RX_CYCLE_AVERAGE	"Register 13Ch -- RX_CYCLE_AVERAGE" on page 492
317	RX_TICK_CYCLE	"Register 13Dh -- RX_TICK_CYCLE" on page 492
320	MAIN_STATES	"Register 140h -- MAIN_STATES" on page 492
321	MAIN_TIMER_LOW	"Register 141h -- MAIN_TIMER_LOW" on page 492
322	MAIN_TIMER_HIGH	"Register 142h -- MAIN_TIMER_HIGH" on page 492
323	MAIN_RX_TO_ADAPTER_COUNTER	"Register 143h -- MAIN_RX_TO_ADAPTER_COUNTER" on page 492
324	MAIN_EXTERNAL_STATE	"Register 144h -- MAIN_EXTERNAL_STATE" on page 492
325	MAIN_EXTERNAL_COUNTER	"Register 145h -- MAIN_EXTERNAL_COUNTER" on page 493
326	MAIN_TX_MUX_COUNTER	"Register 146h -- MAIN_TX_MUX_COUNTER" on page 493
328	AUX_AFE_IN	"Register 148h -- AUX_AFE_IN" on page 493
329	AUX_AFE_OUT	"Register 149h -- AUX_AFE_OUT" on page 493
330	AUX_CHICKEN0	"Register 150h -- AUX_CHICKEN0 Extension of Tx transaction - 2 bits" on page 493

4.6.2.4.1 Register 0h -- HOST_CONTROL -- control bits

Address offset	Name	Description	Mode	Default
0.4	aux_host_always_read	Normally the aux_rx is disabled during transmit. Setting this bit allow loopback operation and all transmit transactions will be enter to the receiver. Use for debugging	RW	0
0.3	aux_host_precharge_enable	According to the current standard the tx precharge is done by sending 10 to 16 data_0 on the line before the SYNC. Old standard define the precharge by forcing the AFE to be in precharge mode before start transmitting the SYNC	RW	0
0.2	aux_host_transmit_immediate_reg	This bit is used only in DP_OUT mode. If SET, a transaction that comes from the adapter will be sent immediately without waiting to send_external_transaction pulse. If CLEAR the MC controls the traffic to/from adapter.	RW	1
0.1:0	aux_host_average_no_of_cycles	Calculate the cycle time by doing average of the last 2,4,8 cycles in the preamble(00-2 cycles,01-4 cycles,1x-8 cycles)	RW	10

4.6.2.4.2 Register 1h -- SWAP_CONTROL -- control the bit ordering of transmit & receive

Address offset	Name	Description	Mode	Default
1.1	aux_host_tx_swap	shift right the output data (LSB first)	RW	0
1.0	aux_host_rx_swap	shift right (LSB first) of the income data	RW	0

4.6.2.4.3 Register 8h -- SEND_INTERNAL_TRANSACTION -- send internal transaction by AUX_TX

Address offset	Name	Description	Mode	Default
8.0	aux_host_send_internal_transaction	send internal transaction by AUX_TX	WO	0

4.6.2.4.4 Register 9h -- SEND_EXTERNAL_TRANSACTION -- send external transaction by AUX_TX

Address offset	Name	Description	Mode	Default
9.0	aux_host_send_external_transaction	send external transaction by AUX_TX	WO	0

4.6.2.4.5 Register Ah -- SEND_NACK_TRANSACTION -- send nack transaction by AUX_TX

Address offset	Name	Description	Mode	Default
10.0	aux_host_send_nack_transaction	send nack transaction by AUX_TX	WO	0

4.6.2.4.6 Register Bh -- SEND_TO_ADAPTER -- forward the receive transaction to the adapter

Address offset	Name	Description	Mode	Default
11.0	aux_host_forward_rx_to_adpater	forward the receive transaction to the adapter. It also enable the AUX_RX as the "enable_rx"	WO	0

4.6.2.4.7 Register Ch -- CLEAR_RX -- Clear all rx bits

Address offset	Name	Description	Mode	Default
12.0	aux_host_clear_rx	clear all rx bits in register 64,65.This command is an indication that the processing of last receive transaction was completed and the AUX_RX can start looking for new receive transaction.	WO	0

4.6.2.4.8 Register Dh -- CLEAR_EXTERNAL -- Clear all external bits

Address offset	Name	Description	Mode	Default
13.0	aux_host_clear_external	clear all external bits in registers 64,67	WO	

4.6.2.4.9 Register Eh -- CLEAR_TIMER -- Clear timer expire bits

Address offset	Name	Description	Mode	Default
14.0	aux_host_clear_timer	clear all expire bits in reg 64	WO	0

4.6.2.4.10 Register Fh -- RESET_DP_AUX_SW -- S/W reset of the DP_AUX

Address offset	Name	Description	Mode	Default
15.0	aux_host_sw_reset	Reset all DP_AUX state machines and clear all the status bits. The registers value remains. (S/W reset)	WO	0

4.6.2.4.11 Register 10h -- DIVIDE_2M -- the ratio between sys_clk and 2MHz

Address offset	Name	Description	Mode	Default
16.7:0	aux_host_divide_2m	The ratio between sys_clk and 2MHz, [(sys_clk frequency/2MHz) - 1], for 25MHz sys_clk the value is 11. This register is used by AUX_TX for generating the AUX_TX clock.	RW	11

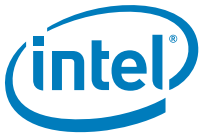
4.6.2.4.12 Register 11h -- TX_PREACHARGE _LENGTH -- length of precharge field

Address offset	Name	Description	Mode	Default
17.5:0	aux_host_precharge_length	length of precharge field, standard definition is 10 to 16 bits/clocks	RW	16

4.6.2.4.13 Register 14h -- FREQUENCY_1M_MAX -- maximum legal frequency receiving from the line

Address offset	Name	Description	Mode	Default
20.7:0	aux_host_1m_max	The maximum legal frequency receiving from the line by the standard is 1.25MHz.The calculation is: (1.25 MHz cycle time)/(sys_clk(-15%) cycle time) -1 800/47-1=16	RW	16

4.6.2.4.14 Register 15h -- FREQUENCY_1M_MIN -- minimum legal frequency receiving



from the line

Address offset	Name	Description	Mode	Default
21.7:0	aux_host_1m_min	The minimum legal frequency receiving from the line by the standard is 0.83MHz.The calculation is: (0.83 MHz cycle time)/(sys_clk(+15%) cycle time) -1 1200/35-1=34	RW	34

4.6.2.4.15 Register 16h -- RX_PRE _MIN -- minimum length of preamble during receive

Address offset	Name	Description	Mode	Default
22.5:0	aux_host_pre_min	Valid minimum length of preamble during receive. The standard defines pre_min = 26. Restriction: The value of this register should be greater than the "average_number_of_cycles defined in reg 0 (2, 4 or 8)	RW	10

4.6.2.4.16 Register 17h -- RX_PRE_MAX -- maximum length of preamble during receive

Address offset	Name	Description	Mode	Default
23.5:0	aux_host_pre_max	Valid maximum length of preamble during receive. The standard defines pre_max = 32	RW	35

4.6.2.4.17 Register 18h -- TIMER_PRESET_DP_IN_HIGH -- The preset value (HIGH part) of the timer in DP_IN mode

Address offset	Name	Description	Mode	Default
24.7:0	timer_preset_dp_in_high	The preset value of the timer in DP_IN mode. With sys_clk= 25MHz the Timer can measure up to ~2500 micro seconds. The defaults value is 300 microseconds (1D4c in Hex)	RW	1Dh

4.6.2.4.18 Register 19h -- TIMER_PRESET_DP_IN_LOW -- The preset value (LOW part) of the timer in DP_IN mode

Address offset	Name	Description	Mode	Default
25.7:0	timer_preset_dp_in_low		RW	4Ch

4.6.2.4.19 Register 1Ah -- TIMER_PRESET_DP_OUT_HIGH -- The preset value (HIGH part) of the timer in DP_OUT mode

Address offset	Name	Description	Mode	Default
26.7:0	timer_preset_dp_out_high	The preset value of the timer in DP_OUT mode. With sys_clk= 25MHz the Timer can measure up to ~2500 micro seconds. The defaults value is 400 microseconds (2710 in Hex)	RW	27h

4.6.2.4.20 Register 1Bh -- TIMER_PRESET_DP_OUT_LOW -- The preset value LOW part) of the timer in DP_OUT mode

Address offset	Name	Description	Mode	Default
27.7:0	timer_preset_dp_out_low		RW	10h

4.6.2.4.21 Register 1Ch -- NACK_FORMAT -- "nack" or "defer" pattern for transmit

Address offset	Name	Description	Mode	Default
28.7:0	aux_host_nack_format	nack or defer pattern for transmit (00100000 for defer, 00010000 for nack)	RW	00100000

4.6.2.4.22 Register 20h -- INTERNAL_TRANSACTION_LENGTH -- length of the internal transaction

Address offset	Name	Description	Mode	Default
32.4:0	aux_host_internal_length	The length of the internal transaction (maximum 20 bytes)	RW	0

4.6.2.4.23 Register 21h -- INTERNAL_DATA_00A -- Internal Transaction bits(7:4) of byte 0

Address offset	Name	Description	Mode	Default
33.3:0	internal_data_00a		RW	0

4.6.2.4.24 Register 22h -- INTERNAL_DATA_00B -- Internal Transaction bits(3:0) of byte 0

Address offset	Name	Description	Mode	Default
34.3:0	internal_data_00b		RW	0

4.6.2.4.25 Register 23h -- INTERNAL_DATA_01 -- Internal Transaction byte 01

Address offset	Name	Description	Mode	Default
35.7:0	internal_data_01	Internal Transaction byte 1	RW	0

4.6.2.4.26 Register 24h -- INTERNAL_DATA_02 -- Internal Transaction byte 02

Address offset	Name	Description	Mode	Default
36.7:0	internal_data_02	Internal Transaction byte 2	RW	0

4.6.2.4.27 Register 25h -- INTERNAL_DATA_03 -- Internal Transaction byte 03

Address offset	Name	Description	Mode	Default
37.7:0	internal_data_03	Internal Transaction byte 3	RW	0

4.6.2.4.28 Register 26h -- INTERNAL_DATA_04 -- Internal Transaction byte 04

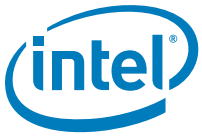
Address offset	Name	Description	Mode	Default
38.7:0	internal_data_04	Internal Transaction byte 4	RW	0

4.6.2.4.29 Register 27h -- INTERNAL_DATA_05 -- Internal Transaction byte 05

Address offset	Name	Description	Mode	Default
39.7:0	internal_data_05		RW	0

4.6.2.4.30 Register 28h -- INTERNAL_DATA_06 -- Internal Transaction byte 06

Address offset	Name	Description	Mode	Default
40.7:0	internal_data_07		RW	0



4.6.2.4.31 Register 29h -- INTERNAL_DATA_07 -- Internal Transaction byte 07

Address offset	Name	Description	Mode	Default
41.7:0	internal_data_07		RW	0

4.6.2.4.32 Register 2Ah -- INTERNAL_DATA_08 -- Internal Transaction byte 08

Address offset	Name	Description	Mode	Default
42.7:0	internal_data_08		RW	0

4.6.2.4.33 Register 2Bh -- INTERNAL_DATA_09 -- Internal Transaction byte 09

Address offset	Name	Description	Mode	Default
43.7:0	internal_data_09		RW	0

4.6.2.4.34 Register 2Ch -- INTERNAL_DATA_10 -- Internal Transaction byte 10

Address offset	Name	Description	Mode	Default
44.7:0	internal_data_10		RW	0

4.6.2.4.35 Register 2Dh -- INTERNAL_DATA_11 -- Internal Transaction byte 11

Address offset	Name	Description	Mode	Default
45.7:0	internal_data_11		RW	0

4.6.2.4.36 Register 2Eh -- INTERNAL_DATA_12 -- Internal Transaction byte 12

Address offset	Name	Description	Mode	Default
46.7:0	internal_data_12		RW	0

4.6.2.4.37 Register 2Fh -- INTERNAL_DATA_13 -- Internal Transaction byte 13

Address offset	Name	Description	Mode	Default
47.7:0	internal_data_13		RW	0

4.6.2.4.38 Register 30h -- INTERNAL_DATA_14 -- Internal Transaction byte 14

Address offset	Name	Description	Mode	Default
48.7:0	internal_data_14		RW	0

4.6.2.4.39 Register 31h -- INTERNAL_DATA_15 -- Internal Transaction byte 15

Address offset	Name	Description	Mode	Default
49.7:0	internal_data_15		RW	0

4.6.2.4.40 Register 32h -- INTERNAL_DATA_16 -- Internal Transaction byte 16

Address offset	Name	Description	Mode	Default
50.7:0	internal_data_16		RW	0

4.6.2.4.41 Register 33h -- INTERNAL_DATA_17 -- Internal Transaction byte 17

Address offset	Name	Description	Mode	Default
51.7:0	internal_data_17		RW	0

4.6.2.4.42 Register 34h -- INTERNAL_DATA_18 -- Internal Transaction byte 18

Address offset	Name	Description	Mode	Default
52.7:0	internal_data_18		RW	0

4.6.2.4.43 Register 35h -- INTERNAL_DATA_19 -- Internal Transaction byte 19

Address offset	Name	Description	Mode	Default
53.7:0	internal_data_19		RW	0

4.6.2.4.44 Register 40h -- AUX_STATUS -- status bits

Address offset	Name	Description	Mode	Default
64.7	Reserved			
64.6	aux_main_expire_external	timer expire (external) in DP_OUT	RO	0
64.5	aux_main_expire_internal	timer expire (internal) in DP_OUT	RO	0
64.4	aux_main_expire_global	timer expire in DP_IN, (internal or external)	RO	0
64.3	aux_main_external_ready	AUX_MAIN read all transaction data from adapter. The transaction is ready for transmit by AUX_TX	RO	0
64.2	aux_main_rx_status_done_external	AUX_RX in DP_OUT mode, completed processing the receiving of external transaction	RO	0
64.1	aux_main_rx_status_done_internal	AUX_RX in DP_OUT mode, completed processing the receiving of internal transaction	RO	0
64.0	aux_main_rx_status_done	AUX_RX in DP_IN mode, completed processing the receiving transaction (internal or external)	RO	0 offset

4.6.2.4.45 Register 41h -- AUX_RX_STATUS -- Status bits of the receive transaction

Address offset	Name	Description	Mode	Default
65.7:6	Reserved			
65.5	aux_main_rx_status_error_corrupted	the received transaction corrupted during the data phase (bad STOP, or un aligned STOP)	RO	0
65.4	aux_main_rx_status_error_cycle_time	during the received transaction the AUX_RX measured clock cycle that is not on the allowed tolerance (<0.4 ms or >0.6 ms)	RO	0
65.3	aux_main_rx_status_error_long_data	the received transaction had more than 20 data bytes	RO	0
65.2	aux_main_rx_status_error_long_preamble	the received transaction had preamble greater than the preamble_max	RO	0
65.1	aux_main_rx_status_last_equal	The receive transaction is equal to the previous transaction. (THIS IS NOT ERROR BIT !!)	RO	0
65.0	aux_main_rx_status_error	The transaction has an error. This bit is or of all error bits in this register	RO	0

4.6.2.4.46 Register 42h -- EXTERNAL_TRANSACTION_READY

Address offset	Name	Description	Mode	Default
66.0	aux_main_external_ready	AUX_MAIN read all transaction data from adapter. The transaction is ready for transmit by AUX_TX	RO	0

4.6.2.4.47 Register 43h -- EXTERNAL_STATUS -- Status bits of the external transaction

Address offset	Name	Description	Mode	Default
67.4	aux_main_external_error_lost_new_equal	The new lost transaction is equal to the current transaction	RO	0
67.3	aux_main_external_error_lost_new	A new transaction lost during transmitting of the current transaction.	RO	0
67.2	aux_main_external_error_lost_previous_equal	The equal bit of the lost previous transaction	RO	0
67.1	aux_main_external_error_lost_previous	the adapter writes new transaction to the DP_AUX before the previous transaction started its transmission. The previous transaction lost.	RO	0
67.0	aux_main_external_equal_to_last	The current external transaction is equal to the previous external transaction	RO	0

4.6.2.4.48 Register 44h -- AUX_TX_STATUS -- status Bit of Transmit Transaction

Address offset	Name	Description	Mode	Default
68.2	aux_main_tx_status_done_external	AUX_TX completed the transmitting of external transaction	RO	0
68.1	aux_main_tx_status_done_internal	AUX_TX completed the transmitting of internal transaction	RO	0
68.0	aux_main_tx_status_done	AUX_TX completed the transmitting of the transaction	RO	0

4.6.2.4.49 Register 45h -- TIMER_STATUS -- Status Bits of the Timer

Address offset	Name	Description	Mode	Default
69.2	aux_main_expire_external	timer expire (external)	RO	0
69.1	aux_main_expire_internal	timer expire (internal)	RO	0
69.0	aux_main_expire_global	timer expire, (internal or external)	RO	0

4.6.2.4.50 Register 5Ah -- AUX_POWER_STATE AUX Phy power state. Register length - 2 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
90	1:0	aux_phy_power_state	Power state of AUX Phy: 0 – Active 1 – Power Down 2 - HiZ	R/W	2

4.6.2.4.51 Register 60h -- RECEIVE_TRANSACTION_LENGTH -- the length of the receive

transaction

Address offset	Name	Description	Mode	Default
96.4:0	aux_rx_length	the length of the receive transaction (maximum 20 bytes)	RW	00000

4.6.2.4.52 Register 61h -- RECEIVE_DATA_00A -- Receive Transaction bits(7:4) of byte 00

Address offset	Name	Description	Mode	Default
97.3:0	rx_data_00a		RW	0h

4.6.2.4.53 Register 62h -- RECEIVE_DATA_00B -- Receive Transaction bits(3:0) of byte 00

Address offset	Name	Description	Mode	Default
98.3:0	rx_data_00b		RW	0h

4.6.2.4.54 Register 63h -- RECEIVE_DATA_01 -- Receive Transaction byte 01

Address offset	Name	Description	Mode	Default
99.7:0	rx_data_01		RW	0h

4.6.2.4.55 Register 64h -- RECEIVE_DATA_02 -- Receive Transaction byte 02

Address offset	Name	Description	Mode	Default
100.7:0	rx_data_02		RW	0h

4.6.2.4.56 Register 65h -- RECEIVE_DATA_03 -- Receive Transaction byte 03

Address offset	Name	Description	Mode	Default
101.7:0	rx_data_0		RW	0h

4.6.2.4.57 Register 66h -- RECEIVE_DATA_04 -- Receive Transaction byte 04

Address offset	Name	Description	Mode	Default
102.7:0	rx_data_04		RW	0h

4.6.2.4.58 Register 67h -- RECEIVE_DATA_05 -- Receive Transaction byte 05

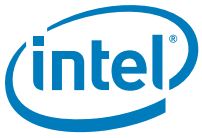
Address offset	Name	Description	Mode	Default
103.7:0	rx_data_05		RW	0h

4.6.2.4.59 Register 68h -- RECEIVE_DATA_06 -- Receive Transaction byte 06

Address offset	Name	Description	Mode	Default
104.7:0	rx_data_06		RW	0h

4.6.2.4.60 Register 69h -- RECEIVE_DATA_07 -- Receive Transaction byte 07

Address offset	Name	Description	Mode	Default
105.7:0	rx_data_07		RW	0h



4.6.2.4.61 Register 6Ah -- RECEIVE_DATA_08 -- Receive Transaction byte 08

Address offset	Name	Description	Mode	Default
106.7:0	rx_data_08		RW	0h

4.6.2.4.62 Register 6Bh -- RECEIVE_DATA_09 -- Receive Transaction byte 09

Address offset	Name	Description	Mode	Default
107.7:0	rx_data_09		RW	0h

4.6.2.4.63 Register 6Ch -- RECEIVE_DATA_10 -- Receive Transaction byte 10

Address offset	Name	Description	Mode	Default
108.7:0	rx_data_10		RW	0h

4.6.2.4.64 Register 6Dh -- RECEIVE_DATA_11 -- Receive Transaction byte 11

Address offset	Name	Description	Mode	Default
109.7:0	rx_data_11		RW	0h

4.6.2.4.65 Register 6Eh -- RECEIVE_DATA_12 -- Receive Transaction byte 12

Address offset	Name	Description	Mode	Default
110.7:0	rx_data_12		RW	0h

4.6.2.4.66 Register 6Fh -- RECEIVE_DATA_13 -- Receive Transaction byte 13

Address offset	Name	Description	Mode	Default
111.7:0	rx_data_13		RW	0h

4.6.2.4.67 Register 70h -- RECEIVE_DATA_14 -- Receive Transaction byte 14

Address offset	Name	Description	Mode	Default
112.7:0	rx_data_14		RW	0h

4.6.2.4.68 Register 71h -- RECEIVE_DATA_15 -- Receive Transaction byte 15

Address offset	Name	Description	Mode	Default
113.7:0	rx_data_15		RW	0h

4.6.2.4.69 Register 72h -- RECEIVE_DATA_16 -- Receive Transaction byte 16

Address offset	Name	Description	Mode	Default
114.7:0	rx_data_16		RW	0h

4.6.2.4.70 Register 73h -- RECEIVE_DATA_17 -- Receive Transaction byte 17

Address offset	Name	Description	Mode	Default
115.7:0	rx_data_17		RW	0h

4.6.2.4.71 Register 74h -- RECEIVE_DATA_18 -- Receive Transaction byte 18

Address offset	Name	Description	Mode	Default
116.7:0	rx_data_18		RW	0h

4.6.2.4.72 Register 75h -- RECEIVE_DATA_19 -- Receive Transaction byte 19

Address offset	Name	Description	Mode	Default
117.7:0	rx_data_19		RW	0h

4.6.2.4.73 Register 78h -- RECEIVE_LAST_TRANSACTION_LENGTH -- the length of the receive transaction

Address offset	Name	Description	Mode	Default
120.4:0	aux_rx_last_transaction_length	shadow register of reg 96.	RO	0h

4.6.2.4.74 Register 79h -- RECEIVE_LAST_DATA_LENGTH -- Receive Transaction byte 03

Address offset	Name	Description	Mode	Default
121.7:0	aux_rx_last_data_length	shadow register of RECEIVE_DATA_05 reg. It contains the data_length field of auxiliary transaction	RO	0h

4.6.2.4.75 Register 80h -- EXTERNAL_TRANSACTION_LENGTH -- the length of the external transaction

Address offset	Name	Description	Mode	Default
128.4:0	aux_main_external_length	the length of the external transaction (maximum 20 bytes)	RW	0h

4.6.2.4.76 Register 81h -- EXTERNAL_DATA_00A -- External Transaction bits(7:4) of byte 00

Address offset	Name	Description	Mode	Default
129.3:0	external_data_00a		RW	0h

4.6.2.4.77 Register 82h -- EXTERNAL_DATA_00B -- External Transaction bits(3:0) of byte 00

Address offset	Name	Description	Mode	Default
130.3:0	external_data_00b		RW	0h

4.6.2.4.78 Register 83h -- EXTERNAL_DATA_01 -- External Transaction byte 01

Address offset	Name	Description	Mode	Default
131.7:0	external_data_01		RW	0h

4.6.2.4.79 Register 84h -- EXTERNAL_DATA_02 -- External Transaction byte 02

Address offset	Name	Description	Mode	Default
132.7:0	external_data_02		RW	0h

4.6.2.4.80 Register 85h -- EXTERNAL_DATA_03 -- External Transaction byte 03

Address offset	Name	Description	Mode	Default
133.7:0	external_data_03		RW	0h

4.6.2.4.81 Register 86h -- EXTERNAL_DATA_04 -- External Transaction byte 04

Address offset	Name	Description	Mode	Default
134.7:0	external_data_04		RW	0h

4.6.2.4.82 Register 87h -- EXTERNAL_DATA_05 -- External Transaction byte 05

Address offset	Name	Description	Mode	Default
135.7:0	external_data_05		RW	0h

4.6.2.4.83 Register 88h -- EXTERNAL_DATA_06 -- External Transaction byte 06

Address offset	Name	Description	Mode	Default
136.7:0	external_data_06		RW	0h

4.6.2.4.84 Register 89h -- EXTERNAL_DATA_07 -- External Transaction byte 07

Address offset	Name	Description	Mode	Default
137.7:0	external_data_07		RW	0h

4.6.2.4.85 Register 8Ah -- EXTERNAL_DATA_08 -- External Transaction byte 08

Address offset	Name	Description	Mode	Default
138.7:0	external_data_08		RW	0h

4.6.2.4.86 Register 8Bh -- EXTERNAL_DATA_09 -- External Transaction byte 09

Address offset	Name	Description	Mode	Default
139.7:0	external_data_09		RW	0h

4.6.2.4.87 Register 8Ch -- EXTERNAL_DATA_10 -- External Transaction byte 10

Address offset	Name	Description	Mode	Default
140.7:0	external_data_10		RW	0h

4.6.2.4.88 Register 8Dh -- EXTERNAL_DATA_11 -- External Transaction byte 11

Address offset	Name	Description	Mode	Default
141.7:0	external_data_11		RW	0h

4.6.2.4.89 Register 8Eh -- EXTERNAL_DATA_12 -- External Transaction byte 12

Address offset	Name	Description	Mode	Default
142.7:0	external_data_12		RW	0h

4.6.2.4.90 Register 8Fh -- EXTERNAL_DATA_13 -- External Transaction byte 13

Address offset	Name	Description	Mode	Default
143.7:0	external_data_13		RW	0h

4.6.2.4.91 Register 90h -- EXTERNAL_DATA_14 -- External Transaction byte 14

Address offset	Name	Description	Mode	Default
144.7:0	external_data_14		RW	0h

4.6.2.4.92 Register 91h -- EXTERNAL_DATA_15 -- External Transaction byte 15

Address offset	Name	Description	Mode	Default
145.7:0	external_data_15		RW	0h

4.6.2.4.93 Register 92h -- EXTERNAL_DATA_16 -- External Transaction byte 16

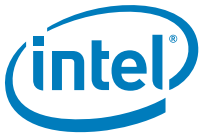
Address offset	Name	Description	Mode	Default
146.7:0	external_data_16		RW	0h

4.6.2.4.94 Register 93h -- EXTERNAL_DATA_17 -- External Transaction byte 17

Address offset	Name	Description	Mode	Default
147.7:0	external_data_17		RW	0h

4.6.2.4.95 Register 94h -- EXTERNAL_DATA_18 -- External Transaction byte 18

Address offset	Name	Description	Mode	Default
148.7:0	external_data_18		RW	0h



4.6.2.4.96 Register 95h -- EXTERNAL_DATA_19 -- External Transaction byte 19

Address offset	Name	Description	Mode	Default
149.7:0	external_data_19		RW	0h

4.6.2.4.97 Register 100h -- RX_DONE_ALL -- counter rx_done

Address offset	Name	Description	Mode	Default
256.7:0	rx_done_all	count all receive transactions	RW	0h

4.6.2.4.98 Register 101h -- RX_DONE_OK -- counter no error rx_done

Address offset	Name	Description	Mode	Default
257.7:0	rx_done_ok	count all receive transactions without any error	RW	0h

4.6.2.4.99 Register 102h -- RX_DONE_LAST_EQUAL -- counter rx_done with last_equal

Address offset	Name	Description	Mode	Default
258.7:0	rx_done_last_equal	count all receive transactions without any error that were equal to their previous transaction	RW	0h

4.6.2.4.100 Register 103h -- RX_DONE_ERRORS -- counter rx_done with any error

Address offset	Name	Description	Mode	Default
259.7:0	rx_done_errors	count all receive transactions with any error	RW	0h

4.6.2.4.101 Register 104h -- RX_DONE_ERROR_CORRUPTED -- counter corrupted_data errors

Address offset	Name	Description	Mode	Default
260.7:0	rx_done_error_corrupted_data	count receive transactions with error corrupted_data	RW	0h

4.6.2.4.102 Register 105h -- RX_DONE_ERROR_LONG_DATA -- counter long_data errors

Address offset	Name	Description	Mode	Default
261.7:0	rx_done_error_long_data	count receive transactions with error long_data	RW	0h

4.6.2.4.103 Register 106h -- RX_DONE_ERROR_LONG_PREAMBLE -- counter long_preamble errors

Address offset	Name	Description	Mode	Default
262.7:0	rx_done_error_long_preamble	count receive transactions with error long_preamble	RW	0h

4.6.2.4.104 Register 107h -- RX_DONE_ERROR_CYCLE_TIME -- counter cycle_time errors

Address offset	Name	Description	Mode	Default
263.7:0	rx_done_error_cycle_time	count receive transactions with error cycle_time	RW	0h

4.6.2.4.105 Register 110h -- TX_DONE_ALL -- counter tx_done

Address offset	Name	Description	Mode	Default
272.7:0	tx_done_all	count all transmit transactions	RW	0h

4.6.2.4.106 Register 111h -- TX_DONE_NACK -- counter tx_nack

Address offset	Name	Description	Mode	Default
273.7:0	tx_done_nack	count all transmit nack/defer transactions	RW	0h

4.6.2.4.107 Register 112h -- TX_DONE_INTERNAL -- counter tx_internal

Address offset	Name	Description	Mode	Default
274.7:0	tx_done_internal	count all transmit internal transactions	RW	0h

4.6.2.4.108 Register 113h -- TX_DONE_EXTERNAL -- counter tx_external

Address offset	Name	Description	Mode	Default
275.7:0	tx_done_external	count all transmit external transactions	RW	0h

4.6.2.4.109 Register 118h -- EXPIRE_GLOBAL -- counter expire_global

Address offset	Name	Description	Mode	Default
280.7:0	expire_global_all	count all expire_global events	RW	0h

4.6.2.4.110 Register 119h -- EXPIRE_INTERNAL -- counter expire_internal

Address offset	Name	Description	Mode	Default
281.7:0	expire_internal_all	count all expire_internal events	RW	0h

4.6.2.4.111 Register 11Ah -- EXPIRE_EXTERNAL -- counter expire_external

Address offset	Name	Description	Mode	Default
282.7:0	expire_external_all	count all expire_external events	RW	0h

4.6.2.4.112 Register 120h -- ADAPTER_OUT -- counter adapter_out

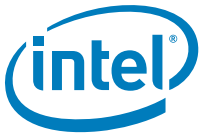
Address offset	Name	Description	Mode	Default
288.7:0	adapter_out_all	count all rx to adapter events	RW	0h

4.6.2.4.113 Register 121h -- ADAPTER_IN -- counter adapter_in

Address offset	Name	Description	Mode	Default
289.7:0	adapter_in_all	count all adapter in bursts	RW	0h

4.6.2.4.114 Register 122h -- ADAPTER_IN_EQUAL -- counter adapter_in_equal

Address offset	Name	Description	Mode	Default
290.7:0	adapter_in_equal	count all adapter in bursts that were equal to the previous burst	RW	0h



4.6.2.4.115 Register 123h -- ADAPTER_IN_LOAST_NEW -- counter adapter_in_lost_new

Address offset	Name	Description	Mode	Default
291.7:0	adapter_in_lost_new_all	count all new adapter in bursts that were lost since the previous burst is in process (DP_IN and DP_OUT) or was not transmitted yet (DP_IN)	RW	0h

4.6.2.4.116 Register 124h -- ADAPTER_IN_LOAST_PREVIOUS -- counter adapter_in_lost_previous

Address offset	Name	Description	Mode	Default
292.7:0	adpter_in_lost_previous_all	count all the previous adapter in bursts that over write by new bursts	RW	0h

4.6.2.4.117 Register 128h -- TX_STATE

Address offset	Name	Description	Mode	Default
296.6:0	aux_tx_state	aux_tx state machine register	RO	1h

4.6.2.4.118 Register 129h -- TX_DATA

Address offset	Name	Description	Mode	Default
297.7:0	aux_tx_data_reg	from this register the serial data is transmitted	RO	0h

4.6.2.4.119 Register 12Ah -- TX_COUNTER

Address offset	Name	Description	Mode	Default
298.6	aux_tx_down_count_end	count end of down counter	RO	0
298.5:0	aux_tx_down_counter	down counter for AUX_TX state machine	RO	3Fh

4.6.2.4.120 Register 130h -- RX_MAIN_STATE

Address offset	Name	Description	Mode	Default
304.4:0	aux_rx_main_state	AUX_RX main state machine register	RO	2h

4.6.2.4.121 Register 131h -- RX_PREAMBLE_STATE

Address offset	Name	Description	Mode	Default
305.5:0	aux_rx_preamble_state	AUX_RX preamble state machine register	RO	2h

4.6.2.4.122 Register 132h -- RX_HHLL_STATE

Address offset	Name	Description	Mode	Default
306.3:0	aux_rx_hhll_state	AUX_RX hhll state machine register	RO	1h

4.6.2.4.123 Register 133h -- RX_DATA_STATE

Address offset	Name	Description	Mode	Default
307.7:0	aux_rx_data_state	AUX_RX data state machine register	RO	1h

4.6.2.4.124 Register 134h -- RX_BYTE_COUNTER

Address offset	Name	Description	Mode	Default
308.4:0	aux_rx_byte_counter	count income data bytes	RO	0h

4.6.2.4.125 Register 135h -- RX_SHIFT_REG

Address offset	Name	Description	Mode	Default
309.7:0	aux_rx_shift_reg	receive shift register	RO	0h

4.6.2.4.126 Register 136h -- RX_PREAMBLE_COUNTER

Address offset	Name	Description	Mode	Default
310.6:0	aux_rx_preamble_counter	count size of preamble	RO	0h

4.6.2.4.127 Register 137h -- RX_CYCLE_COUNTER_LOW

Address offset	Name	Description	Mode	Default
311.7:0	aux_rx_cycle_counter	count system clocks from last change in the auxiliary line input (low part)	RO	0h

4.6.2.4.128 Register 138h -- RX_CYCLE_COUNTER_HIGH

Address offset	Name	Description	Mode	Default
312.2:0	aux_rx_cycle_counter	count system clocks from last change in the auxiliary line input (high part)	RO	0h

4.6.2.4.129 Register 139h -- RX_LAST_CYCLE

Address offset	Name	Description	Mode	Default
313.7:0	aux_rx_last_cycle	last cycle	RO	0h

4.6.2.4.130 Register 13Ah -- RX_SUM_CYCLE_LOW

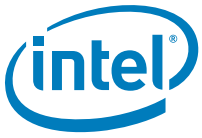
Address offset	Name	Description	Mode	Default
314.7:0	aux_rx_sum_cycles_low	sum of last 8 (or 4 or 2) cycles during preamble (low part)	RO	0h

4.6.2.4.131 Register 13Bh -- RX_SUM_CYCLE_HIGH

Address offset	Name	Description	Mode	Default
315.2:0	aux_rx_sum_cycles_high	sum of last 8 (or 4 or 2) cycles during preamble (high part)	RO	0h

4.6.2.4.132 Register 13Ch -- RX_CYCLE_AVERAGE

Address offset	Name	Description	Mode	Default
316.7:0	cycle_average	cycle average from last preamble cycles	RO	0h



4.6.2.4.133 Register 13Dh -- RX_TICK_CYCLE

Address offset	Name	Description	Mode	Default
317.7:0	tick_cycle	current reference cycle	RO	0h

4.6.2.4.134 Register 140h -- MAIN_STATES

Address offset	Name	Description	Mode	Default
320.6	Reserved			0
320.5	aux_main_tx_state		RO	0
320.4:3	aux_main_rx_state	AUX_MAIN rx state machine register	RO	0h
320.2:1	aux_main_dp_state	AUX_MAIN dp state machine register	RO	0h
320.0	aux_main_timer_state	AUX_MAIN timer state machine register	RO	0h

4.6.2.4.135 Register 141h -- MAIN_TIMER_LOW

Address offset	Name	Description	Mode	Default
321.7:0	aux_main_timer	timer (low part)	RO	FFh

4.6.2.4.136 Register 142h -- MAIN_TIMER_HIGH

Address offset	Name	Description	Mode	Default
322.7:0	aux_main_timer	timer (high part)	RO	FFh

4.6.2.4.137 Register 143h -- MAIN_RX_TO_ADAPTER_COUNTER

Address offset	Name	Description	Mode	Default
323.4:0	rx_to_adapter_counter	count bytes transfer from rx to adapter out	RO	0h

4.6.2.4.138 Register 144h -- MAIN_EXTERNAL_STATE

Address offset	Name	Description	Mode	Default
324.5:0	aux_main_external_state	AUX_MAIN external state machine register	RO	1h

4.6.2.4.139 Register 145h -- MAIN_EXTERNAL_COUNTER

Address offset	Name	Description	Mode	Default
325.4:0	aux_main_external_counter	count data enter from adapter	RO	0h

4.6.2.4.140 Register 146h -- MAIN_TX_MUX_COUNTER

Address offset	Name	Description	Mode	Default
326.4:0	aux_main_tx_mux_counter	count bytes forward to AUX_TX	RO	0h

4.6.2.4.141 Register 148h -- AUX_AFE_IN

Address offset	Name	Description	Mode	Default
328.0	afe_aux_data	Auxiliary data input from AFE	RO	0

4.6.2.4.142 Register 149h -- AUX_AFE_OUT

Address offset	Name	Description	Mode	Default
329.5	aux_host_aux_afe_rx_pd	drive the aux_afe_rx_pd output to the AFE when aux_host_afe_if_test_en (bit 0) is set	RW	0
329.4	aux_host_aux_afe_prech	drive the aux_afe_prech output to the AFE when aux_host_afe_if_test_en (bit 0) is set	RW	0
329.3	aux_host_aux_afe_tx_pd	drive the aux_afe_tx_pd output to the AFE when aux_host_afe_if_test_en (bit 0) is set	RW	0
329.2	aux_host_aux_afe_clk	drive the aux_afe_clk output to the AFE when aux_host_afe_if_test_en (bit 0) is set	RW	0
329.1	aux_host_aux_afe_data	drive the aux_afe_data output to the AFE when aux_host_afe_if_test_en (bit 0) is set	RW	0
329.0	aux_host_afe_if_test_en	TESTER mode enable. Give the TESTER direct interface to the AFE_AUX.	RW	0

4.6.2.4.143 Register 150h -- AUX_CHICKEN0 Extension of Tx transaction - 2 bits

Offset	Bit(s)	Field Name	Description	Type	Default Value
330	1:0	aux_host_tx_stop_extend	Extend AUX Tx stage before it change the direction to Rx stage.	R/W	0

4.6.2.5 Bank 6 -- MISC -- hpd, error counters, misc registers, configuration

Table 167 is a summary of the MISC registers without registers description. The detailed description of the register list is given in the following sections.

Table 167. 0xC00 MISC Register Summary

Register Number	Register Name	Section #
0	LS_RST	"Register 0h -- LS_RST -- ls_rst setting/resetting. Polarity: positive" on page 496
1	AUX_RST	"Register 1h -- AUX_RST -- AUX rest" on page 497
2	ERROR_IND	"Register 2h -- ERROR_IND -- Error indication from various blocks" on page 497
3	DP_MODE	"Register 3h -- DP_MODE -- Dp mode: tx=1, rx=0" on page 497
4	LANE_DATA_ENABLE	"Register 4h -- LANE_DATA_ENABLE -- Enable for lanes 0,1,2,3" on page 497
5	MISC_STATUS_NO_CLR	"Register 5h -- MISC_STATUS_NO_CLR -- 0: Status registers reset by read. 1: Status registers reset by write. Relevant regs: HPD detects" on page 497
6	LS_CLK_SEL	"Register 6h -- LS_CLK_SEL" on page 497
7	MISC_USR0	"Register 7h -- MISC_USR0" on page 497
8	MISC_COUNTER1_L	"Register 8h -- MISC_COUNTER1_L" on page 499
9	MISC_COUNTER1_H	"Register 9h -- MISC_COUNTER1_H" on page 499
10	MISC_COUNTER2_L	"Register Ah -- MISC_COUNTER2_L" on page 499
11	MISC_COUNTER2_H	"Register Bh -- MISC_COUNTER2_H" on page 499

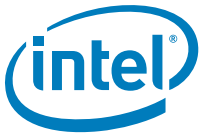


Table 167. 0xC00 MISC Register Summary

Register Number	Register Name	Section #
12	MISC_1USEC_FACTOR	"Register Ch -- MISC_1USEC_FACTOR" on page 499
13	REF_CLK_SEL	"Register Dh -- REF_CLK_SEL" on page 499
14	DWNSPRD_EN	"Register Eh -- DWNSPRD_EN" on page 499
15	TESTBUS_SEL	"Register Fh -- TESTBUS_SEL" on page 499
16	HPD_IRQ_DET_MIN_TIMER_LO	"Register 10h -- HPD_IRQ_DET_MIN_TIMER_LO -- hpd min timer for irq, 8 lsb" on page 500
17	HPD_IRQ_DET_MIN_TIMER_MD	"Register 11h -- HPD_IRQ_DET_MIN_TIMER_MD -- hpd min timer for irq, bits 15:8" on page 500
18	HPD_IRQ_DET_MIN_TIMER_HI	"Register 12h -- HPD_IRQ_DET_MIN_TIMER_HI -- hpd min timer for irq, bits 23:16" on page 500
19	HPD_IRQ_DET_MAX_TIMER_LO	"Register 13h -- HPD_IRQ_DET_MAX_TIMER_LO -- hpd max timer, bits 7:0" on page 500
20	HPD_IRQ_DET_MAX_TIMER_MD	"Register 14h -- HPD_IRQ_DET_MAX_TIMER_MD -- hpd max timer, bits 15:8" on page 500
21	HPD_IRQ_DET_MAX_TIMER_HI	"Register 15h -- HPD_IRQ_DET_MAX_TIMER_HI -- hpd max timer, bits 23:16" on page 500
22	HPD_UNPLGED_DET_MIN_TIMER_LO	"Register 16h -- HPD_UNPLGED_DET_MIN_TIMER_LO -- hpd unplugged timer, bits 7:0" on page 500
23	HPD_UNPLGED_DET_MIN_TIMER_MD	"Register 17h -- HPD_UNPLGED_DET_MIN_TIMER_MD -- hpd unplugged timer, bits 15:8" on page 500
24	HPD_UNPLGED_DET_MIN_TIMER_HI	"Register 18h -- HPD_UNPLGED_DET_MIN_TIMER_HI -- hpd unplugged timer, bits 23:16" on page 500
28	HPD_IRQ_DET	"Register 1Ch -- HPD_IRQ_DET -- hpd irq detection" on page 501
29	HPD_RE_PLUGGED_DET	"Register 1Dh -- HPD_RE_PLUGGED_DET -- hpd re-plugged" on page 501
30	HPD_GEN_TIMER_LO	"Register 1Eh -- HPD_GEN_TIMER_LO -- hpd generation timer bits 7:0" on page 501
31	HPD_GEN_TIMER_MD	"Register 1Fh -- HPD_GEN_TIMER_MD -- hpd generation timer bits 15:8" on page 501
32	HPD_GEN_TIMER_HI	"Register 20h -- HPD_GEN_TIMER_HI -- hpd generation timer bits 23:16" on page 501
33	HPD_GEN	"Register 21h -- HPD_GEN -- generate HPD" on page 501
34	HPD_BYPASS	"Register 22h -- HPD_BYPASS -- Bypass hpd in" on page 501
35	HPD_STATUS	"Register 23h -- HPD_STATUS -- Status of hpd (out)" on page 502
36	HPD_STABLE_TIMER_LO	"Register 24h -- HPD_STABLE_TIMER_LO -- Timer for stable hpd after bits 7:0" on page 502
37	HPD_STABLE_TIMER_MD	"Register 25h -- HPD_STABLE_TIMER_MD -- Hpd stable timer after unplugged, bits 15:8" on page 502
38	HPD_STABLE_TIMER_HI	"Register 26h -- HPD_STABLE_TIMER_HI -- Hpd stable timer after unplugged, bits 23:16" on page 502
39	HPD_FILTER_TIMER_LO	"Register 27h -- HPD_FILTER_TIMER_LO -- Hpd filter timer, bits 7:0" on page 502

Table 167. 0xC00 MISC Register Summary

Register Number	Register Name	Section #
40	HPD_FILTER_TIMER_MD	"Register 28h -- HPD_FILTER_TIMER_MD -- Hpd filter timer, bits 15:8" on page 502
41	HPD_FILTER_TIMER_HI	"Register 29h -- HPD_FILTER_TIMER_HI -- Hpd filter timer, bits 23:16" on page 502
42	HPD_STABLE_STATUS	"Register 2Ah -- HPD_STABLE_STATUS" on page 502
48	DP_IP_ADAPT_CONF_CHANGE_SET	"Register 30h -- DP_IP_ADAPT_CONF_CHANGE_SET -- Configuration data changed from ip to adapt" on page 503
49	DP_IP_ADAPT_CONF_DATA0	"Register 31h -- DP_IP_ADAPT_CONF_DATA0 -- Configuration data0" on page 503
50	DP_IP_ADAPT_CONF_DATA1	"Register 32h -- DP_IP_ADAPT_CONF_DATA1 -- Configuration data1 from ip to adapt" on page 503
51	DP_IP_ADAPT_CONF_DATA2	"Register 33h -- DP_IP_ADAPT_CONF_DATA2 -- Configuration data2 from ip to adapt" on page 503
52	DP_ADAPT_IP_CONF_CHANGED	"Register 34h -- DP_ADAPT_IP_CONF_CHANGED -- Configuration data had changed" on page 504
53	DP_ADAPT_IP_CONF_DATA0	"Register 35h -- DP_ADAPT_IP_CONF_DATA0 -- Adapt to ip configuration data0" on page 504
54	DP_ADAPT_IP_CONF_DATA1	"Register 36h -- DP_ADAPT_IP_CONF_DATA1 -- Adapt to ip configuration data1" on page 504
55	DP_ADAPT_IP_CONF_DATA2	"Register 37h -- DP_ADAPT_IP_CONF_DATA2 -- Adapt to ip configuration data2" on page 504
140	GP0	"Register 8Ch -- GP0" on page 504
141	GP1	"Register 8Dh -- GP1" on page 504
142	GP2	"Register 8Eh -- GP2" on page 504
143	GP3	"Register 8Fh -- GP3" on page 504
145	GP5	"Register 91h -- GP5" on page 505
146	GP6	"Register 92h -- GP6" on page 505
147	GP7	"Register 93h -- GP7" on page 505
148	GP8	"Register 94h -- GP8" on page 505
149	GP9	"Register 95h -- GP9" on page 505
150	GP10	"Register 96h -- GP10" on page 505
151	GP11	"Register 97h -- GP11" on page 505
152	GP12	"Register 98h -- GP12" on page 505
154	GP14	"Register 9Ah -- GP14" on page 505
155	GP15	"Register 9Bh -- GP15" on page 505

4.6.2.5.1 Register 0h -- LS_RST -- ls_rst setting/resetting. Polarity: positive

Address offset	Name	Description	Mode	Default
0.7:1	Reserved			
0.0	ls_rst_req		RW	1

4.6.2.5.2 Register 1h -- AUX_RST -- AUX rest

Address offset	Name	Description	Mode	Default
1.7:1	Reserved			
1.0	aux_rst_req	Aux rest	RW	0

4.6.2.5.3 Register 2h -- ERROR_IND -- Error indication from various blocks

Address offset	Name	Description	Mode	Default
2.7:2	Reserved			
2.1	error_frm		RO	
2.0	error_phy		RO	

4.6.2.5.4 Register 3h -- DP_MODE -- Dp mode: tx=1, rx=0

Address offset	Name	Description	Mode	Default
3.7:1	Reserved			
3.0	mi_dp_mode		RW	1

4.6.2.5.5 Register 4h -- LANE_DATA_ENABLE -- Enable for lanes 0,1,2,3

Address offset	Name	Description	Mode	Default
4.7:4	Reserved			
4.3	mi_lane_data_enable_3		RW	0
4.2	mi_lane_data_enable_2		RW	0
4.1	mi_lane_data_enable_1		RW	0
4.0	mi_lane_data_enable_0		RW	0

4.6.2.5.6 Register 5h -- MISC_STATUS_NO_CLR -- 0: Status registers reset by read. 1: Status registers reset by write. Relevant regs: HPD detects

Address offset	Name	Description	Mode	Default
5.7:1	Reserved			
5.0	mi_status_no_clr		RW	0

4.6.2.5.7 Register 6h -- LS_CLK_SEL

Address offset	Name	Description	Mode	Default
6.7:2	Reserved			
6.1:0	ls_clk_sel		RW	3h

4.6.2.5.8 Register 7h -- MISC_USR0

Address offset	Name	Description	Mode	Default
7.7:6	Reserved			
7.5	mi_adapt_ip_link_init_usr0		RO/RR/1C	
7.4:3	Reserved			
7.2	mi_adapt_ip_conf_changed_usr0		RO/RR/1C	
7.1	mi_hpd_irq_det_usr0		RO/RR/1C	
7.0	mi_hpd_unplugged_det		RO	

4.6.2.5.9 Register 8h -- MISC_COUNTER1_L

Address offset	Name	Description	Mode	Default
8.7:0	misc_counter1_lo		RO	

4.6.2.5.10 Register 9h -- MISC_COUNTER1_H

Address offset	Name	Description	Mode	Default
9.7:0	misc_counter1_hi		RO/1C	

4.6.2.5.11 Register Ah -- MISC_COUNTER2_L

Address offset	Name	Description	Mode	Default
10.7:0	misc_counter2_lo		RO	

4.6.2.5.12 Register Bh -- MISC_COUNTER2_H

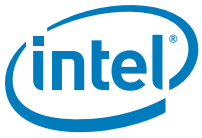
Address offset	Name	Description	Mode	Default
11.7:0	misc_counter2_hi		RO/1C	

4.6.2.5.13 Register Ch -- MISC_1USEC_FACTOR

Address offset	Name	Description	Mode	Default
12.7:0	mi_1usec_factor		RW	24

4.6.2.5.14 Register Dh -- REF_CLK_SEL

Address offset	Name	Description	Mode	Default
13.7:1	Reserved			
13.0	mi_ref_clk_sel	When '1', pll_ref_clk to AFE is from txaux_clk_out from AFE, when '0', pll_ref_clk to AFE is from dp_out_pll_ref_clk	RW	0h



4.6.2.5.15 Register Eh -- DWNSPRD_EN

Address offset	Name	Description	Mode	Default
14.7:1	Reserved			
14.0	dp_out_ip_adapt_dwnsprd_en	Down spread enable.	RW	0h

4.6.2.5.16 Register Fh -- TESTBUS_SEL

Address offset	Name	Description	Mode	Default
15.7:3	Reserved			
15.2:0	testbus_sel	test bus select 0h = no selection 1h = Phy testbus 2h = Framer testbus 3h = aux testbus 4h = analog IF testbus	RW	0h

4.6.2.5.17 Register 10h -- HPD_IRQ_DET_MIN_TIMER_LO -- hpd min timer for irq, 8 lsb

Address offset	Name	Description	Mode	Default
16.7:0	mi_hpd_irq_det_min_timer_lo		RW	69h

4.6.2.5.18 Register 11h -- HPD_IRQ_DET_MIN_TIMER_MD -- hpd min timer for irq, bits 15:8

Address offset	Name	Description	Mode	Default
17.7:0	mi_hpd_irq_det_min_timer_md		RW	18h

4.6.2.5.19 Register 12h -- HPD_IRQ_DET_MIN_TIMER_HI -- hpd min timer for irq, bits 23:16

Address offset	Name	Description	Mode	Default
18.7:0	mi_hpd_irq_det_min_timer_hi		RW	0h

4.6.2.5.20 Register 13h -- HPD_IRQ_DET_MAX_TIMER_LO -- hpd max timer, bits 7:0

Address offset	Name	Description	Mode	Default
19.7:0	mi_hpd_irq_det_max_timer_lo		RW	4Fh

4.6.2.5.21 Register 14h -- HPD_IRQ_DET_MAX_TIMER_MD -- hpd max timer, bits 15:8

Address offset	Name	Description	Mode	Default
20.7:0	mi_hpd_irq_det_max_timer_md		RW	C3h

4.6.2.5.22 Register 15h -- HPD_IRQ_DET_MAX_TIMER_HI -- hpd max timer, bits 23:16

Address offset	Name	Description	Mode	Default
21.7:0	mi_hpd_irq_det_max_timer_hi		RW	0h

4.6.2.5.23 Register 16h -- HPD_UNPLGED_DET_MIN_TIMER_LO -- hpd unplugged timer, bits 7:0

Address offset	Name	Description	Mode	Default
22.7:0	mi_hpd_unplged_det_min_timer_lo		RW	4Fh

4.6.2.5.24 Register 17h -- HPD_UNPLGED_DET_MIN_TIMER_MD -- hpd unplugged timer, bits 15:8

Address offset	Name	Description	Mode	Default
23.7:0	mi_hpd_unplged_det_min_timer_md		RW	C3h

4.6.2.5.25 Register 18h -- HPD_UNPLGED_DET_MIN_TIMER_HI -- hpd unplugged timer, bits 23:16

Address offset	Name	Description	Mode	Default
24.7:0	mi_hpd_unplged_det_min_timer_hi		RW	0h

4.6.2.5.26 Register 1Ch -- HPD_IRQ_DET -- hpd irq detection

Address offset	Name	Description	Mode	Default
28.7:1	Reserved			
28.0	mi_hpd_irq_det_bit	Irq detect. Clear on Write '0. Write '1' is not allowed.	RO/RR/1C	0

4.6.2.5.27 Register 1Dh -- HPD_RE_PLUGGED_DET -- hpd re-plugged

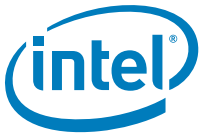
Address offset	Name	Description	Mode	Default
29.7:1	Reserved			
29.0	hpd_re_plged_det_bit	hpd unplugged detect. Clear on read or by Write '0. Write '1' is not allowed.	RO/RR/1C	0

4.6.2.5.28 Register 1Eh -- HPD_GEN_TIMER_LO -- hpd generation timer bits 7:0

Address offset	Name	Description	Mode	Default
30.7:0	mi_hpd_gen_timer_lo		RW	3Eh

4.6.2.5.29 Register 1Fh -- HPD_GEN_TIMER_MD -- hpd generation timer bits 15:8

Address offset	Name	Description	Mode	Default
31.7:0	mi_hpd_gen_timer_md		RW	49h



4.6.2.5.30 Register 20h -- HPD_GEN_TIMER_HI -- hpd generation timer bits 23:16

Address offset	Name	Description	Mode	Default
32.7:0	mi_hpd_gen_timer_hi		RW	0h

4.6.2.5.31 Register 21h -- HPD_GEN -- generate HPD

Address offset	Name	Description	Mode	Default
33.7:1	Reserved			
33.0	mi_hpd_gen		RW/SC	0

4.6.2.5.32 Register 22h -- HPD_BYPASS -- Bypass hpd in

Address offset	Name	Description	Mode	Default
34.7:1	Reserved			
34.0	mi_hpd_bypass		RW	0

4.6.2.5.33 Register 23h -- HPD_STATUS -- Status of hpd (out)

Address offset	Name	Description	Mode	Default
35.7:1	Reserved			
35.0	dp_ip_adapt_hpd_sync		RO	

4.6.2.5.34 Register 24h -- HPD_STABLE_TIMER_LO -- Timer for stable hpd after bits 7:0

Address offset	Name	Description	Mode	Default
36.7:0	mi_hpd_stable_timer_lo	Cycles to identify stable hpd, from rising hpd after is was unplugged. '0' is illegal.	RW	1h

4.6.2.5.35 Register 25h -- HPD_STABLE_TIMER_MD -- Hpd stable timer after unplugged, bits 15:8

Address offset	Name	Description	Mode	Default
37.7:0	mi_hpd_stable_timer_md		RW	0h

4.6.2.5.36 Register 26h -- HPD_STABLE_TIMER_HI -- Hpd stable timer after unplugged, bits 23:16

Address offset	Name	Description	Mode	Default
38.7:0	mi_hpd_stable_timer_hi		RW	0h

4.6.2.5.37 Register 27h -- HPD_FILTER_TIMER_LO -- Hpd filter timer, bits 7:0

Address offset	Name	Description	Mode	Default
39.7:0	mi_hpd_filter_timer_lo		RW	11h

4.6.2.5.38 Register 28h -- HPD_FILTER_TIMER_MD -- Hpd filter timer, bits 15:8

Address offset	Name	Description	Mode	Default
40.7:0	mi_hpd_filter_timer_md		RW	7Ah

4.6.2.5.39 Register 29h -- HPD_FILTER_TIMER_HI -- Hpd filter timer, bits 23:16

Address offset	Name	Description	Mode	Default
41.7:0	mi_hpd_filter_timer_hi		RW	0h

4.6.2.5.40 Register 2Ah -- HPD_STABLE_STATUS

Address offset	Name	Description	Mode	Default
42.7:1	Reserved			
42.0	mi_hpd_stable		RO	0h

4.6.2.5.41 Register 30h -- DP_IP_ADAPT_CONF_CHANGE_SET -- Configuration data changed from ip to adapt

Address offset	Name	Description	Mode	Default
48.7:1	Reserved			
48.0	mi_conf_change_set		RW/SC	0h

4.6.2.5.42 Register 31h -- DP_IP_ADAPT_CONF_DATA0 -- Configuration data0

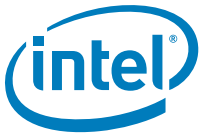
Address offset	Name	Description	Mode	Default
49.7:0	mi_ip_adapt_conf_data0		RW	0h

4.6.2.5.43 Register 32h -- DP_IP_ADAPT_CONF_DATA1 -- Configuration data1 from ip to adapt

Address offset	Name	Description	Mode	Default
50.7:0	mi_ip_adapt_conf_data1		RW	0h

4.6.2.5.44 Register 33h -- DP_IP_ADAPT_CONF_DATA2 -- Configuration data2 from ip to adapt

Address offset	Name	Description	Mode	Default
51.7:0	mi_ip_adapt_conf_data2		RW	0h



4.6.2.5.45 Register 34h -- DP_ADAPT_IP_CONF_CHANGED -- Configuration data had changed

Address offset	Name	Description	Mode	Default
52.7:1	Reserved			
52.0	mi_adapt_ip_conf_changed	Clear by reas or by write '0'. Write '1' is not allowed.	RO/RR/1C	0h

4.6.2.5.46 Register 35h -- DP_ADAPT_IP_CONF_DATA0 -- Adapt to ip configuration data0

Address offset	Name	Description	Mode	Default
53.7:0	mi_adapt_ip_conf_data0		RO	

4.6.2.5.47 Register 36h -- DP_ADAPT_IP_CONF_DATA1 -- Adapt to ip configuration data1

Address offset	Name	Description	Mode	Default
54.7:0	mi_adapt_ip_conf_data1		RO	

4.6.2.5.48 Register 37h -- DP_ADAPT_IP_CONF_DATA2 -- Adapt to ip configuration data2

Address offset	Name	Description	Mode	Default
55.7:0	mi_adapt_ip_conf_data2		RO	

4.6.2.5.49 Register 8Ch -- GP0

Address offset	Name	Description	Mode	Default
140.7:0	mi_gp0		RW	0h

4.6.2.5.50 Register 8Dh -- GP1

Address offset	Name	Description	Mode	Default
141.7:0	mi_gp1		RW	0h

4.6.2.5.51 Register 8Eh -- GP2

Address offset	Name	Description	Mode	Default
142.7:0	mi_gp2		RW	0h

4.6.2.5.52 Register 8Fh -- GP3

Address offset	Name	Description	Mode	Default
143.7:0	mi_gp3		RW	0h

4.6.2.5.53 Register 91h -- GP5

Address offset	Name	Description	Mode	Default
145.7:0	mi_gp5		RW	0h

4.6.2.5.54 Register 92h -- GP6

Address offset	Name	Description	Mode	Default
146.7:0	mi_gp6		RW	0h

4.6.2.5.55 Register 93h -- GP7

Address offset	Name	Description	Mode	Default
147.7:0	mi_gp7		RW	0h

4.6.2.5.56 Register 94h -- GP8

Address offset	Name	Description	Mode	Default
148.7:0	mi_gp8		RW	0h

4.6.2.5.57 Register 95h -- GP9

Address offset	Name	Description	Mode	Default
149.7:0	mi_gp9		RW	0h

4.6.2.5.58 Register 96h -- GP10

Address offset	Name	Description	Mode	Default
150.7:0	mi_gp10		RW	0h

4.6.2.5.59 Register 97h -- GP11

Address offset	Name	Description	Mode	Default
151.7:0	mi_gp11		RW	0h

4.6.2.5.60 Register 98h -- GP12

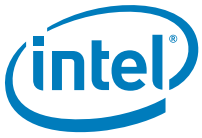
Address offset	Name	Description	Mode	Default
152.7:0	mi_gp12		RW	0h

4.6.2.5.61 Register 9Ah -- GP14

Address offset	Name	Description	Mode	Default
154.7:0	mi_gp14		RW	0h

4.6.2.5.62 Register 9Bh -- GP15

Address offset	Name	Description	Mode	Default
155.7:0	mi_gp15		RW	0h



4.6.2.6 Bank 7 -- Analog_if

Table 168 provides a summary of the Analog Interface registers without registers description. The detailed description of the register list is given in the following sections.

Table 168. 0xE00 Analog Interface Register Summary

Register Number	Register Name	Section #
128	SHIFT_PATTERN_IN0	"Register 80h -- SHIFT_PATTERN_IN0" on page 507
129	SHIFT_PATTERN_IN1	"Register 81h -- SHIFT_PATTERN_IN1" on page 507
130	SHIFT_PATTERN_IN2	"Register 82h -- SHIFT_PATTERN_IN2" on page 507
131	SHIFT_PATTERN_IN3	"Register 83h -- SHIFT_PATTERN_IN3" on page 507
132	SHIFT_PATTERN_IN4	"Register 84h -- SHIFT_PATTERN_IN4" on page 507
133	SHIFT_PATTERN_IN5	"Register 85h -- SHIFT_PATTERN_IN5" on page 507
134	SHIFT_PATTERN_IN6	"Register 86h -- SHIFT_PATTERN_IN6" on page 507
135	SHIFT_PATTERN_IN7	"Register 87h -- SHIFT_PATTERN_IN7" on page 507
136	SHIFT_PATTERN_IN8	"Register 88h -- SHIFT_PATTERN_IN8" on page 507
137	SHIFT_PATTERN_IN9	"Register 89h -- SHIFT_PATTERN_IN9" on page 507
141	TX_AN_IF_DATA_SEL	"Register 8Dh -- TX_AN_IF_DATA_SEL" on page 508

4.6.2.6.1 Register 80h -- SHIFT_PATTERN_IN0

Address offset	Name	Description	Mode	Default
128.7:0	an_shift_pattern0	80bit pattern. (MSb of SHIFT_PATTERN_IN0 is the first on the wire)	RW	0h

4.6.2.6.2 Register 81h -- SHIFT_PATTERN_IN1

Address offset	Name	Description	Mode	Default
129.7:0	an_shift_pattern1		RW	0h

4.6.2.6.3 Register 82h -- SHIFT_PATTERN_IN2

Address offset	Name	Description	Mode	Default
130.7:0	an_shift_pattern2		RW	

4.6.2.6.4 Register 83h -- SHIFT_PATTERN_IN3

Address offset	Name	Description	Mode	Default
131.7:0	an_shift_pattern3		RW	

4.6.2.6.5 Register 84h -- SHIFT_PATTERN_IN4

Address offset	Name	Description	Mode	Default
132.7:0	an_shift_pattern4		RW	

4.6.2.6.6 Register 85h -- SHIFT_PATTERN_IN5

Address offset	Name	Description	Mode	Default
133.7:0	an_shift_pattern5		RW	

4.6.2.6.7 Register 86h -- SHIFT_PATTERN_IN6

Address offset	Name	Description	Mode	Default
134.7:0	an_shift_pattern6		RW	

4.6.2.6.8 Register 87h -- SHIFT_PATTERN_IN7

Address offset	Name	Description	Mode	Default
135.7:0	an_shift_pattern7		RW	

4.6.2.6.9 Register 88h -- SHIFT_PATTERN_IN8

Address offset	Name	Description	Mode	Default
136.7:0	an_shift_pattern8		RW	

4.6.2.6.10 Register 89h -- SHIFT_PATTERN_IN9

Address offset	Name	Description	Mode	Default
137.7:0	an_shift_pattern9		RW	

4.6.2.6.11 Register 8Dh -- TX_AN_IF_DATA_SEL

Address offset	Name	Description	Mode	Default
141.7:3	Reserved			
141.2:0	an_tx_data_sel	000 = phy	RW	000

4.6.2.7 Bank 11 Phy Digital Lane

Table 169. 0x1600 Phy Digital Lane Registers Summary

Register Number	Register Name	Section #
0, 128, 256, 384	TX_SW_INV	See section 4.6.2.7.1
1, 129, 257, 385	TX_SW_PRE	See section 4.6.2.7.2
2, 130, 258, 386	TX_SW_POST	See section 4.6.2.7.3
114	Swizzel_1020_EN	See section 4.6.2.7.4
122	CM_TX_RESTUNE_SET	See section 4.6.2.7.5
123	CM_MISC_CTRL	See section 4.6.2.7.6
124	CM_CAL_CTRL	See section 4.6.2.7.7
125	DP_SPEED	See section 4.6.2.7.8
126	TX_EN	See section 4.6.2.7.8
127	TX_SYNC_CTRL	See section 4.6.2.7.10
359	Allow_RTL_DPPLL_CTRL	See section 4.6.2.7.11
366	CM_DPPLL_RST_B	See section 4.6.2.7.12
367	CM_DPPLL_F_H	See section 4.6.2.7.13
368	CM_DPPLL_F_M	See section 4.6.2.7.14
369	CM_DPPLL_F_L	See section 4.6.2.7.15
380	CM_DPPLL_LOOP_CTRL	See section 4.6.2.7.16
381	CM_DPPLL_POSTDIVSEL	See section 4.6.2.7.17
382	CM_DPPLL_CP_RES_SEL	See section 4.6.2.7.18
383	CM_DPPLL_CTERL	See section 4.6.2.7.19

4.6.2.7.1 TX_SW_INV - Lane 0/1/2/3 TX CID swing control

Offset	Bit(s)	Field Name	Description	Type	Default Value
0	7	reserved	Reserved	RO	0x0
128 256 384	6:0	tx_sw_inv	TX CID swing control	RW	0x0

4.6.2.7.2 TX_SW_PRE - Lane 0/1/2/3 TX 1st pre-cursor swing control

Offset	Bit(s)	Field Name	Description	Type	Default Value
1	7:3	reserved	Reserved	RO	0x0
129 257 385	2:0	tx_sw_pre	TX 1st pre-cursor swing control	RW	0x0

4.6.2.7.3 TX_SW_POST - Lane 0/1/2/3 TX 1st post-cursor swing control

Offset	Bit(s)	Field Name	Description	Type	Default Value

2	7:4	reserved	Reserved	RO	0x0
130 258 386	3:0	tx_sw_post	TX 1st post-cursor swing control	RW	0x0

4.6.2.7.4 Swizzle_1020_EN - Swizzle data towards Phy

Offset	Bit(s)	Field Name	Description	Type	Default Value
114	7:4	Swizzle 20_en	Swizzle each 20 bits within themselves. Bit per lane	RW	0x0
	3:0	Swizzle_10_en	Swizzle each 10 bits within themselves. Bit per lane	RW	0x0

4.6.2.7.5 CM_TX_RESTUNE_SET - Tx termination resistor settings in bypass mode

Offset	Bit(s)	Field Name	Description	Type	Default Value
122	7:3	reserved	Reserved	RO	0x0
	2:0	cm_restune_set	TX termination resistor settings in bypass mode	RW	0x0

4.6.2.7.6 CM_MISC_CTRL- Misc. Phy Common control

Offset	Bit(s)	Field Name	Description	Type	Default Value
123	7:3	reserved	reserved	RO	0x0
	2	cm_dppll_fix_coarse	Force VCO coarse voltage to constant	RW	0x0
	1	cm_dppll_cal_bypass	Bypass PLL VCO calibration	RW	0x0
	0	cm_restune_bypass	Bypass TX termination calibration settings	RW	0x0

4.6.2.7.7 CM_CAL_CTRL- Misc. Phy Common control 2

Offset	Bit(s)	Field Name	Description	Type	Default Value
124	7:3	reserved	reserved	RO	0x0
	2	cm_tx_cal_rdy	TX termination calibration ready indicator	RW	0x1
	1	cm_tx_cal_start	Start TX termination calibration	RW	0x0
	0	cm_en_b	PHY common enable. Active low.	RW	0x0

4.6.2.7.8 DP_SPEED - Misc. Phy Common control 2

Offset	Bit(s)	Field Name	Description	Type	Default Value
124	7:2	reserved	reserved	RO	0x0
	1:0	dp_speed	0: 1.62 1: 2.7 2: 5.4	RW	0x0

4.6.2.7.9 TX_EN - Tx Enable

Offset	Bit(s)	Field Name	Description	Type	Default Value
126	7:4	reserved	Reserved	RW	0x0
	3:0	tx_en	Tx Lane Enable	RW	0x0

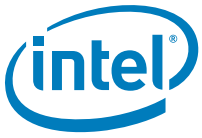
4.6.2.7.10 TX_SYNC_CTRL- Tx Sync control

Offset	Bit(s)	Field Name	Description	Type	Default Value
127	7	tx_sync_h	Parallel data sync. Strobe signal.	RW	0x0
	6:4	reserved	Reserved	RW	0x0
	3:0	tx_sync_en	Enable for parallel data sync. Per lane.	RW	0x0

4.6.2.7.11 Allow_RTL_DPPLL_CTRL - Switch control over PLL interface

Offset	Bit(s)	Field Name	Description	Type	Default Value

359	7	allow_rtl_dppll_ctrl[7]	cm_dppll_strobe	RW	0x0
	6	Reserved	reserved	RO	0x0
	5	allow_rtl_dppll_ctrl[5]	cm_dppll_cpsel	RW	0x0
	4	allow_rtl_dppll_ctrl[4]	cm_dppll_postdivsel	RW	0x0
	3	allow_rtl_dppll_ctrl[3]	cm_dppll_f	RW	0x0
	2	allow_rtl_dppll_ctrl[2]	cm_dppll_i	RW	0x0
	1	allow_rtl_dppll_ctrl[1]	cm_dppll_n	RW	0x0
	0	allow_rtl_dppll_ctrl[0]	cm_dppll_m	RW	0x0



4.6.2.7.12 CM_DPPLL_RST_B - PLL reset

Offset	Bit(s)	Field Name	Description	Type	Default Value
366	7:1	Reserved	reserved	RO	0x0
	0	cm_dppll_rst_b	PLL reset	RW	0x0

4.6.2.7.13 CM_DPPLL_F_H - PLL fractional multiplication factor, high

Offset	Bit(s)	Field Name	Description	Type	Default Value
367	7:2	reserved	reserved	RO	0x0
	1:0	cm_dppll_f[17:16]	PLL fractional multiplication factor	RW	0x0

4.6.2.7.14 CM_DPPLL_F_M - PLL fractional multiplication factor, med

Offset	Bit(s)	Field Name	Description	Type	Default Value
368	7:0	cm_dppll_f[15:8]	PLL fractional multiplication factor	RW	0x0

4.6.2.7.15 CM_DPPLL_F_L - PLL fractional multiplication factor, low

Offset	Bit(s)	Field Name	Description	Type	Default Value
369	7:0	cm_dppll_f[7:0]	PLL fractional multiplication factor	RW	0x0

4.6.2.7.16 CM_DPPLL_LOOP_CTRL - PLL third loop control

Offset	Bit(s)	Field Name	Description	Type	Default Value
380	7:2	reserved	Reserved	RO	0x0
	1	cm_dppll_loop_bw	PLL 3rd Loop bandwidth control: 1'b0 - bandwidth < 30KHz 1'b1 - bandwidth > 120KHz	RW	0x0
	0	cm_dppll_loop_en	PLL 3rd Loop enable	RW	0x0

4.6.2.7.17 CM_DPPLL_POSTDIVSEL - PLL post divider settings

Offset	Bit(s)	Field Name	Description	Type	Default Value
381	7:5	reserved	Reserved	RO	0x0
	4:0	cm_dppll_postdivsel	PLL Post-Divider settings	RW	0x0

4.6.2.7.18 CM_DPPLL_CP_RES_SEL - PLL Resistor Select Control

Offset	Bit(s)	Field Name	Description	Type	Default Value
382	7:5	reserved	Reserved	RO	0x0
	4:2	cm_dppll_cpsel	PLL Charge-Pump current control	RW	0x0
	1:0	cm_dppll_ressel	PLL loop-filter resistor control	RW	0x0

4.6.2.7.19 CM_DPPLL_CTRL - PLL Misc Control

Offset	Bit(s)	Field Name	Description	Type	Default Value
383	7	cm|_pll_lock	PLL lock indication	RO	0x0
	6:4	reserved	Reserved	RO	0x0
	3	cm_dppll_force_lock	Force the PLL to indicate cm_dppll_lock	RW	0x0
	2	cm_dppll_strobe	Strobe for PLL parameters update	RW	0x0
	1	cm_dppll_cal_start	Start PLL VCO calibration	RW	0x0
	0	cm_dppll_en_b	PLL enable. Active low	RW	0x0

4.7 xHCI Memory Mapped Address Space Registers

4.7.1 Host Controller Capability Registers

Table 170. CAPLENGTH - Capability Registers Length

Address Offset:0h
Default Value:80h
Access: RW/L;
Size:8 bits
This register is modified and maintained by BIOS

Bit	Access	Default Value	RST/PWR	Description
7:0	RW/L	80h	USB	Capability Registers Length (CAPLENGTH):

Table 171. HCIVERSION - Host Controller Interface Version Number

Address Offset:2-3h
Default Value:0100h
Access: RO;
Size:16 bits
This register is modified and maintained by BIOS

Bit	Access	Default Value	RST/PWR	Description
15:0	RO	0100h	USB	Host Controller Interface Version Number (HCIVERSION):

Table 172. HCSPARAMS1 - Structural Parameters 1

Address Offset:4-7h
Default Value:04000840h
Access: RW/L;
Size:32 bits
This register is modified and maintained by BIOS

Bit	Access	Default Value	RST/PWR	Description
31:24	RW/L	MaxPorts	USB	Number of Ports (MaxPorts): The value in this field reflects the highest numbered port in the controller, not the actual count of the number of ports. This allows for gaps in the port numbering, between USB2 and USB3 protocol capabilities.
23:19	RW/L	0h	USB	Reserved
18:8	RW/L	MaxInts	USB	Number of Interrupters (MaxInt):
7:0	RW/L	MaxSlots	USB	Number of Device Slots (MaxSlots):

Table 173. HCSPARAMS2 - Structural Parameters 2

Address Offset:8-Bh
Default Value:14200054h
Access: RW/L;
Size:32 bits
This register is modified and maintained by BIOS

Bit	Access	Default Value	RST/PWR	Description
31:27	RW/L	Ceiling (MaxSlots/2) +2 Bits4:0	USB	Max Scratchpad Buffers Lo (MaxScratchpadBufs):
26	RW/L	1h	USB	Scratchpad Restore (SPR):
25:21	RW/L	Ceiling (MaxSlots/2) +2 Bits9:5	USB	Max Scratchpad Buffers Hi (MaxScratchpadBufs):
20:8	RW/L	0h	USB	Reserved
7:4	RW/L	5h	USB	Event Ring Segment Table Max (ERSTMax):
3:0	RW/L	4h	USB	Isochronous Scheduling Threshold (IST):

Table 174. HCSPARAMS3 - Structural Parameters 3

Address Offset:C-Fh
Default Value:00040001h

Access: RW/L;
Size:32 bits
This register is modified and maintained by BIOS

Bit	Access	Default Value	RST/PWR	Description
31:16	RW/L	4h	USB	U2 Device Exit Latency (U2DEL):
15:8	RW/L	0h	USB	Reserved
7:0	RW/L	1h	USB	U1 Device Exit Latency (U1DEL):

Table 175. HCCPARAMS - Capability Parameters

Address Offset:10-13h
Default Value:200077C1h
Access: RW/L;
Size:32 bits
This register is modified and maintained by BIOS

Bit	Access	Default Value	RST/PWR	Description
31:16	RW/L	2000h/ 2008h*	USB	xHCI Extended Capabilities Pointer (xECP): The Default value should be 2008h if NumUSB2 = 0
15:12	RW/L	7h	USB	Maximum Primary Stream Array Size (MaxPSASize):
11	RW/L	0b	USB	Contiguous Frame ID Capability (CFC)
10	RW/L	1b	USB	Stopped EDLTA Capability (SEC).
9	RW/L	1b	USB	Stopped - Short Packet Capability (SPC).
8	RW/L	1h	USB	Parse All Event Data (PAE)
7	RW/L	1h	USB	No Secondary SID Support (NSS):
6	RW/L	1h	USB	Latency Tolerance Messaging Capability (LTC):
5	RW/L	0h	USB	Light HC Reset Capability (LHRC):
4	RW/L	0h	USB	Port Indicators (PIND):
3	RW/L	0h	USB	Port Power Control (PPC):
2	RW/L	0h	USB	Context Size (CSZ):
1	RW/L	0h	USB	BW Negotiation Capability (BNC):
0	RW/L	1h	USB	64-bit Addressing Capability (AC64):

Table 176. DBOFF - Doorbell Offset

Address Offset:14-17h
Default Value:00003000h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:2	RO	C00h	USB	Doorbell Array Offset (DBAO):
1:0	RO	0h	USB	Reserved

Table 177. RTSOFF - Runtime Register Space Offset

Address Offset:18-1Bh
Default Value:00002000h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:5	RO	100h	USB	Runtime Register Space Offset (RTRSO):
4:0	RO	0h	USB	Reserved

Table 178. HCCPARAMS2 - Capability Parameters2

Address Offset:1C-1Fh
Default Value:0000002Ch
Access: RW/L;
Size:32 bits
This register is modified and maintained by BIOS

Bit	Access	Default Value	RST/PWR	Description
31:7	RO	0h	USB	Reserved

Bit	Access	Default Value	RST/PWR	Description
	RW/L	0b	USB	Extended TBC Capability (ETC) - RO. This bit indicates if the TBC field in an Isoch TRB supports Burst Counts greater than 4. When this bit is 1, the Isoch TRB TD Size/ TBC field presents the TBC value, and the TBC/RsvdZ field is RsvdZ. When this bit is 0, the TD Size/TCB field presents the TD Size value, and the TBC/RsvdZ presents the TBC value. This capability shall be enabled only of LEC = 1.
5	RW/L	1b	USB	Configuration Information Capability (CIC) - RO. This bit indicates if the xHC supports extended Configuration Information. When this bit is 1, the Configuration Value, Interface Number, and Alternate Setting fields in the Input Control Context are supported. When this bit is 0, the extended Input Control Context fields are not supported. Refer to section 6.2.5.1 for more information.
4	RW/L	0b	USB	Large ESIT Payload Capability (LEC) - RO. This bit indicates whether the xHC supports ESIT Payloads greater than 48K bytes. When this bit is '1', ESIT Payloads greater than 48K bytes are supported. When this bit is '0', ESIT Payloads greater than 48K bytes are not supported. Refer to section 6.2.3.8 for more information.
3	RW/L	1b	USB	Compliance Transition Capability (CTC) - RO. This bit indicates whether the xHC USB3 Root Hub ports support the Compliance Transition Enabled (CTE) flag. When this bit is '1', USB3 Root Hub port state machine transitions to the Compliance substate shall be explicitly enabled software. When this bit is '0', USB3 Root Hub port state machine transitions to the Compliance substate are automatically enabled. Refer to section 4.19.1.2.4.1 for more information.
2	RW/L	1b	USB	Force Save Context Capability (FSC) - RO. This bit indicates whether the xHC supports the Force Save Context Capability. When this bit is '1', the Save State operation shall save any cached Slot, Endpoint, Stream or other Context information to memory. Refer to Implementation Note "FSC and Context handling by Save and Restore", and sections 4.23.2 and 5.4.1 for more information.
1	RW/L	0b	USB	Configure Endpoint Command Max Exit Latency Too Large Capability (CMC) - RO. This bit indicates whether a Configure Endpoint Command is capable of generating a Max Exit Latency Too Large Capability Error. When this bit is '1', a Max Exit Latency Too Large Capability Error may be returned by a Configure Endpoint Command. When this bit is '0', a Max Exit Latency Too Large Capability Error shall not be returned by a Configure Endpoint Command. This capability is enabled by the CME flag in the USBCMD register. Refer to sections 4.23.5.2 and 5.4.1 for more information.
0	RW/L	0b	USB	U3 Entry Capability (U3C) - RO. This bit indicates whether the xHC Root Hub ports support port Suspend Complete notification. When this bit is '1', PLC shall be asserted on any transition of PLS to the U3 State. Refer to section 4.15.1 for more information.

4.7.2 Host Controller Operational Registers

Table 179. USBCMD - USB Command

Address Offset:80-83h
Default Value:00000000h
Access: RW; RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:15	RO	0h	USB	Reserved

Bit	Access	Default Value	RST/PWR	Description
14	RW	0b	USB	Extended TCB Enable (ETE). This flag indicates that the host controller implementation is enabled to support Transfer Burst Count values greater than 4 in Isoch TDs. This bit may be set only if ETC = 1.
13:12	RO	0h	USB	Reserved
11	RW	0h	USB	Enable U3 MFINDEX Stop (EU3S):
10	RW	0h	USB	Enable Wrap Event (EWE):
9	RW	0h	USB	Controller Restore State (CRS):
8	RW	0h	USB	Controller Save State (CSS):
7	RW	0h	USB	Light Host Controller Reset (LHCRST):
6:4	RO	0h	USB	Reserved
3	RW	0h	USB	Host System Error Enable (HSEE):
2	RW	0h	USB	Interrupter Enable (INTE):
1	RW	0h	USB	Host Controller Reset (HCRST):
0	RW	0h	USB	Run/Stop (RS):

Table 180. USBSTS - USB Status

Address Offset:84-87h
Default Value:00000001h
Access: RO; RW1C;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:13	RO	0h	USB	Rsvd3 (Rsvd3):
12	RO	0h	USB	Host Controller Error (HCE): HC does no set this bit.
11	RO	0h	USB	Controller Not Ready (CNR): HC does not set this bit
10	RW1C	0h	USB	Save/Restore Error (SRE):
9	RO	0h	USB	Restore State Status (RSS):
8	RO	0h	USB	Save State Status (SSS):
7:5	RO	0h	USB	Reserved
4	RW1C	0h	USB	Port Change Detect (PCD):
3	RW1C	0h	USB	Event Interrupt (EINT):
2	RW1C	0h	USB	Host System Error (HSE):
1	RO	0h	USB	Reserved
0	RO	1h	USB	HCHalted (HCH):

Table 181. PAGESIZE - Page Size

Address Offset:88-8Bh
Default Value:00000001h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	0h	USB	Reserved
15:0	RO	1h	USB	Page Size (PAGESIZE):

Table 182. DNCTRL - Device Notification Control

Address Offset:94-97h
Default Value:00000000h
Access: RO; RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	0h	USB	Reserved
15:0	RW	0h	USB	Notification Enable (N0_N15):

Table 183. CRCR_LO - Command Ring Low

Address Offset:98-9Bh
Default Value:00000000h
Access: RW; RO;

Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:6	RW	0h	USB	Command Ring Pointer (CRP):
5:4	RO	0h	USB	Reserved
3	RO	0h	USB	Command Ring Running (CRR):
2	RW1S	0h	USB	Command Abort (CA):
1	RW1S	0h	USB	Command Stop (CS):
0	RW	0h	USB	Ring Cycle State (RCS):

Table 184. CRCR_HI - Command Ring High

Address Offset:9C-9Fh
Default Value:00000000h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	0h	USB	Command Ring Pointer (CRP):

Table 185. DCBAAP_LO - Device Context Base Address Array Pointer Low

Address Offset:B0-B3h
Default Value:00000000h
Access: RW; RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:6	RW	0h	USB	Device Context Base Address Array Pointer (DCBAAP):
5:0	RO	0h	USB	Reserved

Table 186. DCBAAP_HI - Device Context Base Address Array Pointer High

Address Offset:B4-B7h
Default Value:00000000h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	0h	USB	Device Context Base Address Array Pointer (DCBAAP):

Table 187. CONFIG - Configure

Address Offset:B8-BBh
Default Value:00000000h
Access: RO; RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:8	RO	0h	USB	Reserved
7:0	RW	0h	USB	Max Device Slots Enabled (MaxSlotsEn):

Table 188. PORTSCXUSB2 - Port X Status and Control USB2

Address Offset: Port 1: 480-483h; repeated for each additional USB2 port as described below.
Default Value:000002A0h
Access: RO; RWS; RW;
Size:32 bits
There are 2 USB2 PORTSC registers at offsets :
480h, 490h

Bit	Access	Default Value	RST/PWR	Description
31	RW1S	0h	USB	Warm Port Reset (WPR):
30	RO	0h	USB	Device Removable (DR):
29:28	RO	0h	USB	Reserved

Bit	Access	Default Value	RST/PWR	Description
27	RWS	0h	USB	Wake on Over-current Enable (WOE):
26	RWS	0h	USB	Wake on Disconnect Enable (WDE):
25	RWS	0h	USB	Wake on Connect Enable (WCE):
24	RO	0h	USB	Cold Attach Status (CAS):
23	RW1CS	0h	USB	Port Config Error Change (CEC):
22	RW1CS	0h	USB	Port Link State Change (PLC):
21	RW1CS	0h	USB	Port Reset Change (PRC):
20	RW1CS	0h	USB	Over-current Change (OCC):
19	RW1CS	0h	USB	Warm Port Reset Change (WRC):
18	RW1CS	0h	USB	Port Enabled Disabled Change (PEC):
17	RW1CS	0h	USB	Connect Status Change (CSC):
16	RW	0h	USB	Port Link State Write Strobe (LWS):
15:14	RWS	0h	USB	Port Indicator Control (PIC):
13:10	RO	0h	USB	Port Speed (Port_Speed):
9	RWS	1h	USB	Port Power (PP):
8:5	RWS	5h	USB	Port Link State (PLS):
4	RW1S	0h	USB	Port Reset (PR):
3	RO	0h	USB	Over-current Active (OCA):
2	RO	0h	USB	Reserved
1	RW1CS	0h	USB	Port Enabled Disabled (PED):
0	RO	0h	USB	Current Connect Status (CCS):

Table 189. PORTPMSCXUSB2 - Port X Power Management Status and Control USB2

Address Offset: Port 1 484-487h
Default Value:00000000h
Access: RO; RW; RWS;
Size:32 bits
There are 2 USB2 PORTPMSC registers at offsets:
 484h, 494h

Bit	Access	Default Value	RST/PWR	Description
31:28	RWS	0h	USB	Port Test Control (PTC) :
27:17	RO	0h	USB	Reserved
16	RW	0h	USB	Hardware LPM Enable (HLE):
15:8	RWS	0h	USB	L1 Device Slot (L1DS):
7:4	RWS	0h	USB	Host Initiated Resume Duration (HIRD) :
3	RWS	0h	USB	Remote Wake Enable (RWE):
2:0	RO	0h	USB	L1 Status (L1S):

Table 190. PORTHLPMX - Port X Hardware LPM Control Register (X: 1 ... NumUSB2)

Address Offset:Port 1 48C-48Fh
Default Value:00000000h
Access: RO; RWS; RW;
Size:32 bits
There are PORTHLPM registers at offsets :
48Ch, 49Ch, ... (48Ch + (NumUSB2-1)*10h)
This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST).
The definition for the fields depend on the protocol supported. For USB3 this register is reserved and shall be treated by software as RsvdP. For USB2 the definition is given below. Fields contain parameters necessary for xHC to automatically generate an LPM Token to the downstream device.

Bit	Access	Default Value	RST/PWR	Description
31:14	RO	0h	USB	RESERVED
13:10	RW	0h	USB	Host Initiated Resume Duration-Deep (HIRDD): System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us ... Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value.

Bit	Access	Default Value	RST/PWR	Description
9:2	RWS	0h	USB	L1 Timeout (L1TO): Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us
1:0	RWS	0h	USB	Host Initiated Resume Duration Mode (HIRDM): Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved

Table 191. PORTSCXUSB3 - Port X Status and Control USB3 (X: 1 ... NumUSB3)

Address Offset: See Below
Default Value:000002A0h
Access: RO; RWS; RW;
Size:32 bits
The USB3 PORTSC registers are at offsets:
First USB3 port: 480h+NumUSB2*10h
Next USB3 port : First USB3 Port + 10h
and so on...
Final USB3 Port : First USB3 Port + (NumUSB3-1)*10h)

Bit	Access	Default Value	RST/PWR	Description
31	RW1S	0h	USB	Warm Port Reset (WPR):
30	RWS	0h	USB	Device Removable (DR):
29:28	RO	0h	USB	Reserved
27	RWS	0h	USB	Wake on Over-current Enable (WOE):
26	RWS	0h	USB	Wake on Disconnect Enable (WDE):
25	RWS	0h	USB	Wake on Connect Enable (WCE):
24	RO	0h	USB	Cold Attach Status (CAS):
23	RW1CS	0h	USB	Port Config Error Change (CEC):
22	RW1CS	0h	USB	Port Link State Change (PLC):
21	RW1CS	0h	USB	Port Reset Change (PRC):
20	RW1CS	0h	USB	Over-current Change (OCC):
19	RW1CS	0h	USB	Warm Port Reset Change (WRC):
18	RW1CS	0h	USB	Port Enabled Disabled Change (PEC):
17	RW1CS	0h	USB	Connect Status Change (CSC):
16	RW	0h	USB	Port Link State Write Strobe (LWS):
15:14	RWS	0h	USB	Port Indicator Control (PIC):
13:10	RO	0h	USB	Port Speed (Port_Speed):
9	RWS	1h	USB	Port Power (PP):
8:5	RWS	5h	USB	Port Link State (PLS):
4	RW1S	0h	USB	Port Reset (PR):
3	RO	0h	USB	Over-current Active (OCA):
2	RO	0h	USB	Reserved
1	RW1CS	0h	USB	Port Enabled Disabled (PED):
0	RO	0h	USB	Current Connect Status (CCS):

Table 192. PORTPMSCX - Port X Power Management Status and Control USB3(X: 1 ... NumUSB3)

Address Offset: See Below
Default Value:00000000h
Access: RO; RW; RWS;
Size:32 bits
The USB3 PORTPMSC registers are at offsets:
First USB3 port: 484h+NumUSB2*10h
Next USB3 port : First USB3 Port + 10h
and so on...

Final USB3 Port : First USB3 Port + (NumUSB3-1)*10h)

Bit	Access	Default Value	RST/PWR	Description
31:17	RO	0h	USB	Reserved
16	RW	0h	USB	Force Link PM Accept (FLA):
15:8	RWS	0h	USB	U2 Timeout (U2TO):
7:0	RWS	0h	USB	U1 Timeout (U1TO):

Table 193. PORTLIX - Port X Link Info USB3 (X: 1 ... NumUSB3)
Address Offset:See Below
Default Value:00000000h
Access: RO;
Size:32 bits
The USB3 PORTLI registers are at offsets:

First USB3 port: 488h+NumUSB2*10h

Next USB3 port : First USB3 Port + 10h

and so on...

Final USB3 Port : First USB3 Port + (NumUSB3-1)*10h)

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	0h	USB	Reserved
15:0	RO	0h	USB	Link Error Count (LEC):

4.7.3 Host Controller Runtime Registers

Table 194. MFINDEX - Microframe Index

Address Offset:2000-2003h
Default Value:00000000h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:14	RO	0h	USB	Rsvd1 (Rsvd1):
13:0	RO	0h	USB	Microframe Index (MI):

Table 195. IMANx - Interrupter x Management

Address Offset:2020-2023h, 2040-2043h,...,2020+(MaxInts-1)*20h-2023+(MaxInts-1)*20h
Default Value:00000000h
Access: RO; RW; RW1C;
Size:32 bits
There are MaxInts IMAN registers.
x = 1, ..., MaxInts

Bit	Access	Default Value	RST/PWR	Description
31:2	RO	0h	USB	Rsvd1 (Rsvd1):
1	RW	0h	USB	Interrupt Enable (IE):
0	RW1C	0h	USB	Interrupt Pending (Interrupt Pending):

Table 196. IMODx - Interrupter x Moderation

Address Offset:2024-2027h, 2044-2047h, ..., 2024+(MaxInts-1)*20h-2027+(MaxInts-1)*20h
Default Value:00000FA0h
Access: RW;
Size:32 bits
There are MaxInts IMOD registers.
x = 1, ..., MaxInts

Bit	Access	Default Value	RST/PWR	Description
31:16	RW	0h	USB	Interrupt Moderation Counter (IMODC):

Bit	Access	Default Value	RST/PWR	Description
15:0	RW	0FA0h	USB	Interrupt Moderation Interval (IMODI):

Table 197. ERSTSZx - Event Ring Segment Table Size x

Address Offset:2028-202Bh, 2048-204Bh, ..., 2028+(MaxInts-1)*20h-202B+(MaxInts-1)*20h
Default Value:00000000h
Access: RO; RW;
Size:32 bits
There are MaxInts ERSTSZ register.
x = 1, ..., MaxInts

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	0h	USB	Rsvd1 (Rsvd1):
15:0	RW	0h	USB	Event Ring Segment Table Size (ERSTS):

Table 198. ERSTBA_LOx - Event Ring Segment Table Base Address Low x

Address Offset:2030-2033h, 2050-2053h, ..., 2030+(MaxInts-1)*20h-2033+(MaxInts-1)*20h
Default Value:00000000h
Access: RO; RW;
Size:32 bits
There are MaxInts ERSTBA_LO registers
x = 1, ..., MaxInts

Bit	Access	Default Value	RST/PWR	Description
31:6	RW	0h	USB	Event Ring Segment Table Base Address Register (ERSTBA_LO):
5:0	RO	0h	USB	Rsvd1 (Rsvd1):

Table 199. ERSTBA_HIx - Event Ring Segment Table Base Address High x

Address Offset:2034-2037h, 2054-2057h, ..., 2034+(MaxInts-1)*20h-2037+(MaxInts-1)*20h
Default Value:00000000h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	0h	USB	Event Ring Segment Table Base Address (ERSTBA_HI):

Table 200. ERDP_LOx - Event Ring Dequeue Pointer Low x

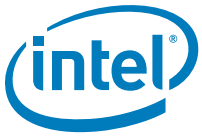
Address Offset:2038-203Bh, 2058-205Bh, ..., 2038+(MaxInts-1)*20h-203B+(MaxInts-1)*20h
Default Value:00000000h
Access: RW; RW1C;
Size:32 bits
There are MaxInts ERDP_LO registers.
x = 1, ...,MaxInts

Bit	Access	Default Value	RST/PWR	Description
31:4	RW	0h	USB	Event Ring Dequeue Pointer (ERDP):
3	RW1C	0h	USB	Event Handler Busy (EHB):
2:0	RW	0h	USB	Dequeue ERST Segment Index (DESI):

Table 201. ERDP_HIx - Event Ring Dequeue Pointer High x

Address Offset:203C-203Fh, 205C-205Fh, ..., 203C+(MaxInts-1)*20h-203F+(MaxInts-1)*20h
Default Value:00000000h
Access: RW;
Size:32 bits
There are MaxInts ERDP_HI registers.
x = 1, ..., MaxInts

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	0h	USB	Event Ring Dequeue Pointer (ERDP):



4.7.3.1 Doorbell Registers

Table 202. DOORBELL1 - Door Bell 1, 2, ..., 32

Address Offset:3000-3003h, 3004-3007h, ..., 307C-307Fh
Default Value:00000000h
Access: RW; RO; RD back always 0
Size:32 bits
Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Bit	Access	Default Value	RST/PWR	Description
31:16	RW	0h	USB	DB Stream ID (DBSID):
15:8	RO	0h	USB	Rsvd1 (Rsvd1):
7:0	RW	0h	USB	DB Target (9 DW):

4.7.4 Host Controller Extended Capability Registers

4.7.4.1 Summary of Extended Capabilities

Capability	ID	Start	End	Cap. Size	Valid Length
USB2 Supported Protocol Capability	2d	8000h	801Bh	7 DW	7 DW
USB3 Supported Protocol Capability	2d	8020h	806Fh	20 DW	10 DW
Intel Vendor Defined Capability	192d	8070h	846Bh	255DW	71 DW
USB Legacy Support Capability	1d	846Ch	84F3h	34 DW	2 DW
Intel Vendor Defined Capability (Port Disable Override Capability)	198d	84F4h	84FFh	3 DW	3 DW
Intel Vendor Defined Capability (HW State Access)	199d	8500	85FFh	64DW	5 DW
Intel Vendor Defined Capability (Chicken bit mirror from PCI Config)	194d	8600h	86FFh	64 DW	64 DW
USB Debug Capability	10d	8700h	873Fh	16 DW	16 DW
Intel Vendor Defined Capability (Debug Device Config)	195d	8740h	87FFh	48 DW	7 DW
Intel Vendor Defined Capability (SSIC Policy and Implementation specific Registers)	196d	8800h	88FFh	64 DW	9 DW
Intel Vendor Defined Capability (SSIC local and remote registers)	197d	8900h	8C33h	205 DW	(1 + (68 * NumSSICPorts)) DW upto 3 SSIC ports
USB3.1 Supported Protocol Capability	2d	8E28h	8E3Bh	12DW	5DW
Intel Vendor Defined Capability (Dublin Policy Registers)	202d	8E58h	8E8Fh	36DW	29DW

4.7.4.2 Supported Protocol Extended Capability

Table 203. Speed ID Mapping

Prot. Capability	Default Speed ID Value	Definition	Bit Rate	Protocol	Equivalent PSI Dword values			
					PLT	PFD	PSIE	PSIM
USB2 Capability	1	Full Speed	12 Mb/s	USB 2.0	0	0	2	12
	2	Low Speed	1.5 Mb/s	USB 2.0	0	0	1	1500
	3	High Speed	480 Mb/s	USB 2.0	0	0	2	480

Prot. Capability	Default Speed ID Value	Definition	Bit Rate	Protocol	Equivalent PSI Dword values			
					PLT	PFD	PSIE	PSIM
USB3 Capability	1	SSIC-G1A-L1	1.248 Gb/s	USB 3.0	0	1	2	1248
	2	SSIC-G2A-L1/ SSIC-G1A-L2	2.496 Gb/s	USB 3.0	0	1	2	2496
	3	SSIC-G3A-L1/ SSIC-G2A-L2/ SSIC-G1A-L4	4.992 Gb/s	USB 3.0	0	1	2	4992
	4	Super Speed	5 Gb/s	USB 3.0	0	1	3	5
	5	SSIC-G1B-L1	1.4576 Gb/s	USB 3.0	0	1	2	1457
	6	SSIC-G2B-L1/ SSIC-G1B-L2	2.9152 Gb/s	USB 3.0	0	1	2	2915
	7	SSIC-G3B-L1/ SSIC-G2B-L2/ SSIC-G1B-L4	5.8304 Gb/s	USB 3.0	0	1	2	5830
USB3.1 Capability	4	Super Speed	5 Gb/s	USB 3.0	0	1	3	5
	5	Super Speed Plus	10 Gb/s	USB 3.0	0	1	3	10

Table 8 HS-BURST: RATE Series and GEARs

RATE A-series (Mbps)	RATE B-series[1] (Mbps)	High-Speed GEARs
1248	1457.6	HS-G1 (A/B)
2496	2915.2	HS-G2 (A/B)
4992	5830.4	HS-G3 (A/B)

Table 204. XECP_SUPP_USB2_0 - XECP_SUPP_USB2_0

Address Offset:8000-8003h
Default Value:Varies based on SKU
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	2h	USB	USB Major Revision: 2.0
23:16	RO	0h	USB	USB Minor Revision
15:8	RO	8h	USB	Next Capability Pointer
7:0	RO	2h	USB	Supported Protocol ID

Table 205. XECP_SUPP_USB2_1 - XECP_SUPP_USB2_1

Address Offset:8004-8007h
Default Value:20425355h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:00	RO	20425355h	USB	XECP_SUPP_USB2_1 (XECP_SUPP_USB2_1) : Namestring USB

Table 206. XECP_SUPP_USB2_2 - XECP_SUPP_USB2_2

Address Offset:8008-800Bh
Default Value:30090F01h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:28	RO	3h	USB	Protocol Speed ID Count: 3 USB 2.0 Speed (High, Full, Low)
27:21	RO	0h	USB	Rsvd0 (Rsvd0) :

Bit	Access	Default Value	RST/PWR	Description
20	RW/L	1h	USB	BESL LPM Capability (BLC) - Bit is set to '1' to indicate that the the ports described by this xHCI Supported Protocol Capability will apply BESL timing to BESL and BESLD fields of the PORTPMSC and PORTHLPMC registers. This field can be modified and maintained by BIOS under Access Control
19	RW/L	1h	USB	Protocol Defined - Hardware LMP Capability (HLC) : This field can be modified and maintained by BIOS under Access Control
18	RO	0h	USB	Protocol Defined - Integrated Hub Implementation (IHI) :
17	RO	0h	USB	Protocol Defined - High SPeed Only (HSO) :
16	RO	1h	USB	Reserved
15:8	RW/L	NumUSB2	USB	Compatible Port Count
7:0	RO	1h	USB	Compatible Port Offset :

Table 207. XECP_SUPP_USB2_3 - XECP_SUPP_USB2_3 (Full Speed)

Address Offset:8010-8013h
Default Value:000C0021h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	Ch	USB	Protocol Speed ID Mantissa (PSIM)
15:9	RO	0h	USB	Rsvd0 (Rsvd0)
8	RO	0h	USB	PSI Full Duplex (PFD)
7:6	RO	0h	USB	PSI Type (PLT)
5:4	RO	2h	USB	Protocol Speed ID Exponent (PSIE)
3:0	RO	1h	USB	Protocol Speed ID Value (PSIV)

Table 208. XECP_SUPP_USB2_4 - XECP_SUPP_USB2_4 (Low Speed)

Address Offset:8014-8017h
Default Value:05DC0012h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	05DCh	USB	Protocol Speed ID Mantissa (PSIM)
15:9	RO	0h	USB	Rsvd0 (Rsvd0)
8	RO	0h	USB	PSI Full Duplex (PFD)
7:6	RO	0h	USB	PSI Type (PLT)
5:4	RO	1h	USB	Protocol Speed ID Exponent (PSIE)
3:0	RO	2h	USB	Protocol Speed ID Value (PSIV)

Table 209. XECP_SUPP_USB2_5 - XECP_SUPP_USB2_5 (High Speed)

Address Offset:8018-801Bh
Default Value:01E00023h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	1E0h	USB	Protocol Speed ID Mantissa (PSIM)
15:9	RO	0h	USB	Rsvd0 (Rsvd0)
8	RO	0h	USB	PSI Full Duplex (PFD)
7:6	RO	0h	USB	PSI Type (PLT)
5:4	RO	2h	USB	Protocol Speed ID Exponent (PSIE)
3:0	RO	3h	USB	Protocol Speed ID Value (PSIV)

Table 210. XECP_SUPP_USB3_0 - XECP_SUPP_USB3_0

Address Offset:8020-8023h
Default Value:03000802h
Access: RO;

Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	3h	USB	USB Major Revision: 3.0
23:16	RO	0h	USB	USB Minor Revision
15:8	RO	14h	USB	Next Capability Pointer
7:0	RO	2h	USB	Supported Protocol ID

Table 211. XECP_SUPP_USB3_1 - XECP_SUPP_USB3_1

Address Offset:8024-8027h
Default Value:20425355h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:00	RO	20425355h	USB	XECP_SUPP_USB3_1 (XECP_SUPP_USB2_1) : Namestring USB

Table 212. XECP_SUPP_USB3_2 - XECP_SUPP_USB3_2

Address Offset:8028-802Bh
Default Value:10000610h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:28	RO	3h1/ 1h	USB	Protocol Speed ID Count : 1 USB 3.0 Speed (Supper Speed)
27:16	RO	0h	USB	Rsvd0 (Rsvd0) :
15:8	RO	0	USB	Compatible Port Count :
7:0	RO	0	USB	Compatible Port Offset :

Table 213. XECP_SUPP_USB3_3 - XECP_SUPP_USB3_3 (SSIC-G1A-L1)

Address Offset:8030-8033h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	4E0h	USB	Protocol Speed ID Mantissa (PSIM)
15:9	RO	0h	USB	Rsvd0 (Rsvd0)
8	RO	1h	USB	PSI Full Duplex (PFD)
7:6	RO	0h	USB	PSI Type (PLT)
5:4	RO	2h	USB	Protocol Speed ID Exponent (PSIE)
3:0	RO	1h	USB	Protocol Speed ID Value (PSIV)

Table 214. XECP_SUPP_USB3_4 - XECP_SUPP_USB3_4 (SSIC-G2A-L1/SSIC-G1A-L2))

Address Offset:8034-8037h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	9C0h	USB	Protocol Speed ID Mantissa (PSIM)
15:9	RO	0h	USB	Rsvd0 (Rsvd0)
8	RO	1h	USB	PSI Full Duplex (PFD)
7:6	RO	0h	USB	PSI Type (PLT)
5:4	RO	2h	USB	Protocol Speed ID Exponent (PSIE)
3:0	RO	2h	USB	Protocol Speed ID Value (PSIV)

Table 215. XECP_SUPP_USB3_5 - XECP_SUPP_USB3_5 (SSIC-G3A-L1/SSIC-G2A-L2/SSIC-G1A-L4))

Address Offset:8038-803Bh
Access: RO;

Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	1380h	USB	Protocol Speed ID Mantissa (PSIM)
15:9	RO	0h	USB	Rsvd0 (Rsvd0)
8	RO	1h	USB	PSI Full Duplex (PFD)
7:6	RO	0h	USB	PSI Type (PLT)
5:4	RO	2h	USB	Protocol Speed ID Exponent (PSIE)
3:0	RO	3h	USB	Protocol Speed ID Value (PSIV)

Table 216. XECP_SUPP_USB3_6 - XECP_SUPP_USB3_6 (Super Speed)

Address Offset:803C-803Fh
Default Value:00050134h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	5h	USB	Protocol Speed ID Mantissa (PSIM)
15:9	RO	0h	USB	Rsvd0 (Rsvd0)
8	RO	1h	USB	PSI Full Duplex (PFD)
7:6	RO	0h	USB	PSI Type (PLT)
5:4	RO	3h	USB	Protocol Speed ID Exponent (PSIE)
3:0	RO	4h	USB	Protocol Speed ID Value (PSIV)

Table 217. XECP_SUPP_USB3_7 - XECP_SUPP_USB3_7 (SSIC-G1B-L1)

Address Offset:8040-8043h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	5B1h	USB	Protocol Speed ID Mantissa (PSIM)
15:9	RO	0h	USB	Rsvd0 (Rsvd0)
8	RO	1h	USB	PSI Full Duplex (PFD)
7:6	RO	0h	USB	PSI Type (PLT)
5:4	RO	2h	USB	Protocol Speed ID Exponent (PSIE)
3:0	RO	5h	USB	Protocol Speed ID Value (PSIV)

Table 218. XECP_SUPP_USB3_8 - XECP_SUPP_USB3_8 (SSIC-G2B-L1/SSIC-G1B-L2))

Address Offset:8044-8047h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	B63h	USB	Protocol Speed ID Mantissa (PSIM)
15:9	RO	0h	USB	Rsvd0 (Rsvd0)
8	RO	1h	USB	PSI Full Duplex (PFD)
7:6	RO	0h	USB	PSI Type (PLT)
5:4	RO	2h	USB	Protocol Speed ID Exponent (PSIE)
3:0	RO	6h	USB	Protocol Speed ID Value (PSIV)

Table 219. XECP_SUPP_USB3_9 - XECP_SUPP_USB3_9 (SSIC-G3B-L1/SSIC-G2B-L2/SSIC-G1B-L4))

Address Offset:8048-804Ch
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	16C6h	USB	Protocol Speed ID Mantissa (PSIM)
15:9	RO	0h	USB	Rsvd0 (Rsvd0)
8	RO	1h	USB	PSI Full Duplex (PFD)
7:6	RO	0h	USB	PSI Type (PLT)
5:4	RO	2h	USB	Protocol Speed ID Exponent (PSIE)

Bit	Access	Default Value	RST/PWR	Description
3:0	RO	7h	USB	Protocol Speed ID Value (PSIV)

Table 220. XECP_SUPP_USB3_1_0 - XECP_SUPP_USB3_1_0

Address Offset:8E28-8E2Bh
Default Value:03000802h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	3h	USB	USB Major Revision: 3
23:16	RO	1h	USB	USB Minor Revision: 0.1
15:8	RO	0Ch	USB	Next Capability Pointer
7:0	RO	2h	USB	Supported Protocol ID

Table 221. XECP_SUPP_USB3_1_1 - XECP_SUPP_USB3_1_1

Address Offset:8E2C-8E2Fh
Default Value:20425355h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:00	RO	20425355h	USB	XECP_SUPP_USB3_1_1 (XECP_SUPP_USB3_1_1) : Namestring USB

Table 222. XECP_SUPP_USB3_1_2 - XECP_SUPP_USB3_1_2

Address Offset:8E30-8E33h
Default Value:10000610h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:28	RO	3h1/ 1h	USB	Protocol Speed ID Count : 1 USB 3.0 Speed (Supper Speed)
27:16	RO	0h	USB	Rsvd0 (Rsvd0) :
15:8	RO	NumUSB3	USB	Compatible Port Count :
7:0	RO	NumUSB2+1	USB	Compatible Port Offset :

Note:

If NumSSICports = 0, Protocol Speed ID Count =1h

Table 223. XECP_SUPP_USB3_1_3 - XECP_SUPP_USB3_1_3 (Super Speed)

Address Offset:8E34-8E37h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	5h	USB	Protocol Speed ID Mantissa (PSIM)
15:9	RO	0h	USB	Rsvd0 (Rsvd0)
8	RO	1h	USB	PSI Full Duplex (PFD)
7:6	RO	0h	USB	PSI Type (PLT)
5:4	RO	3h	USB	Protocol Speed ID Exponent (PSIE)
3:0	RO	4h	USB	Protocol Speed ID Value (PSIV)

Table 224. XECP_SUPP_USB3_1_4 - XECP_SUPP_USB3_1_4 (Super Speed Plus)

Address Offset:8E38-8E3Bh
Access: RO;

Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	10h	USB	Protocol Speed ID Mantissa (PSIM)
15:9	RO	0h	USB	Rsvd0 (Rsvd0)
8	RO	1h	USB	PSI Full Duplex (PFD)
7:6	RO	0h	USB	PSI Type (PLT)
5:4	RO	3h	USB	Protocol Speed ID Exponent (PSIE)
3:0	RO	5h	USB	Protocol Speed ID Value (PSIV)

4.7.4.3 Vendor Defined Capability

Table 225. HOST_CTRL_CAP_REG - Host Controller Capability

Address Offset:8070-8073h
Default Value:0000B0C0h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	00h	USB	Reserved
23:16	RO	45h	USB	Save Length Indicates the number of DWords in this capability starting at 8090h, that need to be saved and restored This value needs to be updated as new chicken bit registers are added. 45h -> 81A7h is the last valid byte to be saved
15:8	RO	FFh	USB	Next Capability Pointer
7:0	RO	C0h	USB	Supported Protocol ID

Table 226. HOST_CLR_MASK_REG - Override EP Flow Control

Address Offset:8078-807Bh
Default Value:00000000h
Access: WO, RD back always 0;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:10	RO	0h	USB	RESERVED
9:5	WO	0h	USB	5bits of slot number as a default configuration. It can scale to max of 128 slots
4:1	WO	0h	USB	4bits of EP number
0	WO	0h	USB	This is a register that is used to clear the internal scheduler's mask that is used to stop scheduling a particular EP. Bit0 indicates the direction of the EP

Table 227. HOST_CLR_IN_EP_VALID_REG - Clear Active IN EP ID Control

Address Offset:807C-807Fh
Default Value:00000000h
Access:WO, Read back to 0;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:0	WO	0h	USB	Clear Active IN EP ID Control (HOST_CLR_IN_EP_VALID_REG): This register is used to clear the internal valid IN EP array that TRM stored in order to guarantee one IN EP per port. This register allows software to clear the valid bit of each port IN EP. This field indicates the port number. For a 2port configuration, only bit1:0 are valid. It can scale for the max number of ports that we support.

Table 228. HOST_CLR_PMASK_REG - Clear Poll Mask Control

Address Offset:8080-8083h
Default Value:00000000h
Access: WO, Read back to 0;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:10	RO	0h	USB	RESERVED
9:5	WO	0h	USB	5bits of slot number as a default configuration. It can scale to max of 128 slots
4:1	WO	0h	USB	4bits of EP number
0	WO	0h	USB	This is a register that is used to clear the internal scheduler's poll mask that is used to indicate whether we need to poll this EP. This is used for USB2. Bit0 indicates the direction of the EP

Table 229. HOST_CTLR_OCRD_REG - Port Credit Control

Address Offset:8084-8087h
Default Value:00000000h
Access: WO, Read back to 0;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31	WO	0h	USB	Write 1 to force XFER state return to IDLE
30	WO	0h	USB	Write 1 to force CPL state return to IDLE
29	WO	0h	USB	Add one credit to a port
28	WO	0h	USB	Substract one credit from a port
27:8	RO	0h	USB	RESERVED
7:0	WO	0h	USB	This is a register that is used to add or substract a per port credit or to control the TRM's XFER and CPL states. port number

Table 230. HOST_CTRL_TEST_BUS_LO - Test Bus Low

Address Offset:8088-808Bh
Default Value:00000000h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:0	RO	0h	USB	Test Bus Low (HOST_CTRL_TEST_BUS_LO): Host controller test bus low 32bits. This is used to read the internal states and other important signals. The host control test bus is gathered from different internal modules for its important states and control/status information. We have a 64bits register that allows us to read a bus of 64bits

Table 231. HOST_CTRL_TEST_BUS_HI - Test Bus High

Address Offset:808C-808Fh
Default Value:00000000h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:0	RO	0h	USB	Test Bus High (HOST_CTRL_TEST_BUS_HI): Host controller test bus high 32bits. This is used to read the internal states and other important signals. The host control test bus is gathered from different internal modules for its important states and control/status information. We have a 64bits register that allows us to read a bus of 64bits

Table 232. HOST_CTRL_TRM_REG - Host Control Transfer Manager (TRM)

Address Offset:8090-8093h
Default Value:4C1BD105h
Access: RW;
Size:32 bits
This register contains fields which control the behavior of the Transfer Manager in the XHC.

Bit	Access	Default Value	RST/PWR	Description
31	RW	0h	USB	Reserved. It must set to 0 .
30	RW	1h	USB	1: Enables a special function which we will detect NAK received and go into a single packet pace mode so that we don't burst ahead. 0: Disables this function.
29	RW	0h	USB	1: Disables the error check for Data Move stream state. It will generate a transfer event with prime PIPE error completion code if error detected. 0: Enable the error check.
28	RW	0h	USB	1: Disables the error check for prime PIPE stream state. It will generate a transfer event with prime PIPE error completion code if error detected. 0: Enable the error check.
27	RW	1h	USB	This bit has been modified for its usage since PPTA0. It is used to allow NO-OP TRB to be treated in a same way as link TRB. In other words, it will update the internal context when it is fetched while the internal context cache TRB FIFO is empty. 1: enabled the cache function 0: disable the function
26	RW	1h	USB	This is a special internal condition enable for CPL engine which it enables all EP halt conditions detected to cause the proper actions in a response. 1: enabled 0: disabled Note: only default condition of 1 is validated.
25	RW	0h	USB	This is a special internal branch condition control in XFER engine which does the EP transfer ring process. When this bit is set, a retry condition identified by completion engine will cause XFER engine to stop what it is currently in progress and start over from state IDLE. 1: enabled the branch condition 0: disabled.
24	RW	0h	USB	This is a special internal branch condition control in XFER engine which does the EP transfer ring process. When this bit is set, the XFER will not continue even if the next TRB is identified as a non DMA TRB. The engine will then wait for the next scheduled request for this EP. 1: enabled the branch condition 0: disabled.
23	RW	0h	USB	When ERDP register is updated by software, it is expected as an atomic function since this is a 64bit register. It is expected that the ERDP (64bits register) is updated together when ERDP high 32 is written. We have this bit designed to ignore the atomic operation required from software for ERDP low 32bits. When this bit is set to 1, it will update the ERDP low 32bits when software issues a CPU write to the ERDP low 32 bit. 1: ignore atomic operation 0: not ignore.
22	RW	0h	USB	Setting this bit to 1 will force an internal doorbell ring on the EP that it has received a response.
21	RW	0h	USB	0: Drop ERDYs received when not in a flow control state. 1: Do not drop ERDYs received when not in a flow control state. Note: We typically drop unexpected ERDY
20	RW	1h	USB	0: Disable timeout of TRB error processing. 1: Enable timeout of a TRB processing in few critical states that possibly have a deadlock for unexpected reason. A vendor defined completion code is generated in the event of a timeout during TRB processing.

Bit	Access	Default Value	RST/PWR	Description
19	RW	1h	USB	This big is modified to enable a feature where we can control whether or not to report an event with completion code of Missed Service Error when a short packet response has been received not in the expected service interval. 1: enables all completion event that supposedly is short to the MSE. 0: Disable this function so that the xHC engine will report an event of with Short packet indication and another event with MSE at the end of the TD.
18	RW	0h	USB	This bit is modified to enable the NOOP TRB as a TD when Missing Service Interval Error has encountered. This is only for PPT B0, LPT and CB. 1: enabled 0: disabled
17	RW	1h	USB	Enable a special branch condition of the XFER ring process state. This is to ensure that we have a DMA request issued to DMA engine during a PHASE1 process of the TTE. 1: enabled 0: disabled
16	RW	1h	USB	0: Disable error reporting for this case. 1: Enable error reporting if a SETUP TRB contains the following: bRequest = SET_ADDRES bmRequestType = (DTD) Host-to-device, Type = Standard, & Recipient = Device
15	RW	1h	USB	Enables a special internal state branch condition for periodic EP during its transfer ring process. If we have identified that the next TRB is a non DMAnable TRB such as LINK TRB, or Event data TRB, then this bit enables XFER engine to continue process the next TRB as if the ENT bit of the TRB is set. 1: enable 0: disable
14	RW	1h	USB	XFER engine has a new function that provides a support to ISO EP within a long PCIe delayed system. The long delay can cause missing service interval while pending response has not all been returned. This bit enables engine to identify a MSI condition and stored the context bit for a pending response so that we can process a MSI event when pending response received. 1: enables this function 0: disable this function
13	RW	0h	USB	0: Bulk and interrupt endpoints use burst size defined by endpoint context. 1: Force the Bulk and Interrupt endpoints use a burst size of 1.
12	RW	1h	USB	0: ENT bit is ignored. 1: ENT bit is processed. The transfer engine will service the next TRB.
11	RW	0h	USB	Setting this bit to 1 will force the transfer engine to set the packet boundary flag. This flag is an important flag which may cause a deadlock. This is a safety feature that we pluged in.
10	RW	0h	USB	This bit is modified to support PPTB0, LPT and CP for a feature that we will clear the single IN EP array based on ISO flush or short flush. 0: Indicate that we do not need to clear IN EP array based on flush conditions. 1: indicate that we do clear IN EP array based on flush conditions
9	RW	0h	USB	Setting this bit to 1 will force the transfer engine state machine to exit the CPL_WAIT state. This is designed to avoid unexpected deadlock in CPL_WAIT state.
8	RW	1h	USB	0: Disable internal TRB cache invalidation. 1: Enable internal TRB cache invalidation auto detect function This will allow engine to handle more than 4TRBs per packet.

Bit	Access	Default Value	RST/PWR	Description
7	RW	0h	USB	0: USB3 responses with NumPkts equal to 0 will be treated as a flow control condition. 1: USB3 responses with NumPkts equal to 0 will not be treated as a flow control condition.
6	RW	0h	USB	0: Babble errors will not disable the port. 1: Babble errors will disable the auto detect function This will allow engine to handle more than 4TRBs per packet.
5	RW	0h	USB	Enable a function which we can clear mask of an EP on any response of that EP. 0: Clear the scheduler mask normally. 1: Clear the scheduler mask on each received packet.
4	RW	0h	USB	This bit is designed to allow XFER engine to do a transfer without checking against the available port credit. 0: Advertises accurate buffer credit information to the scheduler. 1: Advertises non-zero buffer credits to the scheduler. (e.g. never backpressure back on buffer credit information)
3	RW	0h	USB	0: Process stalls reported by the DMA engine. 1: Ignore stall response received reported by the DMA engine.
2	RW	1h	USB	This bit is added for bug FR4836. It is to ring internal doorbell on that EP (applies to USB2 HS Bulk OUT and Control EPs) that receives NYET response. 1: Enable the feature 0 : Disabled
1	RW	0h	USB	0: obay the NPKT0 and EOB flow control. 1: Ignore received flow control for implied NRDY (e.g EOB or NPKT=0) for USB3 only
0	RW	1h	USB	0: Disable TD pacing for IN endpoint. 1: Enable TD pacing for IN endpoints.

Table 233. HOST_CTRL_SCH_REG - Host Control Scheduler

Address Offset:8094-8097h
Default Value:00008100h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31	RW	0h	USB	disable repeat scheduler service of usb2 periodic
30:27	RW	0h	USB	enable scheduler limiter functions to block async. traffic types across ports while periodic pending.
26	RW	0h	USB	enable pkt pending notification to usb3 ports
25	RW	0h	USB	disable async. burst limitation while periodic in progress
24	RW	0h	USB	disable marking overlap flag on all TT periodic INs.
23	RW	0h	USB	disable async. scheduling while periodic active to same port
22	RW	0h	USB	disable “level” method of USB2 port periodic done check (on by default)
21	RW	0h	USB	enable “strobe” method of USB2 port periodic done check (off by default)
20:13	RW	0h	USB	TTE Host Control
31:22	RW	0h	USB	Scheduler: Reserved
21	RW	0h	RW	Scheduler: Enable Stop serving packets to disabled port
20:17	RW	0h	USB	TTE: Reserved
16	RW	0h	USB	disable deferred split error request on speculative IN with data payload and no TRB.
15	RW	1h	USB	TTE: disable split error request w/NULL pointer on speculative INs with data payload and no TRB.
14	RW	0h	USB	TTE: Disable checking of missed microframes
13	RW	0h	USB	TTE: Disable interrupt complete split limit to 3 micro frames
12:11	RW	0h	USB	Cmd Mgr: Cache size control reg 0: 64 1: 32 2,3: 16

Bit	Access	Default Value	RST/PWR	Description
10:9	RW	0h	USB	Cmd Mgr: Allow dynamically setting different max EP allowed. The max EP supported scales with the scratch pad size. This allows driver to allocate small memory sizes if it needed. 0: 32 eps 1: 16 eps 2: 8 eps 3: 4 eps
8	RW	1h	USB	Cmd Mgr: Enables scratch pad function
7	RW	0h	USB	Scheduler: enable check to stop scheduling on port that are not connected
6	RW	0h	USB	Scheduler: disable 1 pack scheduling limit when ISO pending in present microframe
5:4	RW	0h	USB	Scheduler: scheduler sort pattern 00 (default) search ISO ahead of interrupt within each service interval 01 - search USB2-ISO, USB3-ISO, USB2-Interrupt, USB3-Interrupt within each service interval 10 - search strictly by interval 11 - search all ISO intervals ahead interrupt intervals and within each interval, USB2 ahead of USB3
3	RW	0h	USB	Scheduler: enable TTE overlap prevention on interrupt OUT EPs (at cost of possible service interval slip)
2	RW	0h	USB	Scheduler: enable TTE overlap prevention on interrupt IN EPs (at cost of possible service interval slip)
1	RW	0h	USB	Scheduler: Deisable TRM active IN EP valid check function
0	RW	0h	USB	Scheduler: Disable poll delay function

Table 234. HOST_CTRL_ODMA_REG - Host Control ODMA

Address Offset:8098-809Bh
Default Value:14003002h
Access: RO; RW;
Size:32 bits
This register contains a number of fields that provide a specific level of configurability for the OUT DMA

Bit	Access	Default Value	RST/PWR	Description
31:24	RW	14h	USB	The value in this field dictates the wait time (in u-seconds) between retries initiated from the Set Address Finite State Machine
23	RO	0h	USB	RESERVED
22	RW	0h	USB	This bit controls the b2b write (with-in pkt) capability of IDMA DM engine. 0 : b2b write is enabled 1 : b2b write is disabled
21	RW	0h	USB	This bit controls the de-coupling of Context+CPL actions from DataMover Handler. 0 : De-couple Context Processing + CPL Engine handshake from DataMover Handler 1 : Disable de-coupling of Context Processing + CPL Engine handshake From DataMover Handler (Old mode)
20	RW	0h	USB	This bit adds the pipe stage in CPL Engine handshake to de-couple CPL Engine handshake from the Control logic. 0 : De-couple CPL Engine handshake from the control logic (DataMover or Context Handler) 1 : Disable de-coupling CPL Engine handshake from the control logic (DataMover or Context Handler)
19	RO	0h	USB	Reserved
18	RW	0h	USB	Setting this field will enable ACK FIFO credit accounting. ODMA will ensure that ample room exists in the ACK FIFO for expected device responses prior to initiating a given DP
17	RW	0h	USB	Setting this field will backpressure the Set Address Finite State Machine based on the availability of ACK FIFO credits
16	RW	0h	USB	Setting this field will disable the enforced wait time between retries initiated from the Set Address Finite State Machine

Bit	Access	Default Value	RST/PWR	Description
15	RW	0h	USB	Setting this field will prohibit ODMA from automatically dropping all deferred packets received on ISOCHRONOUS endpoints
14	RW	0h	USB	Setting this field will immediately force an EP timeout on all outstanding EPs on a given port when a port disconnect is detected
13	RW	1h	USB	Setting this field will enable ACK FIFO individual credit accounting mechanisms for Async vs. Periodic Endpoints. ODMA will ensure that ample room exists in the ACK FIFO for expected device responses prior to initiating a given DP
12	RW	1h	USB	0: Employs a 1us EP Transaction Base Timer. Enables a Timeout range from 16us to 64us 1: Employs a 125us EP Transaction Base Timer. Enables a Timeout range from 2ms to 8ms
11	RW	0h	USB	Setting this field will prohibit the Set Address Finite State Machine Credit Handshake with TTE Logic
10	RW	0h	USB	Setting this field will disable the EP Transaction Timer function when the Command Manager is performing a Stop Endpoint Command or when the LTSSM is in Recovery
9	RW	0h	USB	Setting this field prohibits the Set Address Finite State Machine from being flow controlled when an ACK with NPKT=0 is received in response to the SETUP DP initiated during SET_ADDRESS
8	RW	0h	USB	Setting this field generates a pulse that clears the ownership of the context semaphore that is shared between the Out DMA Response and Completion Finite State Machines
7	RW	0h	USB	Setting this field generates a pulse that implicitly returns all of the Out DMA ACK credits on all ports
6	RW	0h	USB	Setting this field generates a pulse that returns the Out DMA Set Address Finite State Machine into the IDLE state
5	RW	0h	USB	Setting this field generates a pulse that returns the Out DMA Completion Finite State Machine into the IDLE state
4	RW	0h	USB	Setting this field generates a pulse that returns the Out DMA Response Finite State Machine into the IDLE state
3	RW	0h	USB	Setting this field generates a pulse that returns the Out DMA Read Finite State Machine into the IDLE state
2:1	RW	1h	USB	Controls the duration of the EP Transaction Timeout (depends on the setting of bit[12]) 0: 64us ([12]=0) or 8ms ([12]=1) EP Transaction Timeout 1: 32us ([12]=0) or 4ms ([12]=1) EP Transaction Timeout 2: 16us ([12]=0) or 2ms ([12]=1) EP Transaction Timeout 3: EP Transaction Timer is DISABLED
0	RW	0h	USB	0: Enables the EP Transaction Timeout Function 1: Disables the EP Transaction Timeout Function

Table 235. HOST_CTRL_IDMA_REG - Host Control IDMA

Address Offset:809C-809Fh
Default Value:00000402h
Access: RW;
Size:32 bits
This register contains a number of fields that provide a specific level of configurability for the IN DMA

Bit	Access	Default Value	RST/PWR	Description
31	RO	0h	USB	RESERVED
30	RW	0h	USB	Setting this field will allow the Event Manager to treat either Transfer Manger (when 1) or Completion Engine (when 0) Event requests with higher priority.
29	RW	0h	USB	Setting this field will allow the Doorbell Manager to post events on a given transfer ring
28:26	RO	0h	USB	RESERVED
25	RW	0h	USB	Setting this field will cause the TTE Address FIFO to flush when bit[18] is strobed.

Bit	Access	Default Value	RST/PWR	Description
24	RW	0h	USB	0: Flush the Asynchronous Address FIFO when bit[18] is strobed 1: Flush the Periodic Address FIFO when bit[18] is strobed
23:19	RW	0h	USB	The value in this field indicates the port number of the address FIFO to flush when bit[18] is strobed
18	RW	0h	USB	Setting this field will generate a strobe causing a give Periodic or Asynchronous Address FIFO to flush. FIFO flushed is a function of bits [25:19]
17	RW	0h	USB	0: All response acknowledges (ACKs) are put in the periodic header FIFO in XPPE 1: Only periodic response acknowledges (ACKs) are put in the periodic header FIFO in XPPE
16	RW	0h	USB	0: Default IDMA Pointer Buffer Room to a default value of 8. Requires a strobe of bit[3] to take effect. 1: Default IDMA Pointer Buffer Room to a default value of 4. Requires a strobe of bit[3] to take effect.
15	RW	0h	USB	Setting this field will prohibit IDMA from automatically dropping received DPs when a given endpoint currently has no outstanding transactions
14	RW	0h	USB	Setting this field will prohibit IDMA from automatically dropping received DPs when a given endpoint is currently in a flow controlled state
13	RW	0h	USB	Setting this field will prohibit IDMA from automatically dropping all deferred packets received on ISOCHRONOUS endpoints
12	RW	0h	USB	Setting this field will immediately force an EP timeout on all outstanding EPs on a given port when a port disconnect is detected
11	RW	0h	USB	Setting this field will disable sequence number context checking when NRDY or STALL TP are received
10	RW	1h	USB	0: Employs a 1us EP Transaction Base Timer. Enables a Timeout range from 16us to 64us 1: Employs a 125us EP Transaction Base Timer. Enables a Timeout range from 2ms to 8ms
9	RW	0h	USB	Setting this field will disable the EP Transaction Timer function when the Command Manager is performing a Stop Endpoint Command or when the LTSSM is in Recovery
8	RW	0h	USB	Setting this field enables the Compliance Isochronous mode of operation. It bounds the upper limit on the NPKT field for all ISO Acknowledgments generated from the Host to the value of 2.
7	RW	0h	USB	Setting this field generates a pulse that clears the ownership of the context semaphore that is shared between the IN DMA Acknowledge and Data Mover Finite State Machines
6	RW	0h	USB	Setting this field generates a pulse that returns the IN DMA Data Mover Finite State Machine into the IDLE state
5	RW	0h	USB	Setting this field generates a pulse that returns the IN DMA Acknowledge Finite State Machine into the IDLE state
4	RW	0h	USB	Setting this field generates a pulse that implicitly returns all of the IN DMA Data Packet credits on all ports
3	RW	0h	USB	Setting this field generates a pulse that clears all the Read and Write Pointers associated with the various DMA Address FIFOs causing them to appear empty
2:1	RW	1h	USB	Controls the duration of the EP Transaction Timeout (depends on the setting of bit[10]) 0: 16us ([10]=0) or 2ms ([10]=1) EP Transaction Timeout 1: 32us ([10]=0) or 4ms ([10]=1) EP Transaction Timeout 2: 64us ([10]=0) or 8ms ([10]=1) EP Transaction Timeout 3: EP Transaction Timer is DISABLED
0	RW	0h	USB	0: Enables the EP Transaction Timeout Function 1: Disables the EP Transaction Timeout Function

Table 236. HOST_CTRL_PORT_CTRL - Global Port Control
Address Offset:80A0-80A3h

Default Value:0003F80Fh
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31	RW	0	USB	Overflow Error Detection Enable
30:12	RW	3h	USB	HBUF Water Mark
11	RW	1h	USB	CPL Cut Thru Enable
10:4	RW	0h	USB	Reserved
3:0	RW	Fh	USB	Reserved

Table 237. PMCTRL – Power Management Control

Address Offset:80A4-80A7h
Default Value:0h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31	RW	0b	USB	Async PME Source Enable This field allows the async PME source to be allowed to generate PME. This is specifically required for SOC's that do not allow for any clock other than RTC to be available during RTD3.
30	RW	0b	USB	Legacy PME Source Enable This field allows the legacy PME source to be used in PME generation. The legacy source is in reference to the source prior to the RTD3 changes.
29	RW	0b	USB	Reset Prep Power Gate Trigger Disable This field controls the actions taken for due to reset warn. 0 – Reset Warn will trigger a HW autonomous Power Gate 1 – Reset Warn will not trigger a HW autonomous Power Gate
28	WO	0b	USB	Internal PME flag Clear This Write-Only bit can be used to clear the internal PME flag. SW write to '1' will clear the PME flag. SW write to '0' will have no effect and be ignored by the controller. Read always return '0'.
27	RW	0h	USB	Disable D3 Power Gating without Save
26	RW	0b	USB	XLFPSCOUNTSRC (Source for LFPS OFF Counter) 0: Central RTC Counter for LFPS detection 1: Local Counter for LFPS detection
25	RW	0b	USB	XELFPSRTC (Enable LFPS Filtering on RTC) 0: Use Oscillator clock for LFPS Filtering during P3 1: Use RTC Clock for LFPS Filtering during P3
24	RW	0b	USB	XMPHYSPGDD0I2 (ModPhy Sus Well Power Gate Disable for D0I2) 0 : Modphy sus well power gating enabled 1 : Modphy sus well power gating disabled
23	RW	0b	USB	XMPHYSPGDD0I3 (ModPhy Sus Well Power Gate Disable for D0I3) 0 : Modphy sus well power gating enabled 1 : Modphy sus well power gating disabled
22	RW	0b	USB	XMPHYSPGDRTD3 (ModPhy Sus Well Power Gate Disable for RTD3) 0 : Modphy sus well power gating enabled 1 : Modphy sus well power gating disabled

Bit	Access	Default Value	RST/PWR	Description
21:18	RW	Bh	USB	XD3RTCPTTM (D3 RTC Port Timer Tick Multiplier) This register will be the multiplication factor for determining SSIC Wake Detection Frequency and RXDET based on the " U3 LFPS Periodic Sampling OFF Time Control" value. If this field is 9h and this register is Bh, frequency for RXDET and SSIC H8EXIT detection while MODPHY USB Power gating is enabled would be 99ms.
17	RW	0b	USB	U3 LFPS Periodic Sampling ON Time Control This field controls the ON time for the LFPS periodic sampling for USB3/SSIC ports. 0 – ON time is 2 rtc clocks 1 – ON time is 3 rtc clocks Note: This field is ignored if USB3/SSIC PHY USB Well Power Gating is enabled. The ON Time is determined by "U3 LFPS Periodic Sampling ON Time Control" field of this register if MODPHY USB Well Power Gating is disabled or by "LFPSONCOUNT" Register if MODPHY USB Well Power Gating is enabled.
16	RW	1b	USB	SS AON LFPS Detector Enable This field controls the LFPS ownership between the gated and AON domain for the case when the controller is not power gated. 1: Allow the LFSP Detector in AON to own LFPS detection when the port is in PS3 for U2/U3 (not RxD) regardless of port ownership (i.e. AON owns U2/U3 exit for all PS3 U2/U3 exit). 0: Allow the LFPS Detector in AON to own the LFPS detection only when the AON owns the port and in U2/U3 (not RxD), otherwise the gated domain LFPS detector will handle U2/U3 wake.
15:8	RW	FFh	USB	SS U3 LFPS Detection Threshold This field controls the threshold used to determine when a valid U3 Wake is detected through when using the unfiltered LFPS source. The value on this field will reflect the binary count required to have been detected on the counter being clocked by the unfiltered lfps source to result in a valid U3 wake detection.
7:4	RW	9h	USB	U3 LFPS Periodic Sampling OFF Time Control This field controls the OFF time for the LFPS periodic sampling for USB3 Ports This field is also used for SSIC H8 Exit and RXDET Polling multiplying it with XD3RTCPTTM 0x0 – periodic sampling is disabled. 0x1 – OFF time is 1ms 0x2 – OFF time is 2ms …. 0xF – OFF time is 15ms A speed up mode shall be implemented where this field is in units of us. i.e. 0x1 = 1 us OFF time, 0x2 = 2 us OFF time, etc.
3	RW	0h	USB	PS3 LFPS Source Select 0 – LFPS Source is unfiltered 1 – LFPS Source is filtered (Rx-Elec-Idle) LFPS Source is Rx-Elec-Idle for any non PS3 state.

Bit	Access	Default Value	RST/PWR	Description
2	RW	0h	USB	XHCI Engine Autonomous Power Gate Exit Reset Policy Controls when the xHCI engine is brought out of reset due to a power ungate. 0 – Engine is brought out of reset when D3 to D0 is triggered. This allows for a quick power up sequence while leaving the virtual PCIe LTSSM in L23 is power ungate is not due to D3 to D0. 1 – Engine is brought out of reset along with the rest of the IP. This is required for PMC save/restore flow.
1	RW	0h	USB	USB2 Port Wake Unit Coupling Policy Controls the trigger for USB3 Port Wake Units to initiate Port Level Power Off Preparation. – RTD3 Triggered 1 – Port Triggered when in L1, L2 or Disabled, Disconnected
0	RW	0h	USB	USB3 Port Wake Unit Coupling Policy Controls the trigger for USB3 Port Wake Units to initiate Port Level Power Off Preparation. – RTD3 Triggered 1 – Port Triggered when in PS3 due to RxDetect, U3, U2 or Disabled

Table 238. PGCBCTRL – PGCB Control

Address Offset:80A8-80ABh
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:28	RW	0h	USB	RESERVED FOR FUTURE USE
27:25	RW	0h	USB	IP-Inaccessible Hysteresis Timer 000 _ 50us 001 _ 100us 010 _ 150us 011 _ 200us 000 _ 250us 001 _ 300us 010 _ 350us 111 _ 400us
24	RW	1h	USB	Override Enable
23:20	RW	3h	USB	CDH Aggregation Minimum Wait Time This field controls the minimum time that we must wait for resets to propagate before allowing Power Up flow to complete. The Power Up flow requires special handling of clocks, reset and sleep signaling which requires the CDH to monitor reset propagation. This timer allow for flexibility on when we consider all resets propagated. 0h – Disabled 1h – 2 clocks 2h – 4 clocks 3h – 8 clocks 4h – 16 clocks 5h – 32 clocks 6h – 64 clocks 7h – 128 clocks

Bit	Access	Default Value	RST/PWR	Description
19	RW	0h	USB	CDH Reset Propagation Aggregation Control This bit will indicate the mode of operation for the CDH Reset Propagation Aggregator. It allows for a mode where the aggregation will wait for an indication from each CDH before proceeding OR ignore the CDH indication before proceeding. Regardless of the mode, the aggregator will enforce the CDH Aggregation Mini Wait Time. 0 – Aggregate all the CDH indications before triggering the CDH Aggregation Mini Wait Time. Once the Min Wait Time is met a notification to the Power Sequencer/ Control will be initiated 1 – Trigger the CDH Aggregation Mini Wait Time w/o waiting for CDH indication. Once the Min Wait time is met a notification to the Power Sequencer/Control will be initiated.
18	RW	0h	USB	MMP_PFET_REQ_OVRD This bit will disable the MMP PFET request condition for PGCB control. 1 – MMP PFET Request Ignored 0 – Default
17:16	RW	1h	USB	PGCB Clock Gate Request to PGCB Sleep: cfg_tclkgate[1:0] Value representing the minimum number of delay clocks required between the assertion of "pgcb_ip_clkgate_b" to the deassertion of "pgcb_sleep" on PG exit. (This is only applicable for IP-Accessible PG with state-retention enabled.) Please see the description of cfg_tsleepact for more details.
15:14	RW	1h	USB	PGCB Sleep Deassertion to PGCB ISM Unlock Req: cfg_tsleepinactiv[1:0] For IP-Accessible PG (with state retention): Value representing the minimum number of delay clocks required between the deassertion of "pgcb_sleep" to the deassertion of "pgcb_ip_*_lock_req_b". For IP-Inaccessible PG (or with state-retention disabled): Value representing the minimum number of delay clocks required between the deassertion of "pgcb_sleep" to the deassertion of "pgcb_isol_en_b".
13:12	RW	1h	USB	PGCB Prim Reset Deassertion to PGCB Next State: cfg_tirstup[1:0] For IP-Accessible PG: Value representing the number of delay clocks required between the deassertion of "pgcb_force_prim_rst_b" to the assertion of "pgcb_ip_clkgate_req_b" (or the deassertion of "pgcb_ip_*_lock_req_b if state retention is disabled). For IP-Inaccessible PG: Value representing the number of delay clocks required between the deassertion of "pgcb_force_prim_rst_b" to the deassertion of "pgcb_pmc_save_req_b". Please see the description of cfg_tsleepact for more details.

Bit	Access	Default Value	RST/PWR	Description
11:10	RW	1h	USB	PGCB Side Reset Deassertion to PGCB Prim Reset Deassertion: cfg_tsiderstup[1:0] Value representing the number of delay clocks required between the deassertion of "pgcb_force_rst_b" to the deassertion of "pgcb_force_prim_rst_b". (This is only applicable for IP-Accessible PG.) Please see the description of cfg_tsleepact for more details.
9:8	RW	1h	USB	PGCB Latch Isolation High to PGCB Clock Ungate Request: cfg_tlatchen[1:0] Value representing the number of delay clocks required between the assertion of "pgcb_isol_latchen" to the deassertion of "pgcb_ip_clkgate_req_b". Please see the description of cfg_tsleepact for more details.
7:6	RW	1h	USB	PGCB Isolation Deassertion to PGCB Latch Isolation High Count: cfg_tdeisolate[1:0] Value representing the minimum number of delay clocks required between the deassertion of "pgcb_isol_en_b" to the assertion of "pgcb_isol_latchen". Please see the description of cfg_tsleepact for more details.
5:4	RW	1h	USB	PGCB Reset Assertion to PGCB Power Down Request Count: cfg_tresetact[1:0] For IP-Accessible PG (with state retention): Value representing the minimum number of delay clocks required between the assertion of "pgcb_force_prim_rst_b" (and "pgcb_force_rst_b") to the assertion of "pgcb_pmc_pg_req_b". For IP-Inaccessible PG (or with state-retention disabled): Value representing the minimum number of delay clocks required between the assertion of "pgcb_force_prim_rst_b" (and "pgcb_force_rst_b") to the assertion of "pgcb_sleep". Please see the description of cfg_tsleepact for more details.
3:2	RW	1h		PGCB Isolation Assertion to PGCB Reset Assertion Count: cfg_tisolate[1:0] Value representing the minimum number of delay clocks required between the assertion of "pgcb_isol_en_b" to the assertion of "pgcb_force_prim_rst_b" and "pgcb_force_rst_b". Please see the description of [1:0] for more details.

Bit	Access	Default Value	RST/PWR	Description
1:0	RW	1h	USB	PGCB Sleep Assertion to PGCB Isolation Enable Count: cfg_tsleepact[1:0] For IP-Accessible PG (with state retention): Value representing the minimum number of delay clocks required between the assertion of "pgcb_sleep" (and the deassertion of "pgcb_isol_latchen") to the assertion of "pgcb_isol_en_b". For IP-Inaccessible PG (or with state-retention disabled): Value representing the minimum number of delay clocks required between the deassertion of "pgcb_isol_latchen" to the assertion of "pgcb_isol_en_b", as well as the minimum number of delay clocks required between the assertion of "pgcb_sleep" to the assertion of "pgcb_pmc_pg_req_b". Common for all cfg_t* inputs: '00': 1 clock '01': 2 clocks '10': 8 clocks '11': 256 clocks For any of the cfg_t* inputs that an IP may feel are a don't-care and the IP does not feel they will be useful for post-silicon debug, the recommendation is to tie the input to 2'b01 (2 clocks). Otherwise, the inputs may be tied to another relevant value or connected to a configuration register. Note: These signals may only change while pgcb_pwrupidle is asserted, if pgcb_pwrupidle is deasserted it should be valid and stable. (It may change the same cycle that ip_pgcb_pg_rdy_req_b asserts.)

Table 239. DEVIDLECTRL – Device Idle Control Register

Address Offset:80AC-80AFh
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:4	RO	0h	USB	RESERVED
4	RO	0h	USB	Interrupt Request Capable (IRC): Set to '1' by HW if it is capable of generating an interrupt on command completion, else '0'.
3	RWC	1h	USB	RR: RestoreRequired. When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a '1'. This bit will be set on initial power up.
2	RW	0h	USB	DevIdle (DEVIDLE). SW sets this bit to '1' to move the function into the DevIdle state. Writing this bit to '0' will return the function to the fully active D0 state (D0i0)
1	RO	0h	USB	IR: Interrupt Request. SW sets this bit to '1' to ask for an interrupt to be generated on completion of the command. SW must clear or set this on each write to this register.

Bit	Access	Default Value	RST/PWR	Description
0	RO	0h	USB	CIP: Command-In-Progress. HW sets this bit on a 1->0 or 0->1 transition of bit [2]. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. When clear all the other bits in the register are valid and SW may write to any bit. If Interrupt Request bit [1] was set for the current command, HW may clear this bit before the interrupt has been made visible to SW, since when SW actually handles a particular interrupt is not visible to the HW. SW writes to this bit have no effect.

Table 240. HOST_CTRL_MISC_REG - Host Controller Misc Reg

Address Offset:80B0-80B3h
Default: 0h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31	RW	0h	USB	Reserved
30	RW	0h	USB	USB2 Line State Debounce During Port Reset Policy This register controls how the debounce is enforced during the Port Reset phase. 0 – do not enable the line state debounce during port reset. 1 – enable the line state debounce during port reset.
29	RW	0h	USB	TTE PEXE Credit Fix Disable When set, it disables a fix implemented to re-deem PEXE credits when a port is disconnected.
28	RW	0h	USB	TTE Scheduling Policy This register controls a fix made to prevent over-scheduling by not account for 188B in each uFrame. Setting this bit will disable the fix and allow for over-scheduling.
27	RW	0h	USB	USB3 ITP Delta Timer Source Select This register selects the source for the delta timer tracking used for ITP generation. 0 – the source is a 16.666 ns tick generated from a crystal reference clock 1 - the source is a 16.666 ns tick generated from the aux_cclk. This field needs to remain in sync with Frame Timer Source Select to ensure the are both set or both cleared. There is no support for any other combination.
26	RW	0h	USB	Frame Timer Source Select This register controls the source for the frame timer. 0 – the source for the frame timer is a crystal reference clock 1 – the source for the frame timer is the aux_cclk.
25	RW	0h	USB	uFrame Masking Enable If set, enables the uFrame tick to be masked due to ports being in U3/NC. This controls a fix made to disable the auto masking of uFrame tick due to port state w/o any pipeline idle condition. When cleared, we rely on gating of frame timer due to proper port state and idleness tracking from the pipeline.
24	RW	0h	USB	Late FID Check Disable This register disables the Late FID Check performed when starting an ISOCH stream.

Bit	Access	Default Value	RST/PWR	Description
23	RW	0h	USB	Alarm Set Flag Disable 0: Scheduler performing its "first-round" check on periodic endpoints will assert this flag if an alarm is set. If this flag is asserted, then the Scheduler will be allowed to set the nfirst flag for endpoints in the "second-round" check of periodic endpoints. This prevents a race condition where no wakeup alarm is set in the first round for a new endpoint and then the disable PLL shutdown signal is cleared in the second round due to the setting of nfirst. This would only happen if there was one periodic endpoint and only for new doorbell rings that result in the unmask array bit being set in the proximity of the transition between the first-round and the second-round. 1: (Chicken-bit operation) The flag is disabled Note: This bit was created for COE HSD 4796077.
22	RW	0h	USB	Polling Doorbell Rang Disable 0: Polling State Machine will not move on from Bulk/ Control Endpoint until a DMA transfer is reported by the TRM. Polling State Machine behaves as if the Doorbell is still asserted. This prevents a TD consisting of a single Link TRB from consuming the scheduling opportunity for a NAK'd/NYET Endpoint after a new Doorbell and thus never waking the Link for the Doorbell. 1: (Chicken-bit operation) The flag is disabled. Note: This bit was created for COE HSD 4547808.
21	RW	0h	USB	ERDY Flag Disable 0: An ERDY received on any Interrupt Endpoint will force the backbone clock high until the next µframe to allow that Endpoint's TRM Pending Mask to be cleared. 1: (Chicken-bit operation) The flag is disabled. Note: This bit was created for COE HSD 4903177 for CHV/ANS/SPTLP.
20	RW	0h	USB	Reserved
19	RW	0h	USB	USB2 Resume Cx Inhibit Disable Controls if USB2 L1 Resume is allowed to contribute to "DMA Active" which will inhibit Cx state. 0 – USB2 L1 Resume is allowed to inhibit Cx via "DMA Active" 1 – USB2 L1 Resume is NOT allowed to inhibit Cx via "DMA Active" When cleared, Cx will only be inhibited when the DMA traffic for the port begins.
18:16	RW	1h	USB	Extra uFrame This register controls the extra number of uFrames added onto the advancing of late FID check.
15:0	RW	37Fh (895d)	USB	Valid Isoch Scheduling Range This register defines the window in miliseconds from the current Frame that will be considered for scheduling in an upcoming Frame. Anything scheduled outside of this window will be considered as late and will trigger the Missed Service Error.

Table 241. HOST_CTRL_MISC_REG2 - Host Controller Misc Reg2

Address Offset:80B4-80B7h
Default: 0h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:29	RW	0h	USB	RESERVED

Bit	Access	Default Value	RST/PWR	Description
28	RW	0h	USB	Disable Scheduler FrameID check – New policy to enable/ disable Scheduler's FrameID check capability. This mode is added as a part of adding CFC=1 capability. 0 – Enable Scheduler FrameID check 1 – Disable Scheduler FrameID check Note, this policy is only supported by the version of the controller that supports CFC=1 capability. Also, this policy should only be used when CFC=1 is enabled.
27:0	RW	0h	USB	RESERVED

Table 242. SSPE – Super Speed Port Enable

Address Offset:80B8-80BBh

Default Value:0h

Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:2	RO	0h	USB	RESERVED
1:0	RW	1h	USB	USB3 Port Enable This field controls whether SuperSpeed capability is enabled for a given USB3 port. When set to 1, Enables SS termination Enables PORTSC to to see the connects on the ports. When set to 0, Disables SS termination Blocks PORTSC from reporting attach/connect. Places port in the lowest power state.

Table 243. SSPITPE – Super Speed Port ITP Enable

Address Offset:80BC-80BFh
Default Value:0h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:2	RO	0h	USBUSB	RESERVED
1:0	RW	All 1's	USB	ITP Transmit Enable Width is scaled with USB3 Port Count

Table 244. AUX_CTRL_REG - AUX Reset Control

Address Offset:80C0-80C3h
Default Value:015FC0F0h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31	WO	0h	USB	This allows software to fire a reset that is equivalent to fundamental reset. Using this bit should only be for debug/test purpose. 1: normal 0: asserted one fundamental reset

Bit	Access	Default Value	RST/PWR	Description
30	RW	0h	USB	This will enable hc_rst to complete when OC is detected on a Port 0: Fix is enabled (Default) 1: Fix is Disabled
29	RW	0h	USB	This bit enables AUX reset control module to assert the pcie_phy_reset either from PIPE reset or from Aux power up reset only. The pcie_phy_reset is an internal signal for CB PHY only. 1: PIPE PHY reset 0: Aux PowerUp Reset
28	RW	0h	USB	This bit enables the AUX PM control module to assert mac_phy_powerdown state to P1 as soon as PERST# is deasserted. If disabled, then the AUX PM control state will follow its nature cause to determine the power down states for PIPE. 1: enabled 0: disabled
27	RW	0h	USB	This bit enables the internal reset control module to immediately start a reset assertion process when PERST# is deasserted without waiting for PCIe device is out of D3 state. This is for warm reboot only. The PERST# can still have impact as a reset if the xHC is in D3 and allow PERST# as a powerup reset bit set. 1: enabled PERST# as an immediately reset 0: disabled
26	RW	0h	USB	This bit disables the PERST# to cause an internal reset. 1: disabled the PERST# 0: enabled
25	RW	0h	USB	This bit enables a speed up function or AUX reset at startup. Normally we wait for 20ms after AUX power level has reached. When in speed up mode, we wait only around 3-4us. 1: enabled for fast sim 0: disabled
24	RW	1h	USB	When set to 1 ignore a port reset that is caused by a USBport link went down.
23	RW	0h	USB	When set to 1 ignore main powerup reset to USB PHY PIPE reset
22	RW	1h	USB	When set to '1' allow software to fire a cold reset to USB port logic
21	RW	0h	USB	When set to '1' ignore HC reset to reset the USB2 Port logic
20	RW	1h	USB	When set to '1' ignore HC reset to the USB PHY power-on reset
19	RW	1h	USB	When set to '1' enable the HC liked reset caused by PCIe link down condition detected. If PCIe link down detected, a link down reset will always be fired to PCIe core.
18	RW	1h	USB	When set to '1' enable EEPROM reload on every main power-up
17	RW	1h	USB	When set to '1' ignore HC reset to the PCIe PHY PIPE reset
16	RW	1h	USB	When set to '1' ignore the LTSSM of USB link state transition caused reset to USB PHY PIPE reset
15	RW	1h	USB	When set to '1' ignore warm reset of the portSC to the USB PHY power on reset
14	RW	1h	USB	When set to '1' allow PCIe link down to cause a reset to the rest of the core as the HC reset would.
13	RW	0h	USB	When set to '1' ignore hot reset to the USB3 port logic
12	RW	0h	USB	When set to '1' ignore warm reset to the USB3 port logic
11	RW	0h	USB	When set to '1' ignore main power up reset to USB3 port logic
10	RW	0h	USB	When set to '1' ignore main power up reset to USB2 port logic
9	RW	0h	USB	When set to '1' ignore main power up reset to PCIe core
8	RW	0h	USB	When set to '1' ignore main power up reset to PCIe PHY
7	RW	1h	USB	When set to '1' ignore HC reset to the USB PHY
6	RW	1h	USB	When set to '1' ignore warm reset to the USB PHY
5	RW	1h	USB	When set to `1`, it enables the reset isolation function that we have added during HC reset or Per port reset.

Bit	Access	Default Value	RST/PWR	Description
4	RW	1h	USB	When set to '1' allow main power off condition to trigger a main power domain reset
3	RW	0h	USB	When set to '1' ignore waiting for PERST# deassertion during main power show down.
2	RW	0h	USB	When fundamental reset is asserted during AUX power up, if this bit is set, then we will ignore PERST# such that purely wait for timeout to deassert fundamental reset.
1	RW	0h	USB	Indicates a fundamental reset 0: no reset
0	WO	0h	USB	Write 1 to this register will cause a fundamental reset if the bit1 is also written to 1

Table 245. HOST_BW_OV_SS_REG - Super Speed Bandwidth Overload

Address Offset:80C4-80C7h
Default Value:004A4008h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	0h	USB	RESERVED
23:12	RW	4A4h	USB	Max. TT BW allowed. see white paper
11:0	RW	8h	USB	BW calculation: Overhead per packet for SS BW calculations. see white paper.

Table 246. HOST_BW_OV_HS_REG - High Speed TT Bandwidth Overload

Address Offset:80C8-80CBh
Default Value:0001A01Fh
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	0h	USB	RESERVED
23:12	RW	01Ah	USB	BW calculation: Overhead per packet for HS-TT BW calculations. see white paper.
11:0	RW	01Fh	USB	BW calculation: Overhead per packet for HS BW calculations. see white paper.

Table 247. HOST_BW_OV_FS_LS_REG - Bandwidth Overload Full Low Speed

Address Offset:80CC-80CFh
Default Value:00014080h
Access: RW;
Size:33 bits

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	0h	USB	RESERVED
23:12	RW	14h	USB	BW calculation: Overhead per packet for FS BW calculations. see white paper.
11:0	RW	080h	USB	BW calculation: Overhead per packet for LS BW calculations. see white paper.

Table 248. HOST_BW_OV_SYS_REG - System Bandwidth Overload

Address Offset:80D0-80D3h
Default Value:00032010h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	0h	USB	RESERVED
23:12	RW	32h	USB	BW calculation: Overhead per TT packet for System BW calculations. see white paper.

Bit	Access	Default Value	RST/PWR	Description
11:0	RW	10h	USB	BW calculation: Overhead per packet for System BW calculations. see white paper.

Table 249. HOST_CTRL_SCH_ASYNC_DELAY_REG - Scheduler Async Delay

Address Offset:80D4-80D7h
Default Value:00000000h
Access: RW;
Size:32 bits
Global defaults for inserting delays between packets in the scheduler for async. types.

Bit	Access	Default Value	RST/PWR	Description
31:20	RO	0h	USB	RESERVED
19	RW	0h	USB	High-Speed Bulk Delay Enable
18:16	RW	0h	USB	High-Speed Bulk Delay Default (0=125us,1=250us,2=500us,3=1ms,…)
15	RW	0h	USB	Full-Speed Bulk Delay Enable
14:12	RW	0h	USB	Full-Speed Bulk Delay Default (0=125us,1=250us,2=500us,3=1ms,…)
11	RW	0h	USB	High-Speed Control Delay Enable
10:8	RW	0h	USB	High-Speed Control Delay Default (0=125us,1=250us,2=500us,3=1ms,…)
7	RW	0h	USB	Full-Speed Control Delay Enable
6:4	RW	0h	USB	Full-Speed Control Default (0=125us,1=250us,2=500us,3=1ms,…)
3	RW	0h	USB	Low-Speed Control Delay Enable
2:0	RW	0h	USB	Low-Speed Control Delay Default (0=125us,1=250us,2=500us,3=1ms,…)

Table 250. DUAL_ROLE_CFG Dual Role Configuration Register

Address Offset:80D8-80DBh
Access: RW;
Size:32 bits
Device Mode control.
All bits in this register must be in the Always ON Power domain (ungated USB or AON – as appropriate)

Bit	Access	Default Value	RST/PWR	Description
31:16	RW	0h	USB	Rsvd1 (Rsvd1):
22	RW	0h	USB	0 – enable PIPE RX term switch on idpin. During the connection to a device, there may be a delay in DRD switch from XDCI to XHCI mode,the rx term can be low after idpin deasserts. If this bit is 0, the rx term will be assert immediately after idpin toggle. Otherwise, the device may fall back to USB2 mode. 1 -- drive 0s on utmi rx signals to controller if not connected.
21	RW	1h	USB	0 – enable the utmi rx signal broadcast to both host and device 1 -- drive 0s on utmi rx signals to controller if not connected.
20	RW	0h	USB	0 – enable the rx signal broadcast to both host and device 1 -- drive 0s on rx signals to controller if not connected.
19	RW	0h	USB	reserved
18	RW	0h	USB	0 – ignore the SS gasket port sharing on device port 1 – use the SS gasket port sharing
17	RW	0h	USB	0 – enable the direct DRD switch on USB3 port by idpin 1 – disable the direct DRD switch
16	RW	0h	USB	reserved
15	RW	0h	USB	Rsvd2 (Rsvd2)
14:3	RW	100h	USB	ID ping debounce timer (DEBOUNCE_VAL): in the unit of RTC clock (33us) default to 8.448 ms
2	RW	0h	USB	Rsvd1 (Rsvd1)

Bit	Access	Default Value	RST/PWR	Description
1:0	RW	0h	USB	DRD switch mode (DRD_CONFIG): 00 – Dynamic DRD switch mode 01 – static mode 10 – static mode 11 -- reserved

Table 251. AUX_CTRL_REG1 - AUX Power Management Control

Address Offset:80E0-80E3h
Default Value:808DBCA0h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31	RW	1h	USB	D3 Hot function enable register. This bit is from pin input which is set "1". But we allow software to alter it if it is needed. 1: D3 hot enabled 0: D3 hot not abled.
30	RW	0h	USB	This bit enables the gate-off the core clock when AUX PM control is in low power state. 1: enabled to gate off the core clock 0: disable this function
29	RW	0h	USB	This bit is there for a bug fix where we need to ensure that phystatus did not get lost during the rate change where clock switch logic takes some cycles to complete such that the PCie;s core clock is at half of the PCIe PHY pclk. 1: extended phystatus assertion 0: not extended phystatus
28	RW	0h	USB	Disable the overwrite function in AUX PM control module for its initiated rate change. 1: AUX PM control module will not alter the PCIe rate change function . 0: allows AUX PM control module to initiate its PCIE rate change when it needs to enable P2 overwrite P1 function.
27	RW	0h	USB	Enable AUX reset module to treat every PERST# as a foundamental reset 1: enabled 0: disabled
26	RW	0h	USB	This is a test/control bit. This bit is designed to control the lowest powerdown state of the PCIe that AUX PM module signaled to PIPE is P1. 1: always drive to P1 instead of P2 0: drive as normal operation
25	RW	0h	USB	When set to 1 set the SSV flag.
24	RW	0h	USB	When set to 1 clear the SSV flag
23	RW	1h	USB	A debug control bit which is used to enable save&restore function. 1: enabled 0: disabled
22	RW	0h	USB	Reserved
21	RW	0h	USB	This bit sets the internal save_restore_enable flag to 0 when written to 1. Software is expected to clear this bit after it wrote this bit to 1. This is for test/debug purpose of the save&restore function. 1: clear the internal flag save_restore_enable 0: allows regular save&restore function to proceed.
20	RW	0h	USB	reserved
19:18	RW	3h	USB	Controls the drive strength of the IO buffer
17	RW	0h	USB	This bit enable USB port P2 overwrite
16	RW	1h	USB	1: Disable USB3 port clock gating 0: Enable USB3 port clock gating
15	RW	1h	USB	1: Enable P3 mode in RxDetect 0: Disable P3 mode in RxDetect
14	RW	0h	USB	1: Enable USB3 PIPE reset when out of P3 mode 0: Disable USB3 PIPE reset when out of P3 mode

Bit	Access	Default Value	RST/PWR	Description
13	RW	1h	USB	This bit enables the AUX PM control state machine to take over txelecidle signal of the PIPE during several special conditions. 1: Allow mask to mac_phy_txeleidle of PCIe core. 0: Disable the mask
12	RW	1h	USB	This bit enables the PCIe status function. 1: xHC as a PCIe device will generate the PME message. 0: xHC as a PCIe device will not generate any PME nor report PME status.
11	RW	1h	USB	When set to '1' enable isolation function for dual power zone.
10	RW	1h	USB	This bit allows the AUX PM control module to decide whether we entered into P2 overwrite condition based on the power down state of the PCIe core is at P1 or the LTSSM of PCIe core is in L1. What we used to have is based on P1 of the PCIe core mac_phy_powerdown signal. This is not correct because LTSSM can be in RX detect to result a P1 of power down state. To preserve our old function, we add this chicken bit. 1: P2OverWrite function based on LTSSM in L1 0: P2Pverwrite function based on PCIe core PIPE mac_phy_powerdown is in P1.
9	RW	0h	USB	When set to '1' disable core clock gating based on low power state entered
8	RW	0h	USB	When set to '1' enable PHY status timeout function which is designed to cover the PCIePHY issue that we may have not able to detect the PHY status toggle. This is a safety feature in case we have gotten into a deadlock during PHY status acknowledgement.
7	RW	1h	USB	When set to '1' ignore the aux_pm_en reg from PCIe core to continue the remote wake/clock switching support
6	RW	0h	USB	When set to '1' enable P2 overwrite P1 when PCIe core has indicated the transition from P0 to P1. This is to enable entering the even lower power state.
5	RW	1h	USB	When set 1 '1' enable the remote wake function by allowing P2 clock/switching and P2 entering
4:1	RW	0h	USB	Forced PM state
0	WO	0h	USB	When set to '1' force PM state to go to the state indicated in bit 4:1

Table 252. HOST_CTRL_WATERMARK_REG - Port Watermark

Address Offset:80E8-80EBh
Default Value:00800080h
Access: ;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RW	80h	USB	RBUF water mark
15:0	RW	80h	USB	XBUF water mark

Table 253. HOST_CTRL_PORT_LINK_REG - SuperSpeed Port Link Control

Address Offset:80EC-80EFh
Default Value:18010000h
Access: RW;

Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:27	RW	3h	USB	When bit 26 is set to 1, this field indicates LTSSM state to be forced for test mode.When bit 26 is set to 0, this field is overloaded for normal operation mode. Bit 31 indicates polarity check mode 0: Only the 8th consecutive TS1/TS2 1: Any TS1/TS2 Bit 30 indicates TS2 link function check mode 0: Only the 8th consecutive TS2 1: Any TS2 Bit 29 indicates TS2 scrambler disable TX mode 0: do not return scrambler disable bit from RX 1: return scrambler disable bit from RX
26	RW	0h	USB	0: Normal operation mode 1: Direct link to a specific state specified by bit 31:27 This bit is for test purpose only. It shall be written 0 in normal operation mode.
25	RW	0h	USB	0: Normal operation mode 1: Direct link to U0 This bit is for test purpose only. It shall be written 0 in normal operation mode.
24:21	RW	0h	USB	Compliance pattern to be forced to enter compliance mode This value is for test purpose only.
20	RW	0h	USB	0: Disable link error slave count 1: Enable link error slave count
19	RW	0h	USB	1: enable TS receive to complete U1/U2/U3 exit LFPS handshake 0: disable TS receive to complete U1/U2/U3 exit LFPS handshake
18	RW	0h	USB	1: enable logic idle receive to exit Polling.Configuration and Recovery.Configuration 0: disable logic idle receive to exit Polling.Configuration and Recovery.Configuration
17	RW	0h	USB	This bit specifies the port initialization timeout value. 1: 20us – 21us 0: 19us – 20us
16:15	RW	2h	USB	This field defines the latency to drive the PHY to enter low power mode 0: 4 cycles 1: 8 cycles 2: 16 cycles 3: 32 cycles
14:12	RW	0h	USB	This value defines the minimum time for the link to stay in Recovery.Active other than from U3. The granuity is 128us.
11:9	RW	0h	USB	This value defines the minimum time for the link to stay in Polling.Active and Recovery.Active from U3. The granuity is 128us.
8	RW	0h	USB	0: Normal operation mode 1: Force link to accept power management command
7	RW	0h	USB	0: Normal operation mode 1: Direct link to Recovery from U0
6	RW	0h	USB	0: Normal operation mode 1: Link fast training mode This bit should be written 0 in normal operation.
5	RW	0h	USB	0: Enable link scrambler 1: Disable link scramber
4	RW	0h	USB	0: Normal operation mode 1: Direct link to U3 from U0 This bit is for test purpose only. It shall be written 0 in normal operation mode.
3	RW	0h	USB	0: Normal operation mode 1: Direct link to U2 from U0 This bit is for test purpose only. It shall be written 0 in normal operation mode.
2	RW	0h	USB	0: Normal operation mode 1: Direct link to U1 from U0 This bit is for test purpose only. It shall be written 0 in normal operation mode.

Bit	Access	Default Value	RST/PWR	Description
1	RW	0h	USB	0: Disable link loopback master mode 1: Enable link loopback master mode
0	RW	0h	USB	0: Enable link compliance mode 1: Disable link compliance mode

Table 254. USB2_LINK_MGR_CTRL_REG1 - USB2 Port Link Control 1, 2, 3, 4

Address Offset:80F0-80FFh
Default Value:See Below. Note: The default value can be different based on different configuration of this design
Access: RW;
Size:128 bits
These set of registers is used to control USB set of timers. They are spread over 4 registers each 32 bits wide.

Bit	Access	Default Value	RST/PWR	Description
127: 125	RO	0h	USB	RESERVED
124:123	RW	0h	USB	additional guardband for L1 advance prewake. 00 = +0 us 01 = +1uF 10 = +2uF 11=+4uF
122	RW	0h	USB	select L1 min idle duration that will be driven to Scheduler. Either drive '0' or based on L1 Timeout value
121	RW	0h	USB	Enable periodic_prewake to prevent L1 entry if in U0, or wake from L1 if already in U2.
119:118	RO	0h	USB	RESERVED
117: 105	RW	40h	USB	#of microseconds after detecting U2 remote wake condition to reflect K
104: 92	RW	3Fh	USB	# of microseconds after entering U2, linestate changes are ignored as bus settles
91: 79	RW	10CBh	USB	# of microseconds after entering U3, linestate changes are ignored as bus settles
78: 63	RW	D6D7h	USB	# of microseconds for total reset duration
63: 50	RW	31h	USB	# of microseconds of Chirp-K to register that a device is chirping
49: 37	RW	31h	USB	# of microseconds of K/J in disconnected state to register connect has occurred.
36: 24	RW	31h	USB	# of microseconds of SE0 in FS/LS mode to register disconnect had occurred.
23:21	RW	0h	USB	Reserved
20	RW	1h	USB	Mode for extended L1 Exit recovery delay: 0: 12us 1: 50us
19	RW	1h	USB	Mode select for L1 Timeout increments: 0: time out increments are in 125us 1: L1 Timeout increments are in 256us. Refer to USB2 PORTHLPMC.L1 Timeout in XHCI Spec for additional details
18	RW	0h	USB	Reserved
17	RW	0h	USB	0: Detect minimal packet EOP. 1: Detect nominal packet EOP.
16	RW	0h	USB	0: Normal 1: Force full speed on host ports (disable chirp response)
15	RW	0h	USB	0: Enforce 192 byte limit on complete-split INs. Treat any packet > 192 as babble case. 1: Disable 192 byte limit check.
14	RW	0h	USB	0: Internal FS/LS Disconnect from linestate[1:0] 1: External provided FS/LS Disconnect from hostdisconnect input
13:12	RW	0h	USB	Select UTMI Reset Source (FRD UTMI Reset Only) 00: HCReset or Force PHY Reset or {internal reset after disconnect/suspend for restart} (default) 01,11: UTMI reset = ~UTMI suspendm 10: UTMI reset = ~UTMI suspendm & synchronization to port clk.
11	RW	0h	USB	1: Enable HS Disconnect Window Function 0: Disable HS Disconnect Window Function
10	RW	0h	USB	0: Enable Port Error Detection (default) 1: Disable Port Error Detection
9	RW	1h	USB	0: Enable Peek function for ISO-OUT (default) 1: Disable Peek function for ISO-OUT

Bit	Access	Default Value	RST/PWR	Description
8	RW	1h	USB	0: Drive Resume-K on parallel Interface 1: Drive Resume-K directly on FS/LS Serial Interface (default)
7	RW	1h	USB	0: Disable Drop-Ping Function in USB2 Protocol (default) 1: Enable Drop-Ping Function in USB2 Protocol
6	RW	0h	USB	0: Disable Force-Ping Function in USB2 Protocol (default) 1: Enable Force-Ping Function in USB2 Protocol
5	RW	1h	USB	0: Disable Auto-Ping Function 1: Enable Auto-Ping Function in USB2 Protocol (default)
4	RW	0h	USB	0: PHY is suspend=U3,U2,disconnect (default) 1: Disable PHY SuspendM in All States
3	RW	0h	USB	0: Normal operation (internal clock gated in U2,U3,disconnect) 1: UTMI Internal Clock Gate Disable
2	RW	0h	USB	0: PHY is suspendM=0 in Disconnect State (default) 1: Disable PHY SuspendM in Disconnect State
1	RW	0h	USB	0: Normal Operation (default) 1: Force PHY Reset
0	RW	0h	USB	0: Normal Operation (default – FPGA/ASIC) 1: USB2 Accelerated Simulation Timing (default – simulation)

Table 255. HOST_CTRL_BW_CTRL_REG - HOST CONTROLLER BW CONTROL REG

Address Offset:8100-8103h
Default Value:8008h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	0h	USB	Reserved
15:0	RW	8008h	USB	Reserved

Table 256. FPGA_REV_REG – FPGA Revision Register

Address Offset:8104-8107h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31: 0	RO	11000000h	USB	FPGA Revision This field demarks the FPGA Revision Number. This is managed through the FPGA Revision Define.

Table 257. HOST_IF CTRL_REG - HOST_IF_CTRL_REG

Address Offset:8108-810Bh
Default Value:01h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31	RW	0h	USB	Enable SW update to HW Slot Table Setting this bit will unlock the HW Slot Table contents (like Slot Table, rd/wr pointers of Slot Table, and Slot En state array)
30:2	RO	0h	USB	Rsvd1 (Rsvd1):
1	RW	0h	USB	HC Halt Timeout Enable Enables the HC halt flow to time-out after 15 ms.
0	RW	1h	USB	Host IF (HOSTIF):

Table 258. HOST_BW_OV_BURST_REG – BANDWIDTH OVERLOAD BURST

Address Offset:810C-810Fh
Default Value:00008020h
Access: RW;

Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	0h	USB	RESERVED
23:12	RW	08h	USB	BW calculation: Overhead per burst for system BW calculations. see white paper.
11:0	RW	20h	USB	BW calculation: Overhead per burst for SS BW calculations. see white paper.

Table 259. HOST_CTRL_TRM_REG2 – Host Controller Transfer Manager Control 2

Address Offset:8110-8113h
Default Value:F0EC838Ch
Access: RW;
Size:32 bits
This register contains fields which control the behavior of the Transfer Manager in the XHC.

Bit	Access	Default Value	RST/PWR	Description
31	RW	1h	USB	This bit is added for bug FR2601. It is for cache invalidate case where xHC engine needs to insert wait states for completion engine when the completion has received a short packet before XFER engine has finished the TRB fetch for this packet at its packet boundary. 1: enables the feature 0: disabled
30	RW	1h	USB	This bit is added for bug FR2642. It is to delay the completion engine to generate an event due to internal error conditions that halted an EP until XFER engine has reached a packet boundary. 1: enabled 0: disabled
29	RW	1h	USB	This bit is added for bug FR2639. It enables the internal functions where xHC engine needs to immediatedly serve the EP again. 1: enabled 0: disabled
28	RW	1h	USB	This bit is added for bug FR2495. It enables that error completion code of the first error condition detected within an TD so that we can report the same error completion codes for all other TRBs within this TD. 1: enables the feature 0: disabled
27	RW	0h	USB	This bit disables a new feature where xHC engine will have an ODMA FIFO added for the commands between TRM and ODMA so that we can avoid the back-pressure situation due to the number of outstanding PCIe read limitation. This is for performance enhancement. 1: feature disabled 0: enabled
26	RW	0h	USB	This bit is added for bug FR2446. It is to enable TRM to only send one IN request for TTE 1st phase request even if it has not reached the packet boundary. 1: enabled 0: disabled
25	RW	0h	USB	This bit is added for bug FR2395. This disable the single IN EP for TTE function 1: only allow single IN EP per port for TTE 0: disabled
24	RW	0h	USB	This bit is added for bug FR2333 where the xHC engine has always ignored the credit returned from device for its OUT EP buffers when the EP is a periodic EP. 0: will enable the xHC engine to follow the flow control 1: will disable this feature
23	RW	1h	USB	This bit is added for bug FR2283. This is to ensure only 1 clear pulse generated when a completion has received. 1: enabled 0: disabled

Bit	Access	Default Value	RST/PWR	Description
22	RW	1h	USB	This bit enables a 2ms timeout for all TTE related EP stop endpoint command. The xHC engine will not check whether there is a pending response in context. It will only wait for 2ms and indicates that EP has been stopped. 1: enabled 0: disabled
21	RW	1h	USB	This bit enables xHC engine TRM to report the second or more events on an ISP flush on a second or more TRBs with ISP bit set that are flushed for a short packet response received. 1: enabled 0: disabled
20	RW	0h	USB	This bit enables a new feature where the completion engine of TRM can check the credit returned from remote device to not excced its max burst size. If it does, we will keep the internal credits in the context to the max burst size so that xHC engine will not transmit more than max burst size. Note: CB has this bit default set to 0 PPT B0 and LPT will have this bit set to 1. 1: disabled 0: enabled
19	RW	1h	USB	Enable MSI_CNT update once we hit current interval during advancing. The new MSI_CNT value is calculated based on current uFrame w.r.t current Frame based on EP's SI. Disabling this will make controller to advance till either of below condition is met – MSI_CNT reaches to 0 Hit Isoc TD with FrameID for future frame/SI 1 – Enable MSI_CNT update 0 – Disable MSI_CNT update Note, this policy is only supported by the version of the controller that supports CFC=1 capability. Also, this policy should only be used when CFC=1 is enabled.
18	RW	1h	USB	This bit enables the xHC engine to fully support the non-0 control EP. This bit allows the xHC TRM to keep track of on non-0 control EP per port so that the responses can be routed to the correct DMA engine. 1: enabled 0: disabled
17	RW	0h	USB	This bit enables xHC engine to evaluate the next TRB even if the EP is at the end of a TD. 1: enables the feature 0: disables the feature
16	RW	0h	USB	Setting this bit to '1' will force xHC engine to ring internal doorbell on the EP that it has just received response for.
15	RW	1h	USB	This bit enables a feature where xHC engine will skip a service interval when an Interrupt EP has missed its service interval. 1: enables to skip a service interval 0: disables this feature
14	RW	0h	USB	New feature added to prevent the back-pressure from ODMA due to the fact that it ran out of ODMA timeout timer resources. This is for performance enhancement. We have put into the ODMA credit is part of resource calculation before TRM allows the next scheduling for OUT EP. 1: enables this feature 0: Disables this feature

Bit	Access	Default Value	RST/PWR	Description
13	RW	0h	USB	The xHC engine has a feature that can check with Receive Port Credit per root port to whether or not allowed the next schedule onto this port. This is for performance enhancement. This bit enables this feature 1: Feature enabled 0: Feature disabled
12	RW	0h	USB	1: Disable the error reporting for a received stream ID value of 0x0000. 0: Report received stream ID of 0x0000 as an error Note: only used when an endpoint is configured for stream operation.
11	RW	0h	USB	Enable the host to transfer to the prime-pipe state (and transmit a prime pipe) on each transfer back to the IDLE state. 1: Feature enabled 0: Feature disabled Note: only used when an endpoint is configured for stream operation.
10	RW	0h	USB	Reserved
9	RW	1h	USB	1: enable the XFER engine to auto detecting a missing service interval function when there is a long delay such that we missed a service interval due to the pending response. 0: disable this function in XFER engine.
8	RW	1h	USB	1: enable the function to support 0length TTE second phase request from TTE module. 0: disable this function.
7	RW	1h	USB	1: enable a packet pace function under a special condition. This is an internal feature to XFER engine. It is not expected to be used other than default. 0: disable this function.
6	RW	0h	USB	1: assert the sch_req_incomplete signal in XFER engine when a context FC is ON. This is an internal safety feature for XFER engine. 0: not to have this function
5	RW	0h	USB	1: enable the address device command to query a port credit before it is executed in ODMA engine. 0: Disable this function.
4	RW	0h	USB	1: Enable XFER engine to use context empty flag not assert as a way of identifying a TTE overlap condition. 0: Enable XFER engine to use a no-pending response flag as a way of identifying a TTE overlap condition
3	RW	1h	USB	1: enable the context storage for a flag to identify a DMA request as a 1st of TD DMA request. 0: disable the context storage.
2	RW	1h	USB	1: enable the credit redeem when a port is in NC state. 0: Disable the credit redeem
1	RW	0h	USB	1: enable the function where XFER engine uses the remaining burst count as an indication that the next TRB on the transfer ring for an ISO TD is either link TRB or event data TRB. 0: Disable this non DMA TRB detect function
0	RW	0h	USB	1: enable XFER engine to process a reserved TRB type as a NO-OP TRB 0: report TRB ERR for reserved TRB type.

Table 260. Sierra Back Door Registers

Address Offset:8114-8127h
Default Value:See below
Access: RW;
Size:160 bits (5 DW registers)

Table 261. HOST_CTRL_BW_MAX_REG – Max BW control Reg 4

Address Offset:8128-8133h
Default Value:See below
Access: RW;

Size:64 bits

Bit	Access	Default Value	RST/PWR	Description
95:84	RO	0h	USB	Reserved
83:72	RW	93Fh	USB	Max. Number of BW units for SSP ports. (denominator in 90% calculation)
71:60	RW	F42h	USB	Max. Number of OUT BW units for PCIe ports. (denominator in 90% calculation)
59:48	RW	F42h	USB	Max. Number IN of BW units for PCIe (system interface) (denominator in 90% calculation)
47:36	RW	528h	USB	Max. Number of BW units for TIs. (denominator in 90% calculation)
35:24	RW	505h	USB	Max. Number of BW units for FS/LS ports. (denominator in 90% calculation)
23:12	RW	647h	USB	Max. Number of BW units for HS ports. (denominator in 80% calculation)
11:0	RW	F42h	USB	Max. Number of BW units for SS ports. (denominator in 90% calculation)

Table 262. USB2_PROTOCOL_GAP_TIMER_LOW_REG – USB2 Protocol Gap Timer LOW

Address Offset:8134-8137h
Default Value:See below
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:24	RW	12d	USB	GAP time after FS
23:16	RW	5d	USB	GAP time after HS RX
15:8	RW	20d	USB	GAP time after HS TX SOF
7:0	RW	12d	USB	GAP time HS TX Packet

Table 263. USB2_PROTOCOL_GAP_TIMER_HIGH_REG – USB2 Protocol Gap Timer HIGH

Address Offset:8138-813Bh
Default Value:See below
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	0	USB	Reserved
23:16	RW	12d	USB	GAP time after LS TX thru FS hub
15:8	RW	60d	USB	GAP time after LS RX thru FS hub
7:0	RW	100d	USB	GAP timer after LS

Table 264. USB2_BTO_CTRL_REG – USB2 Bus Timeout Control

Address Offset:813C-813Fh
Default Value:8D4258B8

Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description

31:22	RW	46A	USB	Bus timeout count for LS
				This value depended on whether this parameter USB2_PROTO_PROGRAMMBLE_DELAY is defined during synthesis.
				If USB2_PORT_CLK_60 is defined,
				{If USB2_PROTO_PPTLPT_DELAY is defined,
				Then the default value is : x46A,
				else x2DA,}
				Else
				{If USB2_PROTO_PPTLPT_DELAY is defined,
				Then the default value is : = x230
				else
				x172,}

21:11	RW	96	USB	Bus timeout count for FS
				This value depended on whether this parameter USB2_PROTO_PROGRAMMBLE_DELAY is defined during synthesis.
				If USB2_PORT_CLK_60 is defined,
				{If USB2_PROTO_PPTLPT_DELAY is defined,
				Then the default value is : x96,
				else
				x64,}
				Else
				{If USB2_PROTO_PPTLPT_DELAY is defined,
				Then the default value is : x50
				else
				x37}

10:0	RW	B8	USB	Bus timeout count for HS This value depended on whether this parameter USB2_PROTO_PROGRAMMBLE_DELAY is defined during synthesis. If USB2_PORT_CLK_60 is defined, 0xB8 Else 0x61

Table 265. HOST_IF_PWR_CTRL_REG0 - Power Scheduler Control 0

Address Offset:8140-8143h
Default Value:0A019132h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:24	RW	Ah	USB	Engine Idle Hysteresis (EIH): This register controls the min. idle span that has to be observed from the engine idle indicators before the power state flags (xhc_*_idle) will indicate a 1 (TBD units)
23:12	RW	19h	USB	Fabric PLL Shutdown Advance Wake (FPSAW): This register controls the time before the next scheduled transaction where the Fabric PLL request will assert. Register Format: Bits [11:7] # of 125us uframes Bits [6:0] # of microseconds (0-124) Note this field shall be set to a minimum of 4 us.
11:0	RW	132h	USB	Fabric PLL Shutdown Min. Idle Duration (FPSMID): The sum of this register plus the FPSAdvance Wake form to a Total Idle time. When the next scheduled periodic transaction is after present time + Total Idle, the Fabric PLL request will de-assert, allowing the PLL to shutdown, based upon relevant enabled EP types (see Alarm bit definitions below). Register Format: Bits [11:7] # of 125us uframes Bits [6:0] # of microseconds (0-124)

Table 266. HOST_IF_PWR_CTRL_REG1 - Power Scheduler Control 1

Address Offset:8144-8147h
Default Value:0000033Fh
Access: RW;
Size:32 bits
These bit enable by EP type those EPs classes that are considered for determining next periodic active interval for pre-wake of the periodic_active signal. EP classes that are disabled may never be observed in setting of the periodic_active signal.

Bit	Access	Default Value	RST/PWR	Description
31:20	RW	0h	USB	Rsvd1 (Rsvd1):
19	RW	0h	USB	Enhanced Engine IDLE 0: HSD 375274 fix is enabled. "Engine IDLE" is deasserted if the Scheduler State Machine is performing the Periodic walk. 1: Revert to previous behavior
18:15	RW	0h	USB	Rsvd1 (Rsvd1):
14	RW	0h	USB	Disable BELT Latch: 1: The Power Scheduler's interface to the LTR Manager signals BELT and No_Requirement are not latched with the Request signal and can change before Halt is deasserted. Asserting this bit will disable the fix from HSD LPTLP 375141. 0: The Power Scheduler's interface to the LTR Manager signals BELT and No_Requirement are latched when the Request signal is asserted and will remain latched until Halt is deasserted.
13	RW	0h	USB	LPM Prewake Naked Interrupt Enable 0: Ignore the Naked INTR for LPM. 1: Do not ignore the Naked INTR for LPM.
12	RW	0h	USB	LPM Prewake Interrupt Enable 11: Disable interrupt prewake for LPM. 01: Enable interrupt OUT prewake for LPM. 10: Enable interrupt IN prewake for LPM. 00: Enable both interrupt IN/OUT prewake for LPM.
11:10	RW	0h	USB	Engine Idle Hysteresis Scale Controls the Engine Idle Hysteresis scale. 0 - clock 1 - 1 us 2 - 125 us
9	RW	1h	USB	HS Interrupt OUT Alarm (HSIO):
8	RW	1h	USB	HS Interrupt IN Alarm (HSII): Note: This is required to be set to enable the functionality behind the PCICFG.HSCFG2.HSIIPAPC method of tracking HS Intr IN EP's for Periodic Active.
7	RW	0h	USB	SS Interrupt OUT Alarm (SSIO):
6	RW	0h	USB	SS Interrupt IN Alarm (SSII):
5	RW	1h	USB	SS Interrupt OUT and not in FC Frame Alarm (SSIO):
4	RW	1h	USB	SS Interrupt IN and not in FC Frame Alarm (SSII):
3	RW	1h	USB	HS ISO-OUT Alarm (SSOA):
2	RW	1h	USB	HS ISO-IN Alarm (SSIA):
1	RW	1h	USB	SS ISO-OUT Alarm (SSOA):
0	RW	1h	USB	SS ISO-IN Alarm (SSIA):

Table 267. AUX_CTRL_REG2 – Aux PM Control Register 2

Address Offset:8154-8157h
Default Value:81390206h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:28	RW	0h	USB	This bit disables the dependency on Wake Enables defined in PORTSC for L1P2 exit when in D0
30:28	RW	0h	USB	RESERVED

Bit	Access	Default Value	RST/PWR	Description
27:25	RW	0h	USB	Reserved
24	RW	1h	USB	This bit enables a L1 exit notification to SNPS PCIe core. There is a case where USB ports have waked up and AUX PM module has started the wakeup process. The AUX PM control state got into a wait for P0 state because it needs to wait until PCIe core to signal powerdown state change. Due to the fact that the core is in D3Hot, there is no run_stop bit set such that no internal interrupt will be fired. This causes the LTSSM of PCIe stayed in L1 even though AUX PM has known that it needs an L1 exit. This bit works together with bit21 of this register. 1: enables this feature 0: disables this feature.
23	RW	0h	USB	1: do not assert PLC for disconnection 0: assert PLC for disconnection
22	RW	0h	USB	This bit enables a feature in PCIe core LTSSM to treat IDLE received as TS2 when LTSSM is in wait for TS2 receive state. This is a function requested from PHY where it is possible to not able to receive TS2 without error. 1: treat Logic IDLE as TS2 received when in some PCIe LTSSM state. 0: disable this feature.
21	RW	1h	USB	We added a feature where if PCIe core LTSSM enters L1 due to the D3hot, the aux PM control will not start a P2 overwrite function in anticipating for the next L23 enter. 1: disables p2 overwrite due to the D3HOT where PCIe core enters the L1. 0: enables P2 overwrite even if we are in D3Hot.
20	RW	1h	USB	1: enables the port to enter U3 automatically when in U1/U2 0: disables the port to enter U3 automatically when in U1/U2
19	RW	1h	USB	1: No linkdown reset is issue during low power state
18	RW	0h	USB	This bit enables a feature in AUX PM module where if PCIe core LTSSM is in P0 for a duration of time, we will exit the deep sleep state. This is for failure control in case. 1: enables this feature 0: disable this feature
17	RW	0h	USB	This bit selects U2 exit LFPS timer value 0: 320ns – 400ns in 25MHz domain 1: 240ns – 320ns in 25MHz domain
16	RW	1h	USB	This bit enables a function that AUX PM module exits from the deep sleep state due to the USB ports wakeup level signal. We have added this feature where USB ports will generated a wakeup level signal to wakeup the AUX PM module if it is in deep sleep state and this level signal will be cleared if the change bits are updated by software. 1: enables this function 0: disables this function which means that a wakeup pulse generated from each USB PortSC event will wake up the AUX PM module from deep sleep if the D3 state is programmed.
15:14	RW	0h	USB	This field defines the timeout value to enter P3 mode in U2. 00: 7us – 8us 01: 511us – 512us 10: disables the timer (0us) 11: disables the timer (0us)
13	RW	0h	USB	1: enables PHY P3 mode in U2. 0: disables PHY P3 mode in U2.
12:11	RW	0h	USB	Reserved
10	RW	0h	USB	This bit enables a function that the SPNS PCIe core is controlled by xHCI engine internal periodic EP traffic conditions. 1: enables the xHC engine to request an exit of L1 when the service time has reached for an periodic EP. 0: disabled this function

Bit	Access	Default Value	RST/PWR	Description
9	RW	1h	USB	This bit selects the port status change event generation mode. 1: port status change event is blocked until all status change bit are cleared. 0: port status change event is only blocked by the individual status change bit.
8:4	RW	0h	USB	Reserved.
3	RW	0h	USB	This bit enables the AUX PM module to automatically wakeup from deep power down when engine has detected non-idle condition. 1: feature enabled 0: feature disabled
2	RW	1h	USB	This bit ensures the P1 drive during PERST#. 1: feature enabled 0: feature disabled
1	RW	1h	USB	This bit enables PCIe PCLK isolation function when in two power domain. 1: feature enabled 0: feature disabled
0	RW	0h	USB	This bit enables a feature where we can get P2 overwrite to automatically turned on when there is no pending traffic in the engine. Note: This bit may vary depending on the synthesis parameter selection. 1: feature enabled 0: feature disabled

Table 268. HOST_CTRL_SCH _REG - Host Control Scheduler 2

Address Offset:8160-8163h
Default Value:0h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:19	RO	0h	USB	Rsvd1 (Rsvd1):
18:0	RW	0h	USB	Reserved for future use

Table 269. USB2PHYPM – USB2 Phy Power Management Control

Address Offset:0x8164 – 0x8167
Default Value:0x0000_0000
Access: RW; RO
Size: 32bits

Bit	Access	Default Value	RST/PWR	Description
31:8	RO	0	NA	Reserved
7	RW	1	USB	Enable Command Manager Active indication for Tx/Rx Bias circuit HS Phy PM Policy
6	RW	1	USB	Enable TTE Active indication for Tx/Rx Bias circuit HS Phy PM Policy
5	RW	1	USB	Enable IDMA Active indication for Tx/Rx Bias circuit HS Phy PM Policy
4	RW	1	USB	Enable ODMA Active indication for Tx/Rx Bias circuit HS Phy PM Policy
3	RW	1	USB	Enable Transfer Manager Active indication for Tx/Rx Bias circuit HS Phy PM Policy
2	RW	1	USB	Enable Scheduler Active indication for Tx/Rx Bias circuit HS Phy PM Policy

Bit	Access	Default Value	RST/PWR	Description
1	RW	0	USB	Enable Rx Bias ckt disable When set enables the Rx bias ckt to be disabled when conditions met (as described by the HS phy PM policy bits)
0	RW	0	USB	Enable Tx Bias ckt disable When set enables the Tx bias ckt to be disabled when conditions met (as described by the HS phy PM policy bits)

Table 270. USB2PHYPM2 – USB2 Phy Power Management Control 2

Address Offset:0x8168 – 0x816B
Default Value:0x0002_82EE
Access: RW; RO
Size: 32bits

Bit	Access	Default Value	RST/PWR	Description
31:21	RO	0	USB	Reserved
20:15	RW	5h	USB	Tx/Rx Off Min Time: Minimum number of clocks (uclk60x) for which Tx/Rx shall be switched off. This is used to decide if bias circuits can be switched off in the current micro-frame ahead of the next Tx/Rx.
14:7	RW	5h	USB	Tx/Rx Off Wait time: Guardband time in number of clocks (uclk60x) before which Tx/Rx can be turned off when there is no activity
6:0	RW	6Eh	USB	Tx/Rx Pre Tx on time: This is the time (in uclk60 clock periods) when Tx/Rx Bias needs to be turned on ahead of Transmit or Receive. This is based on the AFE requirement when bias needs to be ON before the transmit/receive occurs on the bus.

Table 271. AUXCLKCTL - xHCI Aux Clock Control Register

Address Offset:0x816C – 0x816F
Default Value:0x0000_0400
Access: RW; RO
Size: 32bits

Bit	Access	Default Value	RST/PWR	Description
31:21	RO	0	NA	Reserved
20	RW	0	USB	Port Reset Auto Complete when in Device Mode: This bit controls the release of warm rst_req_done immediately on reciept of req when in Device Mode 0: Auto Complete Port Reset 1: Wait for Port Reset on the wire for completion of Port Reset
19	RW	0	USB	USB3 Partition Engine/Link trunk gating Enable When set to '1' enables gating of the SOSC trunk to the XHCI engine/link in the PARUSB3 partition. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.

Bit	Access	Default Value	RST/PWR	Description
18	RW	0	USB	USB3 Partition Frame Timer trunk gating Enable When set to '1' enables gating of the SOSC trunk to the Frame Timer in the PARUSB3 partition. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
17	RW	0	USB	USB2 link partition clock gating enable When set to '1' enables gating of the SOSC trunk to the USB2 link and Phy logic in the PARUSB2 partition. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
16	RW	0	USB	USB2/USHIP 12.5 MHz partition clock gating enable When set to '1' enables gating of the 12.5 MHz SOSC trunk to the USB2 and USHIP logic in the PARUSB2 partition. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
15	RO	0	NA	Reserved
14	RW	0	USB	USB3 Port Aux/USB clock gating enable When set, allows the aux_cclk clock into the USB3 port to be gated when conditions are met. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
13:12	RW	0x0	USB	Rx Detect Timer when port Aux Clock is Gated This field defines the value of the timer used to perform Rx Detect when port Aux Clock has been gated. 0x0: 100ms 0x1: 12ms Others: Reserved Note: This timer shall use the Fast Training Timer Tick (about 1us tick) for simulation purposes. For Fast Training mode, the above timeouts will become about 11us and about 100us, +/- implementation uncertainty, respectively.
11:8	RW	0x4	USB	U2 Residency Before ModPHY Clock Gating Before gating ModPHY Aux clock, Host Controller shall wait for this time in U2. This time is meant to ensure that the attached device has entered U2 as well. 0x0: 1us 0x1: 128us 0x2: 256us 0x3: 512us 0x4: 640us 0x5: 768us 0x6: 896us 0x7: 1024us Others:Reserved Note: This counter shall start counting once pipe has entered PS3 state in response to link in U2.

Bit	Access	Default Value	RST/PWR	Description
7	RW	0	USB	Frame Timer Clock Gating Ports in U2 Enable (FTCGPU2E) This bit, when set, allows Host Controller to gate the clock to the Frame Timer when ports are in U2. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
6	RW	0	USB	USB2 port clock throttle enable When set, allows the Aux clock into the USB2 ports to be throttled when conditions allow. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
5	RW	0	USB	XHCI Engine Aux clock gating enable When set, allows the aux clock into the XHCI engine to be gated when idle. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
4	RW	0	USB	XHCI Aux PM block clock gating enable When set, allows the aux clock into the Aux PM block to be gated when idle. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
3	RW	0	USB	USB3 Aux Clock Trunk Gating Enable When set, allows Aux Clock Trunk feeding to USB3.0 ports to be gated when port Aux clock is gated at all USB3.0 ports and all USB3.0 modPHY instances. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
2	RW	0	USB	USB3 Port Aux/Port clock gating enable When set, allows the aux_pclk clock into the USB3 port to be gated when conditions are met. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
1	RW	0	USB	ModPHY port Aux clock gating enable in U2 When set, allows the aux clock into the ModPhy to be gated when Link is in U2 and pipe has been in PS3 for at least the time defined by U2 Residency Before ModPHY Clock Gating field. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.

Bit	Access	Default Value	RST/PWR	Description
0	RW	0	USB	ModPHY port Aux clock gating enable in Disconnected, U3 or Disabled When set, allows the aux clock into the ModPHY to be gated when Link is in Disconnected, U3 or Disabled state. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.

Table 272. USB2LPM – USB LPM Parameters

Address Offset:0x8170 – 0x8173
Default Value:0x0009_0032
Access: RW; RO
Size: 32bits

Bit	Access	Default Value	RST/PWR	Description
31:22	RO	0	USB	Reserved
21:19	RW	0b001	USB	Min U3 Exit LFPS Duration This field defines the minimum duration of LFPS driven by Host Controller upon U3 exit LFPS handshake. Note that there's an uncertainty of +-16us in actual duration driven by the Host Controller. 0b000:96us 0b001:160us 0b010:224us 0b011:288us 0b100:352us 0b101:416us 0b110:480us 0b111:544us
18:16	RW	0b001	USB	Min U2 Exit LFPS Duration This field defines the minimum duration of LFPS driven by Host Controller upon U2 exit LFPS handshake. Note that there's an uncertainty of +-16us in actual duration driven by the Host Controller. 0b000:96us 0b001:160us 0b010:224us 0b011:288us 0b100:352us 0b101:416us 0b110:480us 0b111:544us
15	RW	0	USB	Max PING LFPS Rx Detection This field defines the maximum timing for PING LFPS. If an incoming LFPS will be considered a PING if it has a timing such that it is less than or equal to the selected value. Otherwise it will be considered for the other types of LFPS. 0b – Max PING LFPS timing set to 256 ns (32 link clocks) 1b – Max PING LFPS timing set to 320 ns (40 link clocks)
14:10	RO	0	NA	Reserved

Bit	Access	Default Value	RST/PWR	Description
9:0	RW	032h	USB	xHCI BESL to HIRD Distance This field defines the gap between BESL and duration of Resume signalling from Host upon Host Initiated Resume from USB2.0 LPM. Default value of this register corresponds to xHCI spec defined 50us value. Value BESL to HIRD Distance 000h 0us 001h 1us 002h 2us : : : 3FFh 1023us

Table 273. XHCLTVCTL1 – XHCI Latency Tolerance Control 1

Address Offset:0x8174 – 0x8177
Default Value:0x0040_047D
Access: RW; RO
Size: 32bits

Bit	Access	Default Value	RST/PWR	Description
31	RW	0	USB	Disable scheduler direct transition from IDLE to NO requirement 0: (default) allow scheduler direct transition from IDLE to NO requirement 1: Disable scheduler direct transition from IDLE to NO requirement
30	RW	0b	USB	XHCI LTR Transition Policy (XLTRTP) When '0', the LTR messaging state machine transitions through High _ Med _ Low _ Active states assuming enough latency is available for each transition. When '1', LTR messaging state machine transitions from High, Medium, or Low LTR states to Active state upon the Alarm Timer timeout and stays in Active until the next service boundary.
29	RW	0b	USB	Include Scheduler First Round in Active Signal Disable 0: 'xHC Engine Idle' from the Power Scheduler will not assert if the Scheduler is performing its first round pass through periodic endpoints. 1: (Chicken bit) Revert to previous behavior. Scheduler's first round checks not included in 'xHC Engine Idle' equation.
28	RW	0b	USB	XHCI LTR Active Enable (XLTRAE) 0: The Power Scheduler will not request an LTR message on a transition to ACTIVE. 1: The Power Scheduler will request an LTR message on a transition to ACTIVE.
27	RW	0b	USB	Power Scheduler Local Clock Gating Enable (PWRLCGE) 0: Power Scheduler does not use local clock gating 1: Power Scheduler's local clock gating enabled. Note: This functionality is no longer required. This LCG existed previous to the inclusion of Aux clock gating.
26	RW	0b	USB	LTR EVM Hysteresis Max Count Power Scheduler's 'Periodic IDLE' residency before we assert 'Periodic Complete' 0: Hysteresis set to 127 clock ticks. (.64µs) 1: Hysteresis set to 31 clock ticks (.16µs)
25	RW	0b	USB	Reserved (for future ECO use).
24	RW	0b	USB	XHCI LTR Enable (XLTRE) This bit must be set to enable LTV messaging from XHCI to the PMC.

Bit	Access	Default Value	RST/PWR	Description
23:12	RW	400h	USB	Periodic Active LTV 23:22 Latency Scale 00b : Reserved 01b : Latency Value to be multiplied by 1024 10b : Latency Value to be multiplied by 32,768 11b : Latency Value to be multiplied by 1,048,576 21:12 Latency Value (ns) Defaults to 0µs
11:0	RW	47Dh	USB	USB2 Port L0 LTV 11:10 Latency Scale 00b : Reserved 01b : Latency Value to be multiplied by 1024 10b : Latency Value to be multiplied by 32,768 11b : Latency Value to be multiplied by 1,048,576 9:0 Latency Value (ns) Defaults to 128µs

Table 274. XHCLTVCTL2 – XHCI Latency Tolerance Control 2

Address Offset:0x8178 – 0x817B
Default Value:0x0000_17FF
Access: RW; RO
Size: 32bits

Bit	Access	Default Value	RST/PWR	Description
31:13	RO	0	NA	Reserved
12:0	RW	17FFh	USB	LTV Limit: This register defines a maximum LTR value that is allowed to be advertised to the PMC. This is meant to be used as a workaround or mitigation if issues are discovered with the LTR values generated by the XHC using the defined algorithms. If the LTR value of the XHC is larger than the value in this register field, the value in this field is sent to the PMC instead. Default value is the highest possible (101b) 12:10: Latency Multiplier Field 000b – Value times 1 ns 001b – Value times 32 ns 010b – Value times 1,024 ns 011b – Value times 32,768 ns 100b – Value times 1,048,576 ns 101b – Value times 33,554,432 ns 110b-111b – Not Permitted 9:0: Latency Value Default = 3FFh

Table 275. LTVHIT - xHC Latency Tolerance Parameters – High Idle Time Control

Address Offset:0x817C – 0x817F
Default Value:0x0000_0000
Access: RW; RO
Size: 32bits

Bit	Access	Default Value	RST/PWR	Description
31:29	RO	0	NA	Reserved
28:16	RW	0000h	USB	Minimum High Idle Time (MHIT) This is the minimum schedule idle time that must be available before a "High" LTR value can be indicated. This value must be larger than HIWL 12:7 – Time value in # of 125µs Bus Intervals (0 – 8ms) 6:0 – Fractional BI Time value in µs (0 – 124µs)
15:13	RO	0	NA	Reserved

Bit	Access	Default Value	RST/PWR	Description
12:0	RW	0000h	USB	High Idle Wake Latency (HIWL) This is the latency to access memory from the High Idle Latency state. This value must be larger than MIWL and LIWL 12:7 – Time value in # of 125µs Bus Intervals (0 – 8ms) 6:0 – Fractional BI Time value in µs (0 – 124µs)

Table 276. LTVMIT - xHC Latency Tolerance Parameters – Medium Idle Time Control

Address Offset:0x8180 – 0x8183
Default Value:0x0000_0000
Access: RW; RO
Size: 32bits

Bit	Access	Default Value	RST/PWR	Description
31:29	RO	0	NA	Reserved
28:16	RW	0000h	USB	Minimum Medium Idle Time (MMIT) This is the minimum schedule idle time that must be available before a "Medium" LTR value can be indicated. This value must be larger than MIWL 12:7 – Time value in # of 125µs Bus Intervals (0 – 8ms) 6:0 – Fractional BI Time value in µs (0 – 124µs)
15:13	RO	0	NA	Reserved
12:0	RW	0000h	USB	Medium Idle Wake Latency (MIWL) This is the latency to access memory from the Medium Idle Latency state. This value must be larger than LIWL 12:7 – Time value in # of 125µs Bus Intervals (0 – 8ms) 6:0 – Fractional BI Time value in µs (0 – 124µs)

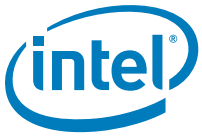
Table 277. LTVLIT - xHC Latency Tolerance Parameters – Low Idle Time Control

Address Offset:0x8184 – 0x8187
Default Value:0x0000_0000
Access: RW; RO
Size: 32bits

Bit	Access	Default Value	RST/PWR	Description
31:29	RO	0	NA	Reserved
28:16	RW	0000h	USB	Minimum Low Idle Time (MLIT) This is the minimum schedule idle time that must be available before a "Low" LTR value can be indicated. This value must be larger than LIWL 12:7 – Time value in # of 125µs Bus Intervals (0 – 8ms) 6:0 – Fractional BI Time value in µs (0 – 124µs)
15:13	RO	0	NA	Reserved
12:0	RW	0000h	USB	Low Idle Wake Latency (LIWL) This is the latency to access memory from the Medium Idle Latency state. 12:7 – Time value in # of 125µs Bus Intervals (0 – 8ms) 6:0 – Fractional BI Time value in µs (0 – 124µs)

Table 278. XECP_CMDM_CTRL_REG1 - Command Manager Control 1

Address Offset:818Ch-818Fh
Default Value:3510AFFCh
Access: RW;
Size:32 bits



This register contains fields which control the behavior of the Command Manager in the xHC.

Bit	Access	Default Value	RST/PWR	Description
31:28	RW	3h	USB	Bandwidth calculation parameter: Default bandwidth for an Interrupt endpoint.
27:24	RW	5h	USB	Bandwidth calculation parameter: Default bandwidth for an Isoch. Endpoint.
23	RO	0h	USB	Reserved
22	RW	0h	USB	Determine if stream context needs to be saved/restored due to the retry flag. Note: This is only needed when we've switched streams mid-TRB and have partial length to maintain
21	RW	0h	USB	Setting this field will cause the Configure Endpoint command to lock slot context to avoid contention with other active Endpoints on that same slot
20	RW	0h	USB	Setting this field will enable cause a Configure Endpoint Command to fail if the number of active EPs post configuration exceeds the maximum number of EPs available in cache
19	RW	0h	USB	Setting this field will prohibit the bandwidth computation during the Get Port Bandwidth command
18	RW	0h	USB	Setting this field will mask the system bandwidth checks during the bandwidth calculations
17	RW	0h	USB	Setting this field will mask the primary and secondary bandwidth checks during the bandwidth calculations
16	RW	0h	USB	0: Disable clearing of split state if TSP=1. 1: Enable clearing of split state if TSP=1
15	RW	1h	USB	0: Disable clearing other context during a disable slot command. 1: Enable clearing other context during a disable slot command.
14	RW	0h	USB	0: Disable evaluating the endpoint state during an Evaluate Context command 1: Enable evaluating the endpoint state during an Evaluate Context command.
13	RW	1h	USB	When context preservation (bit-12) is enabled: 0: Do not modify the retry bits. 1: Force the retry bits of the TRM context to 1.
12	RW	0h	USB	0: Disable context preservation 1: Enable context preservation for all commands based on the state of the TSP bit.
11	RW	1h	USB	0: Disable clearing other context during a configure endpoint command. 1: Enable clearing other context during a configure endpoint command.
10	RW	1h	USB	0: Disable clearing other context during a reset device command. 1: Enable clearing other context during a reset device command.
9	RW	1h	USB	0: Disable clearing other context during a reset endpoint command. 1: Enable clearing other context during a reset endpoint command.
8	RW	1h	USB	0: Disable clearing other context during an enable slot command. 1: Enable clearing other context during an enable slot command.
7	RW	1h	USB	0: Disable clearing TRM, Scheduler, and DMA context during a configure endpoint command. 1: Enable clearing TRM, Scheduler, and DMA context during a configure endpoint command.
6	RW	1h	USB	0: Disable clearing TRM, Scheduler, and DMA context during an address device command. 1: Enable clearing TRM, Scheduler, and DMA context during an address device command.
5	RW	1h	USB	0: Disable clearing TRM, Scheduler, and DMA context during an enable slot command. 1: Enable clearing TRM, Scheduler, and DMA context during an enable slot command.
4	RW	1h	USB	0: Disable clearing TRM, Scheduler, and DMA context during a reset device command. 1: Enable clearing TRM, Scheduler, and DMA context during a reset device command.
3	RW	1h	USB	0: Address device does not return the error for this condition. 1: Address device command returns a context state error when the EP is in the default state and BSR=1
2	RW	1h	USB	0: Disable clearing TRM, Scheduler, and DMA context during a set TR DQ pointer command. 1: Enable clearing TRM, Scheduler, and DMA context during a set TR DQ pointer command.

Bit	Access	Default Value	RST/PWR	Description
1	RW	0h	USB	0: Bandwidth calculation handled normally. 1: Forces a failure in the endpoint bandwidth calculation.
0	RW	0h	USB	0: Disable generation of the completion event. 1: Enable the command manager to generate a completion event after processing an update endpoint command.

Table 279. XECP_CMDM_CTRL_REG2 - Command Manager Control 2

Address Offset:8190h-8193h
Default Value:06C60000h
Access: RW;
Size:32 bits
This register contains fields which control the behavior of the Command Manager in the xHC. The functions controlled by this register are made available largely for debug/diagnostic purposes.

Bit	Access	Default Value	RST/PWR	Description
31	RW	0h	USB	Set this field to write all 5dw of output context
30	RW	0h	USB	Enable Stop EP 2ms Timeout
29	RW	0h	USB	Enable Slot ID Overwrite
28	RW	0h	USB	State Save Error Generator
27	RW	0h	USB	0: Turn ON the TTE clock. 1: Turn OFF the TTE clock.
26	RW	1h	USB	0: Disable clearing other context during a stop endpoint command. 1: Enable clearing other context during a stop endpoint command.
25	RW	1h	USB	0: Disable clearing other context during stall handling. 1: Enable clearing other context during stall handling.
24	RW	0h	USB	0: The internal context write dq pointer is updated normally (based on previous wr dqpointer) 1: The internal context write dq pointer value will be set to the read dq pointer value when the command manager updates internal context.
23	RW	1h	USB	0: Disable clearing TRM, Scheduler, and DMA context during a reset endpoint command. 1: Enable clearing TRM, Scheduler, and DMA context during a reset endpoint command.
22	RW	1h	USB	0: Disable hardware bandwidth calculations. 1: Enable hardware bandwidth calculations.
21	RW	0h	USB	0: Delay processing command ring TRB while internal context requests are pending. 1: Process command ring TRBs normally.
20	RW	0h	USB	0: Disable clearing other context during a set dq pointer command. 1: Enable clearing other context during a set dq pointer command.
19	RW	0h	USB	0: Check the slot and endpoint state prior to processing a reset endpoint command. 1: Ignore the slot and endpoint state when processing a reset endpoint command.
18	RW	1h	USB	0: Disable sequence number preservation during set dq pointer command. 1: Enable sequence number to be preserved during set dq pointer command.
17	RW	1h	USB	0: Disable stop endpoint command interruption. 1: Enable stop endpoint command to be interrupt if the command is not completing normally.
16	RW	0h	USB	0: Pending commands have a higher priority than update endpoint processing. 1: Update endpoint processing in the command manager has a higher priority than pending commands. Note: Enabling this bit can prevent prolonged stall handling.
15	RW	0h	USB	0: Stall handling does clear the EP context fields. 1: Stall handling does not clear the EP context fields.
14	RW	0h	USB	0: Force the default burst size to be 1 when clearing context. 1: Force the default burst size to be the defined maximum burst size when clearing context.

Bit	Access	Default Value	RST/PWR	Description
13:0	RW	0h	USB	Clear state machine present state: Setting a bit in this field to 1, will reset the specified command manager state machine to the starting/idle state. bit-0: disable slot state machine bit-1: enable slot state machine bit-2: reset endpoint state machine bit-3: reset device state machine bit-4: command ring state machine bit-5: stop endpoint state machine bit-6: set dq pointer state machine bit-7: force header state machine bit-8: evaluate context state machine bit-9: update endpoint state machine bit-10: address device state machine bit-11: port bandwidth state machine bit-12: read output context state machine bit-13: configure endpoint state machine

Table 280. XECP_CMDM_CTRL_REG3 - Command Manager Control 3

Address Offset:8194h-8197h
Default Value:0020505Ah
Access: RW;
Size:32 bits
This register contains fields which control the behavior of the Command Manager in the xHC. The functions controlled by this register are made available largely for debug/diagnostic purposes.

Bit	Access	Default Value	RST/PWR	Description
31	RW	0h	USB	RESERVED
30	RW	0h	USB	Default Control EP double counting Enable. When cleared, Control EP accounting is not enabled. If this feature is disabled, it implies that the Default Control EP accounting is comprehended through the BW Check, thus it has to be enabled via 805C[22], otherwise Default Ctrl EP's will not be accounted for. This allows for a usage where BW Check is disabled in HW while requiring HW to enforce EP resource check. This bit also controls ignore_hi_atomic_en functionality.
29:26	RW	0h	USB	RESERVED
25	RW	0h	USB	Setting this bit enables a mode to clear local LCStreamID as a part of StopEP cmd for StreamEP
24:22	RW	0h	USB	RESERVED
21	RW	1h	USB	stop_ep_clr_stream_st_en_reg
20	RW	0h	USB	Setting this field will prohibit the Command Manager from locking context during the execution of either Stop Endpoint, Reset Device, Disable Slot, Evaluate Context or Configure Endpoint commands
19	RW	0h	USB	Setting this field will cause both the IDMA & ODMA engines to stop their transaction timers when the Command Manager is executing a Stop Endpoint Command since they may be locked out of context
18	RW	0h	USB	Setting this field will enable DMA context to be cleared during a Disable Slot command
17:16	RW	0h	USB	This field determines the amount of wait time inserted at the end of a Disable Slot command prior to signaling a completion on the command ring. 0: Disabled 1: 100us 2: 9ms 3: 10ms
15:8	RW	50h	USB	Bandwidth calculation parameter: Default high speed bandwidth to advertise on each port.
7:0	RW	5Ah	USB	Bandwidth calculation parameter: Default bandwidth to advertise on each port.

Table 281. PDDIS – xHC Pull Down Disable Control

Address Offset: 8198h – 819Bh
Access: RO; RW

Size: 32b

Bit	Access	Default Value	RST/PWR	Description
31:2	RO	00h	USB	Reserved
1:0	RW	0b	Sus	PDDISEN: Allow USB Pulldown disable Each bit corresponds to a USB2 port indexed by the bit number (zero based). Bit 0 = USB2 port 1 Bit 1 = USB2 port 2 Etc. When set, allow the pulldown on D+ or D- (as appropriate) to be disabled when the port is connected and in L2. e.

Table 282. THROTT –XHCI Throttle Control

Address Offset: 819Ch – 819Fh
Access: RO; RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:21	RO	00h	USB	Reserved
20	RW	0b	USB	SSIC Thermal Throttle Ux Mapping Controls if U1 or U2 is forced upon the start of thermal throttle OFF period. 0 – Force ports into U2 during Thermal Throttle triggered Ux entry. 1 – Force ports into U1 during Thermal Throttle triggered Ux entry.
19:18	RW	0b	USB	USB3 Thermal Throttle Ux LGO delay Controls the delay enforced between LMP for FLPMA and LMP for Ux LGO. After sending LPMA ON , wait for pre-defined number of clocks to initiate LGO_U1/LGO_U2 00: 8 clocks 01: 32 clocks 10: 128 clocks 11: 0 clocks This field does not apply to ports that are not operating in the mode required to issue FLMA ON.
17	RW	0b	USB	Thermal Throttling Disable 0: Thermal throttling is enabled. 1: Thermal throtling is disabled. The host controller ignores the TT control inputs and does not throttle.
16	RW	0b	USB	USB3 Thermal Throttle Ux Mapping Controls if U1 or U2 is forced upon the start of thermal throttle OFF period. 0 – Force ports into U2 during Thermal Throttle triggered Ux entry. 1 – Force ports into U1 during Thermal Throttle triggered Ux entry.
15	RW	0b	USB	Throttle Priority Mode 0: “Off” period has priority: In this case, when the throttle signal is asserted, the host controller enters the “off” state on the next uframe boundary, and stays in the off state for the prescribed duration or until the end of the 16 uframe throttle period – whichever occurs first. On subsequent throttle periods, the off period occurs first and then the on period. 1: The “On” period has priority: In this case, when the throttle signal is asserted, the host controller completes the required On period first before entering the off period. If the required number of uFrames has already been executed in a 16 uframe throttle window, the controller enters the off period immediately.
14	RW	0b	USB	Disable Force L1 when throttled. 1: USB2 port will not force L1 entry on throttled ports. L1 entry will be based on the normal idle timeout 0: USB2 ports will attempt to enter L1 immediately after throttled ports are idle.

Bit	Access	Default Value	RST/PWR	Description
13	RW	0b	USB	Disable Interrupt Throttling 0: Interrupt traffic is throttled 1: Interrupt traffic is not throttled
12	RW	0b	USB	Disable Isochronous Throttling 0: Isochronous traffic is throttled 1: Isochronous traffic is not throttled
11:8	RW	0h	USB	T1 Action: # bus intervals to be idle for async traffic out of the 16 interval master period; from 0 to 15.
7:4	RW	0h	USB	T2 Action: # bus intervals to be idle for async traffic out of the 16 interval master period; from 0 to 15.
3:0	RW	0h	USB	T3 Action: # bus intervals to be idle for async traffic out of the 16 interval master period; from 0 to 15. Note: this value shall never bet set to exceed throttling of more than 14 uFrames. It implies that we will have at least 2 un-throttled micro frames.

Table 283. LFPSPM - LFPS PM Control

Address Offset:81A0h-81A3h
Default Value:0h
Access: RW;
Size:32 bits
This register is subject to HW save and restore.

Bit	Access	Default Value	RST/PWR	Description
31:2	RO	0h	USB	Reserved
1:0	RW	0h	USB	LFPS Power Management in U3 Enable This field allows xHC to turn off LFPS Receiver when the port is in U3. This allows the Host Controller to save some extra power (about 200µW per port) in idle states if device connected on a port is not Resume capable or Resume enabled. This choice has to be done by BIOS and based on platform knowledge. For example, if an in-box device is not Resume Capable, BIOS could allow xHC to turn-off Rx LFPS when the port is in U3. Each bit represents a port. Bit [0] is for USB3.0 Port 1, Bit [1] is for USB3.0 Port 2 . ‘0’ in a bit position: LFPS Receiver shall be kept enabled when the port is in U3. ‘1’ in a bit position: LFPS Receiver shall be disabled when the port is in U3.

Table 284. U2PDM –USB2 Port Disconnect Mask

Address Offset: 81A4h – 81A7h
Access: RO; RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:2	RO	00h	USB	Reserved

Bit	Access	Default Value	RST/PWR	Description
1:0	RW	0b	USB	USB2 Port Disconnect Mask Per Port Control to allow for masking of port dis-connect events. 0: Do not mask Port Dis-Connect 1: Mask Port Dis-Connect by masking CSC from being set and suppressing PME due to the disconnect. PLS and CCS will reflect the true port state.

Table 285. U2PCM –USB2 Port Connect Mask

Address Offset: 81A8h – 81ABh
Access: RO; RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:2	RO	00h	USB	Reserved
1:0	RW	0b	USB	USB2 Port Connect Mask Per Port Control to allow for masking of port connect events. 0: Do not mask Port Connect 1: Mask Port Connect by masking CSC from being set and suppressing PME due to the connect. PLS and CCS will reflect the true port state.

Table 286. U3PDM –USB3 Port Disconnect Mask

Address Offset: 81ACh – 81AFh
Access: RO; RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:2	RO	00h	USB	Reserved
1:0	RW	0b	USB	USB3 Port Disconnect Mask Per Port Control to allow for masking of port dis-connect events. 0: Do not mask Port Dis-Connect 1: Mask Port Dis-Connect by masking CSC from being set and suppressing PME due to the disconnect. PLS and CCS will reflect the true port state.

Table 287. U3PCM –USB3 Port Connect Mask

Address Offset: 81B0h – 81B3h
Access: RO; RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:2	RO	00h	USB	Reserved
1:0	RW	0b	USB	USB3 Port Connect Mask Per Port Control to allow for masking of port connect events. 0: Do not mask Port Connect 1: Mask Port Connect by masking CSC from being set and suppressing PME due to the connect. PLS and CCS will reflect the true port state.

Table 288. THROTT2 –XHCI Throttle Control2

Address Offset: 81B4h – 81B7h
Access: RO; RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:2	RO	00h	USB	Reserved

Bit	Access	Default Value	RST/PWR	Description
1:0	RW	All 1's	USB	Thermal Throttle Force LPM Accept Enable Per Port Control to allow for enforcement to be based on device detection if certain devices do not support FLPMA. 0: Do not set FLPMA prior to Ux entry due to TT 1: Set FLPMA prior to Ux entry due to TT

Table 289. LFPSONCOUNT – LFPS On Count

Address Offset: 81B8h – 81BBh
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:18	RW	0h	USB	RSVD
17:16	RW	0h	USB	XU2P3LPSC (U2P3 LFPS Periodic Sampling Control) This field controls the OFF time for the LFPS periodic sampling for SS and SSIC ports in U2P3. If LFPSPM for a port is '1', it will override the OFF time and LFPS receiver will remain OFF permanently. For Fast Sim mode, 500us will be equivalent to 5us. 0x0 – Polling Disable. (RXDET Polling will become 100ms.) 0x1 – 500us OFF Time 0x2 – 1ms OFF Time 0x3 – 1.5ms OFF Time
15:10	RW	08h	USB	XLFPSONCNTSSIC (LFPS ON Count for SSIC Ports) This time would describe the number of clocks SSIC LFPS will remain ON. SSIC LFPS detection operation may be carried out on using RTC clock or Oscillator clock. The value of this register should be adjusted accordingly. For RTC recommended value is 2. For Oscillator clock, recommended value is 8.
9:0	RW	0C8h	USB	XLFPSONCNTSS (LFPS ON Count for SS Ports) This time would describe the number of clocks LFPS will remain ON. LFPS detection operation may be carried out on using RTC clock or Oscillator clock. The value of this register should be adjusted accordingly. For RTC recommended value is 2. For Oscillator clock, recommended value is 200.

Table 290. D0i2CTRL – D0i2 Control Register

Address Offset: 81BCh – 81BFh
Access: RO, RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:30	RO	0h	USB	RSVD
29:26	RW	2h	USB	D0i2 Minimum Residency This field controls the minimum time that we must stay in D0i2 to ensure that the entry sequence has settled before we attempt to exit. 0h – Disabled 1h – 8 clocks 2h – 16 clocks 3h – 32 clocks 4h – 128 clocks 5h – 256 clocks 6h – 512 clocks 7h – 1024 clocks

Bit	Access	Default Value	RST/PWR	Description
25:22	RW	1h	USB	D0i2 Entry Hysteresis Timer This field allows for a hysteresis timer to be implemented specifically for D0i2. This will allow for D0i2 entry to be controlled independently from the timer used for D0i3 and D3. 0h – Disabled 1h – 8 clocks 2h – 16 clocks 3h – 32 clocks 4h – 64 clocks 5h – 128 clocks 6h – 256 clocks 7h – 512 clocks
21	RW	0b	USB	Active Periodic EP Disable This field allows the xHC to control how aggressive it enters D0i2 in the presence of active Periodic EP's. Setting this field will allow D0i2 only when there are no active Periodic EP's on the schedule. Either there are no active DB or any active Interrupt EP is flow controlled.
20:16	RW	2b	USB	MSI D0i2 Pre Wake Time (MSID0I2PWT) This is the latency that is expected to be incurred to exit the D0i2 state. This wake latency is the latency to be added to the tracked D0i2 wake by the MSI module. Example: If while allowing D0i2 there is an MSI generation that will trigger in 250 us from now ,the MSI module will trigger a D0i2 wake up 250 us – "MSI D0i2 Pre Wake Time". The D0I2WL is to ensure that the act of D0i2 exit does not impact the action(s) required by the alarm(s) that was enabled prior to D0i2. 3:0 – 250 ns ticks 0h – 0 ns 1h – 250 ns … 1Fh – 3750 ns
15:4	RW	4Bh	USB	MSI Idle Threshold This field allows the xHC to control how aggressive it enters D0i2 in the presence of pending MSI. This field is valid only if Pending MSI Disable is "0", allowing D0i2 in the presence of pending MSI's. D0i2 will be prevented if the amount of idle time between Event Ring being idle to the time an MSI will be generated does not exceed this time. Register Format: Bits [11:0] # 250 ns ticks
3	RW	0h	USB	Pending MSI Disable This field allows the xHC to disable D0i2 when there are pending MSI's in the event manager. Setting this field will require all IMOD counters to be 0h and all MSI's delivered. Clearing this field will allow for D0i2 power gating while there are 1 or more IMOD counters decrementing which implies that an MSI is pending and will be generated once the corresponding IMOD counter reaches 0h.
2	RW	0h	USB	Frame Timer Run Disable This field allows the xHC to disable D0i2 when the frame timer is running. Clearing this field will allow D0i2 when the frame timer is required as defined in the XHCI Spec. Setting this field will not allow D0i2 when the frame timer is required and will limit D0i2 for the condition where the frame timer is not required.
1	RW	0h	USB	USB2 L1 Disable This field allows the xHC to disable D0i2 when USB2 ports are in L1. This implies that D0i2 will only be triggered when ports are in L2 or deeper.

Bit	Access	Default Value	RST/PWR	Description
0	RW	0h	USB	USB3 U2 Disable This field allows the xHC to disable D0i2 when USB3 ports are in U2. This implies that D0i2 will only be triggered when ports are in U3 or deeper.

Table 291. D0i2SchAlarmCtrl – D0i2 Scheduler Alarm Control Register

Address Offset: 81C0h – 81C3h
Access: RO,RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:29	RO	0h	USB	RSVD
28:16	RW	0000h	USB	D0i2 Idle Time (D0I2IT) This is the minimum schedule idle time that must be available before D0i2 can allowed. 12:7 – Time value in # of 125µs Bus Intervals (0 – 8ms) 6:0 – Fractional BI Time value in µs (0 – 124µs) This field controls how much scheduler idle time is required to trigger D0i2. The scheduler idle time is the same idle time that is used by other functions implementing alarm timers such as PLL shutdown, LTR and USB2 L1 override. If there is a need to require other alarm timers to have been set such as LTR has triggered a Low Idle time, then this field needs to be as aggressive as LTR Low Min Idle Time to ensure D0i2 is triggered once the scheduler has detected IDLE in the schedule. This is only to be used as alternate modes of operation or back up modes.
15:13	RW	000b	USB	Reserved
12:0	RW	0000h	USB	D0i2 Wake Latency (D0I2WL) This is the latency that is expected to be incurred to exit the D0i2 state. This wake latency is the latency to be added to the tracked D0i2 wake by the scheduler. Example: If while allowing D0i2 there is an alarm that will trigger in 250 us from now ,the scheduler will allow D0i2 and track this alarm with an adjustment to wake up 250ns – D0I2WL) from. The D0I2WL is to ensure that the act of D0i2 exit does not impact the action(s) required by the alarm(s) that was enabled prior to D0i2. 12:7 – Time value in # of 125µs Bus Intervals (0 – 8ms) 6:0 – Fractional BI Time value in µs (0 – 124µs)

Table 292. USB2PMCTRL – USB2 Power Management Control

Address Offset: 81C4h – 81C7h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:12	RW	0h	USB	RSVD
11	RW	0h	USB	USB2 PHY USB Power Gate PORTSC Block Policy (U2PSPGPSCBP) This controls the policy for blocking PORTSC Updates while the USB2 PHY USB Well is power gated. When set, the controller will block any updates to the PORTSC caused by port status change if the USB2 PHY USB is power gated. 0 – Do not

Bit	Access	Default Value	RST/PWR	Description
10:8	RW	0h	USB	USB2 PHY USB Well Power Gate Entry Hysteresis Count (U2PSPGEHC) This controls the amount of hysteresis time the controller will enforce after detecting the USB2 PHY USB Power Gate entry condition. 0h – 0 clocks 1h – 32 clocks 2h – 64 clocks 3h – 128 clocks 4h – 256 clocks 5h – 512 clocks 6h – 1024 clocks 7h – 2048 clocks
7:4	RW	0h	USB	USB2 Common Lane Power Gate Latency (U2CLPGLAT) This field represents the worst case latency for the USB2 Common Lane to enter and exit its power gate state. This fields is required to be compared to a ports HIRD/HIRD value for the ports that have allowed L1 to L2 mapping to determine if the Common Lane can be allowed to power off. If the power gate entry/exit latency is greater than the HIRD/HIRDD then the common lane should not be allowed to power gate as this will result in a L1 exit violation. 0h – 100 us 1h – 200 us 2h – 300 us … Eh – 1500us Fh – 1600 us
3:2	RW	0h	USB	USB2 PHY USB Well Power Gate Policy (U2PSUSPGP) This field controls when to enable the USB2 PHY USB Well Power Gating when the proper conditions are met. 00 – USB2 PHY USB Power Gating is Disabled. 01 – USB2 PHY USB Power Gating is Enabled in Only D0 and D0i2 (Excludes D0i3 and D3) 10 – USB2 PHY USB Power Gating is Eanabled in only in D0, D0i2 and D0i3 (Excludes D3) 11 – USB2 PHY USB Power Gating is Eanabled in D0/D0i2/D0i3/ D3
1	RW	0h	USB	USB2 Common Lane Power Gating Enable During L1 to L2 Mapping for USB2 PHY Power Gating (U2CLPGEL1L2) This field when set enables the controller to allow for the common lane power gating to be enabled when all ports are exposed as in L2 to the USB2 PHY while at least 1 port has been mapped to L2 from L1. This field alone does not guarantee power gating since the L1 HIRD/HIRDD Value must be compared with the PHY's power gate exit latency (U2CLPGLAT) held in this register to ensure that L1 exit is not violated. 0 – USB2 Common Lane Power Gating is disabled when any port has been mapped from L1 to L2. 1 – USB2 Common Lane Power Gating is allowed when any port has been mapped to L2 from L1 with the additional condition that the HIRD/HIRDD is greater than the PHY's Power Gate exit latency.

Bit	Access	Default Value	RST/PWR	Description
0	RW	0h	USB	USB2 Data Lane L1 to L2 Mapping Enable for USB2 PHY Power Gating (U2DLL1L2ME) This field when set enables the controller to map an L1 entry directly to L2 to allow the USB2 PHY to trigger its Autonomous Power Gating. The USB2 PHY will trigger PG only when in L2 since it does not fully understand the requirements for L1. 0 – USB2 L1 to L2 mapping is disabled for all ports 1 – USB2 L1 to L2 mapping is enabled for all ports

Table 293. TRB_PRF_CTRL_REG1 –TRB Prefetch Control Register 1

Address Offset:81D0-81D3h
Default: 0h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:6	RW	0h	USB	Reserved
5	RW	0h	USB	Disable TRB-$ for CTRL EPs – Setting this bit disable TRB caching for control EPs. When set, all control EP's TRB request to TRB-$ will take bypass path. 0 : Enable TRB-$ for CTRL EPs 1 : Disable TRB-$ for CTRL EPs
4	RW	0h	USB	Disable multiple Outstanding prefetch request per EP When set, it disables issuing multiple prefetch requests and serializes the prefetch for a given EP. In other word, there will be only one prefetch request outstanding per EP. 0 : Enable multiple prefetches per EP. 1 : Disable multiple Outstanding prefetch requests per EP
3	RW	0h	USB	Disable TRB cache's "Defer" response generation capability. When set, TRB Cache will not return "Defer" response to TRM Xfer engine's TRB request upon cache miss or when the requested TRB is not available in cache to serve. 0 : TRB Cache will generate "Defer" response if the requested TRB is not available in the cache 1: Disable "Defer" response generation capability. In this case, the TRB cache will generate response back when the TRB is available.
2	RW	0b	USB	Enable Cache Bypass for Cache Full : This mode enables TRB Cache bypass path when the cache is full and no entry is in the state that can be flushed/replaced. In that case, this mode will allow TRM to make progress on this new EP who's TRB fetch request resulted in cache miss and no cache resource available for allocation. 0 : Disable the bypass path. In this mode, the cache always waits for the state where one entry is available to be flushed/ replaced. 1: Enable the bypass path.
1	RW	0b	USB	Disable Link TRB Traversal : The field enables/disable TRB Prefetcher to prefetch/traverse beyond the Link TRB. 0 : Enable prefetching beyond Link TRB 1 : Disable prefetching beyoud Link TRB
0	RW	0b	USB	TRB Prefetcher Enable : This field enables/disables the TRB Prefetch feature. 0: Disable TRB Prefetcher 1: Enable TRB Prefetcher

Table 294. TRB_PRF_CTRL_REG2 –TRB Prefetch Control Register-2

Address Offset:81D4-81D7h
Default: 20100410h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:30	RW	0h	USB	Reserved
29:24	RW	20h	USB	Max Prefetch (TRB) EPs Cache depth This controls the number of EPs whose TRBs can be cached. Setting it to smaller than the actual cache depth will effectively reduce the cache depth and impact the performance.
23:21	RW	0h	USB	Reserved These ones are spare bits for future scalability
20:16	RW	10h	USB	Max TRB prefetch (per EP) – This allows us to control number of TRBs that can be prefetched and cached at a given time for EPs. The value set in this field is in term of number of TRB.
15:13	RW	0h	USB	Reserved These ones are spare bits for future scalability
12:8	RW	4h	USB	Min TRBs per prefetch read – This allows us to control Min number of TRBs that is required to be fetched as a part of single prefetch read request to avoid smaller size prefetches. This is mainly to efficiently use the read credit on IOSF/Backbone. The value set in this field is in term of number of TRBs. Note that, each TRB is 16B wide. Note that, the behavior will be undefined if set to 0. Make sure to set this value smaller than "Max TRBs per prefetch read" field. The behavior will be undefined if it is not followed.
7:5	RW	0h	USB	Reserved These ones are spare bits for future scalability of "Max TRB per prefetch read" field due to cache size increase.
4:0	RW	10h	USB	Max TRBs per prefetch read – This allows to control Max number of TRBs that can be fetched in single prefetch read request. The value set in this field is in term of number of TRBs. Note that, each TRB is 16B wide. Note that, the behavior will be undefined if set to 0. Also, the value in this field should be chosen such so the controller doesn't violate the MaxRdReqSize setting. Formula – Max number of TRBs per read <= (MaxRdReqSize / 16)

Table 295. TRB_PRF_CACHEINV_REG – TRB Prefetch Cache Invalidation Register

Address Offset:81D8-81DBh
Default: 0h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31	RW1S	0h	USB	Invalidate/Flush the entire TRB Cache. When this is set, the Slot ID and EP ID fields of the register is don't care. SW sets this bit to trigger a Cache wide entry invalidation. HW will clear this bit once the Cache invalidation is complete.
30	RW1S	0h	USB	Invalidate/Flush TRB Cache for EP specified by Slot ID and EP ID fields of the register. SW sets this bit to trigger a specific entry invalidation. HW will clear this bit once the Cache invalidation is complete.

Bit	Access	Default Value	RST/PWR	Description
29:24	RW	0h	USB	Reserved
23	RW	0h	USB	Enable TRB-$ flushing for Disable Slot command. 0 : Disable flushing of TRB-$ for Disable Slot. 1 : Enable flushing of TRB-$ for Disable Slot. Always set it to 0 if TRB PRF Cache feature is disabled or not supported.
22	RW	0h	USB	Enable TRB-$ flushing for Stop EndPoint command. 0 : Disable flushing of TRB-$ for Stop Endpoint. 1 : Enable flushing of TRB-$ for Stop Endpoint. Always set it to 0 if TRB PRF Cache feature is disabled or not supported.
21	RW	0h	USB	Enable TRB-$ flushing for SetTRDQPointer Command. 0 : Disable flushing of TRB-$ for SetTRDQPointer. 1 : Enable flushing of TRB-$ for SetTRDQPointer. Always set it to 0 if TRB PRF Cache feature is disabled or not supported.
20	RW	0h	USB	Enable TRB-$ flushing for Update EndPoint (cases that triggers EP state change and stream switch etc). 0 : Disable flushing of TRB-$ for Update EndPoint. 1 : Enable flushing of TRB-$ for Update EndPoint. Always set it to 0 if TRB PRF Cache feature is disabled or not supported.
19	RW	0h	USB	Enable TRB-$ flushing for Reset EndPoint command. 0 : Disable flushing of TRB-$ for Reset Endpoint. 1 : Enable flushing of TRB-$ for Reset Endpoint. Always set it to 0 if TRB PRF Cache feature is disabled or not supported.
18	RW	0h	USB	Enable TRB-$ flushing for Reset Device command. 0 : Disable flushing of TRB-$ for Reset Device. 1 : Enable flushing of TRB-$ for Reset Device. Always set it to 0 if TRB PRF Cache feature is disabled or not supported.
17	RW	0h	USB	Enable TRB-$ flushing for Config EndPoint command. 0 : Disable flushing of TRB-$ for Config EndPoint. 1 : Enable flushing of TRB-$ for Config EndPoint. Always set it to 0 if TRB PRF Cache feature is disabled or not supported.
16	RW	0h	USB	Enable/Disable full handshake for TRB-$ flush. 0 : Enable full handshake 1 : Disable full handshake Always set it to 1 if TRB PRF Cache feature is disabled or not supported.
15:13	RW	0h	USB	Reserved
12:8	RW	0h	USB	EP ID : EP Id (in DCI format) of EP that is requested to be invalidated
7:0	RW	0h	USB	Slot ID : Slot ID of EP that is requested to be invalidated

Table 296. TRB_PRF_CACHE_STATUS_REG1 – TRB Prefetch Cache Status Register-1
Address Offset:81DC-81DFh
Default: 0h

Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:27	RO	0h	USB	Prefetch TRB Address (bits 8:4 of TRB Address)
26:22	RO	0h	USB	Prefetch pointer
21	RO	0h	USB	Link TRB Stop prefetch flag
20	RO	0h	USB	"Invalidate pending" flag
19:15	RO	0h	USB	EP/DCI the Way ID provided by SW is allocated to.
14:9	RO	0h	USB	Device/Slot the Way ID provided by SW is allocated to.
8	RO	0h	USB	Way ID Valid : Indicates whether the way is allocated and is "valid" for the Way ID provided by SW.
7:0	RW	0h	USB	TRB-$ way ID : TRB-$ way ID that we want to read out the status of.

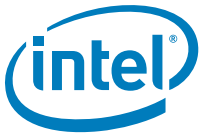
Table 297. TRB_PRF_CACHE_STATUS_REG2 – TRB Prefetch Cache Status Register-2

Address Offset:81E0-81E3h
Default: 0h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:30	RO	0h	USB	Reserved
30	RO	0h	USB	Multiple Link Invalidation
29:28	RO	0h	USB	Last Link TRB Distant (in terms of TRB count)
27	RO	0h	USB	Last Link TRB Distant Valid
26:25	RO	0h	USB	EOR state
24:20	RO	0h	USB	CPL TRB Address
19:15	RO	0h	USB	CPL Pointer
14:10	RO	0h	USB	Xfer TRB Address
9:5	RO	0h	USB	Xfer Pointer
4:0	RO	0h	USB	Write Pointer

Table 298. HOST_BW_OV_SSP_REG – Super Speed Bandwidth Overload

Address Offset: 81F0h – 81F3h



Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	0h	USB	Reserved
23:12	RW	02h	USB	BW calculation: Overhead per packet for SSP BW calculations. see white paper.
11:0	RW	08h	USB	BW calculation: Overhead per burst for SSP BW calculations. see white paper.

Table 299. HOST_CTRL_LINK_PORT_SPEED_REG

Address Offset:81F4 - 81F7h
Default Value:0h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
[31:USB3_PORTS]			USB	RESERVED
[USB3_PORTS-1:0]	RW	0	USB	PORT_SPEED_MODE 0: PORT Speed field in the PortSC will reflect the speed value based on the connected device as SSP, SS or SSIC with correct rate. 1: PORT Speed filed will reflect SS (with USB3.0 Capability) as the only speed when device is connected.

Table 300. HOST_CTRL_SUS_LINK_PORT_REG

Address Offset: 81F8-81FBh
Default Value:0h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:4			AON	RESERVED
3	RW	1	AON	USB3_PORTEN_FORCE DISC Configuration to enable the force disconnect for SS port if SSPE is cleared and Port is not in RXDET P3 state.
2	RW	0	AON	USB3_EXI_FORCE DISC Configuration to enable the force disconnect for SS port if EXI over BSSB is requesting for the port ownership and Port is not in RXDET P3 state.
1	RW	0	AON	USB3_HOST_ALLOC_FORCE DISC Configuration to enable the force disconnect for SS port if XDCI is requesting for the port ownership and Port is not in RXDET P3 state.
0	RW	0	AON	USB3_LFPS_POLLING_MODE 0: Wait for BIOS programming done before proceeding. This also implies that for D3 exit, restore from the scratch pad is complete. 1: Don’t wait for the BIOS programming done and make forward progress based on the default values. BIOS should not update the LFPS default values if this bit set to 1.

Note:
There exists a DEFINE to track the last register that need to be saved/restored as part of the register save/restore to scratchpad that needs to be updated. This is what it needs to be based on the defined registers above.
`define LAST_CHICKEN_BITS_OFS (`XECP_HOST_ADDR_OFS+16'd396) // OFFSET x81F4

Table 301. USB2_LINESTATE - Port Line State USB2

Address Offset:83F4-83F7h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:(NumUSB2*2)	RO	0h	USB	RESERVED
(NumUSB2*2-1) : (NumUSB2*2-2)	RO	0h	USB	Port N UTMI Linestate

Table 302. ECC Parity Error Log Register

Address Offset:83F8-83FBh
Access: RW, RW1C, RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31	RW1C	0x0	USB	Command Parity Error detected on received IOSF transaction
30	RW1C	0x0	USB	Data Parity Error detected on received IOSF transaction
29	RW1C	0x0	USB	Error Present detected on received IOSF transaction
28:26	RO	0x0	USB	Reserved
25:21	RW1C	0x0	USB	Correctable ECC Error RF Info When set indicates the specific RF the ECC Error was detected on. This is used along with the ECC Source, and Port Info to determine the specific RF on which Correctable ECC Error was seen on. USB2 Port RF: 00000: Reserved 00001: Async. TX Payload 00010: Periodic TX Payload 00011: RX Payload 00100: TTE Periodic TX Payload 00101: TTE RX Payload Others: Reserved USB3 Port RF: 00000: Reserved 00001: Async TX Payload 00010: Periodic TX Payload 00011: RX Payload Others: Reserved XHCI Engine RF: 00000: Reserved 00001: TTE Context 00010: TRM Context 00011: XHCI Completion Collect 00100: Debug Device Completion Collect 00101: DBC-EXI Trace Data
20:15	RW1C	0x0	USB	Correctable ECC Error Source Port Info When set indicates the Port# if the ECC Error was detected on any of the USB2/USB3 Port RFs. This is valid only when bit[1:0] != 00

Bit	Access	Default Value	RST/ PWR	Description
14:13	RW1C	0x0	USB	Correctable ECC Error Source Log When an Correctable ECC is detected for an RF, the corresponding bit is set to '1' 11: Detected Uncorrectable ECC Error on USB3 RFs 10 : Detected Uncorrectable ECC Error on USB2 RFs 01: Detected Uncorrectable ECC Error on XHCI Engine RFs 00 : No Error Note: On detection of first Uncorrectable ECC Error HW shall lock the Correctable log registers (Source, Port, RF) until SW clears the ECC Error log or cleared by reset.
12:8	RW1C	0x0	USB	Uncorrectable ECC Error RF Info When set indicates the specific RF the ECC Error was detected on. This is used along with the ECC Source, and Port Info to determine the specific RF on which uncorrectable ECC Error was seen on. USB2 Port RF: 00000: Reserved 00001: Async. TX Payload 00010: Periodic TX Payload 00011: RX Payload 00100: TTE Periodic TX Payload 00101: TTE RX Payload Others: Reserved USB3 Port RF: 00000: Reserved 00001: Async TX Payload 00010: Periodic TX Payload 00011: RX Payload Others: Reserved XHCI Engine RF: 00000: Reserved 00001: TTE Context 00010: TRM Context 00011: XHCI Completion Collect 00100: Debug Device Completion Collect 00101: DBC-EXI Trace Data
7:2	RW1C	0x0	USB	Uncorrectable ECC Error Source Port Info When set indicates the Port# if the ECC Error was detected on any of the USB2/USB3 Port RFs. This is valid only when bit[1:0] != 00
1:0	RW1C	0x0	USB	Uncorrectable ECC Error Source Log When an uncorrectable ECC is detected for an RF, the corresponding bit is set to '1' 11: Detected Uncorrectable ECC Error on USB3 RFs 10 : Detected Uncorrectable ECC Error on USB2 RFs 01: Detected Uncorrectable ECC Error on XHCI Engine RFs 00 : No Error Note: On detection of first Uncorrectable ECC Error HW shall lock the Uncorrectable log registers (Source, Port, RF) until SW clears the ECC Error log or cleared by reset.

Table 303. ECC Poisining Control Register

Address Offset:83FC-83FFh
Access: RO;

Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:23	RW	0x0	USB	XHCI Engine RFs ECC Poisoning Inversion bits for the 64b or 128bit (based on RF width)
22:14	RW	0x0	USB	USB3 RFs ECC Poisoning Inversion bits for the 64b or 128bit (based on RF width)
13:5	RW	0x0	USB	USB2 RFs ECC Poisoning Inversion bits for the 64b or 128bit (based on RF width)
4:3	RO		USB	Reserved
2	RW	0x0	USB	Enable ECC Poisoning for XHCI Engine related RFs that support ECC
1	RW	0x0	USB	Enable ECC Poisoning for USB3 Port related RFs that support ECC. Setting this bit enables poisoning of USB2 Port related RFs. This applies to all USB3 ports
0	RW	0x0	USB	Enable ECC Poisoning for USB2 Port related RFs that support ECC. Setting this bit enables poisoning of USB2 Port related RFs. This applies to all USB2 ports

Table 304. USB2/HSIC Port State Register

Address Offset:8400-8407h
Access: RO;
Size:64 bits

Bit	Access	Default Value	RST/PWR	Description
63:N	RO	0h	USB	RSVD
N:0	RO	0h	USB	USB2/HSIC Port State Per USB2/HSIC Port State Register indicating the following states 0x0 – Disconnected (PLS=5h) 0x1 – Suspended (PLS=3h) 0x2 – Disabled (PLS=7h) 0x3 – Reserved (PLS=all others) This register is Read Only and will reflect the state of the ports. Status can change at any time and any usage of this information must be done with care and under specific flows where port state change race conditions are properly handled. Note: The expectation is that this register is consumed when the controller is power gated which implies that valid values exposed should be 0x, 0x1 or 0x2. A value of 0x3 is not expected when in power gated state and implies there is an error.

Note: N = (2 * USB2/HSIC Port Count)

Table 305. USB3/SSIC Port State Register

Address Offset:8408-840Fh
Access: RO;
Size:64 bits

Bit	Access	Default Value	RST/PWR	Description
63:N	RO	0h	USB	RSVD

Bit	Access	Default Value	RST/PWR	Description
N:0	RO	0h	USB	USB3/SSIC Port State Per USB3/SSIC Port State Register indicating the following states 0x0 – Disconnected (PLS=5h) 0x1 – Suspended (PLS=3h) 0x2 – Disabled (PLS=4h) 0x3 – Reserved (PLS=all others) This register is Read Only and will reflect the state of the ports. Status can change at any time and any usage of this information must be done with care and under specific flows where port state change race conditions are properly handled. Note: The expectation is that this register is consumed when the controller is power gated which implies that valid values exposed will be 0x, 0x1 or 0x2. A value of 0x3 is not expected when in power gated state and implies there is an error.

Note: N = (2 * USB3/SSIC Port Count)

Table 306. FUSE1 : Miscellaneous Fuses

Address Offset:8410h-8413h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:9	RO	0h	USB	Reserved :
8	RO/V	0h	USB	USB2 PLL Shutdown Disable (USB2PLLSDIS) : 0: USB2 PLL shutdown enabled 1: USB2 PLL shutdown disabled
7	RO/V	0h	USB	USB I/O Power Management Disable (USBIOPMDIS) : 0: USB2 HW LPM and USB3 HW Ux under XHC enabled 1: USB2 HW LPM and USB3 HW Ux under XHC disabled
6	RO/V	0h	USB	XHC Dynamic Clock Gating Disable (XHCDCGDIS) : 0: USB3 (XHC) dynamic clock gating enabled 1: USB3 (XHC) dynamic clock gating disabled
5	RO/V	0h	USB	USBr Disable (USBRDIS) : 0: USBr enabled 1: USBr disabled
4:3	RO/V	0h	USB	Reserved
2	RO/V	0h	USB	Reserved
1	RO/V	0h	USB	HS Port Count 0: 10 HS ports (USBr available) 1: 8 HS ports (no USBr) This reflects the state of Fuse 470
0	RO/V	0h	USB	XHCI Function Disable (XHCFD) : When asserted, it indicates the XHCI is fused to function disabled.

Table 307. FUSE2: Port Map Fuses1-(Ports 1 to 16)

Address Offset:8414h-8417h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31: (NumUSB3*2)	RO	0h	USB	Reserved

Bit	Access	Default Value	RST/PWR	Description
((NumUSB3*2)-1) : 0	RO	0h	USB	1:0 – Port 1 3:2 – Port 2 5:4 – Port 3 … 31:30 – Port 16 Bit Description: 00: Port assgned to USB3 01: Port assigned to non-XHCI controller 10: Port assigned to Flex IO mapping. Mapping is based on Soft Straps. 11; Reserved.

Table 308. FUSE3: Port Map Fuses2 (Ports 16 to 32)

Address Offset:8418h-841Bh
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:0	RO	0h	USB	Reserved

Table 309. STRAP1: Flex IO Straps

Address Offset:841Ch-841Fh
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31: (NumUSB)	RO	0h	USB	Reserved
NumUSB3-1:0	RO	0h	USB	FlexIO mapping Each bit corresponds to the appropriately numbered USB3 port (zero based) Bit 0 = port 1, bit 1 = port 2 etc. 0: Port is owned by XHCI 1: Port is not owned by XHCI

Table 310. STRAP2: USB3 Mode Strap

Address Offset:8420h-8423h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31: (NumUSB)	RO	0h	USB	Reserved
NumUSB3-1:0	RO	0h	USB	USB3/SSIC Mode Each bit corresponds to the appropriately numbered USB3 port (zero based) Bit 0 = port 1, bit 1 = port 2 etc. 0: Port is operated in USB3 mode 1: Port is operated in SSIC mode.

Table 311. DFT1: DFT Register1

Address Offset:8430h-8433h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	R0	0h	USB	SS/SSIC DFT CRC (SSDFTCRC): These register bits contain the value of SS DFT CRC
15:12	RO	0h	USB	Rsvd1 (Rsvd1):

Bit	Access	Default Value	RST/PWR	Description
11	RW	0h	USB	DFTLFPSSEL 0: Rxelecidle is driven from GPIO Pin 1: Rxelecidle is Driven as specified by Super Speed DFT LFPS Mode Select (SSDFTLMSEL):
10	RW	0h	USB	Super Speed DFT LFPS Mode Select (SSDFTLMSEL): This bit selects the Super Speed DFT LFPS mode, and will only take effect when Super Speed HBP mode is enabled. 0b: HBP logic will internally loopback TX LFPS as RX LFPS and AFE RX LFPS path to the controller is disconnected. 1b: RX LFPS path works normally
9:6	RW	0h	USB	SS/SSIC DFT CRC Select (SSDFTCRCSEL): These bits select which Super Speed DFT CRC value is reflected in SSDFTCRC bits. In addition, these bits also select which SuperSpeed DFT CRC MSB value is sent to GPIO monitor pin, i.e. sata3gp_gp37 to aid silicon debug. Live version of selected CRC's MSB will be- sent to GPIO monitor pin, i.e. sata3gp_gp37. 0h (default): No SuperSpeed DFT CRC is selected. 1h: Data Payload CRC 2h: Link Management Packet CRC 3h: Transaction Packet CRC 4h: Isochronous Timestamp Packet CRC 5h: Data Packet Header CRC 6h: Link Command Packet CRC 7h: RRAP Packet CRC 8h: Tx/Rx Cfg CRC Others: Reserved Note : CRC types 7 and 8 are only applicable if Port is SSIC Port
5	RO	0h	USB	RSVD
4:0	RW	0h	USB	SS/SSIC DFT CRC Port Select (SSICDFTCPS): One CRC per packet type is shared for all the Super Speed ports. These bits select the Super Speed port for which CRC data will be updated. 000b: (default) No SuperSpeed Port is selected 001b: SS/SSIC Port 0 010b: SS/SSIC Port 1 011b: SS/SSIC Port 2 100b: SS/SSIC Port 3 101b: SS/SSIC PORT4 110b :SS/SSIC Port 5 others : Rsvd

Table 312. DFT2: DFT Register2

Address Offset:8434h-8437h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	0h	USB	HS/HSIC TX CRC (TXCRC): These register bits contain the value of TX CRC. This TX CRC is placed right after the 480MHz XCLKQ.

Bit	Access	Default Value	RST/PWR	Description
15:11	RW	0h	USB	HSIC/UTMI+ DFT Port Select (UTMIDFTPS): One CRC is shared for all the UTMI+ ports. These bits select the UTMI+ port for which CRC data will be updated and loopback status reflected in UTMILPBKSTS. 0h: (default) No UTMI+ Port is selected 1h: UTMI+ Port 0 2h: UTMI+ Port 1 3h: UTMI+ Port 2 4h: UTMI+ Port 3 5h: UTMI+ Port 4 6h: UTMI+ Port 5 7h: UTMI+ Port 6 8h: UTMI+ Port 7 9h: UTMI+ Port 8 Ah: UTMI+ Port 9 Bh: UTMI+ Port 10 Ch: UTMI+ Port 11 Dh: UTMI+ Port 12 Eh: UTMI+ Port 13 Others: Reserved
10:7	RW	0h	USB	Loop Number (UTMILPBKLOOPN_3_0): Number of repeatable fixed pattern within a packet Note: Connect register bit 3 to counter bit 7, register bit 2 to counter bit 5, register bit 1 to counter bit 3, register bit 0 to counter bit 1. Counter bits 6, 4, 2 and 0 will be tied off to 0. Hence, the programmable loop number shall be: 0000b: 0 loop 0001b: 2 loops 0010b: 8 loops 0011b: 10 loops ... 1100b: 160 loops 1101b: 162 loops 1110b: 168 loops 1111b: 170 loops (max) +E27
6:5	RW	0h	USB	Operational Mode (UTMIOPMODE_1_0): Operational Mode in test mode. These signals select between various operational modes: 00b: Normal Operation 01b: Non-Driving 10b: Disable Bit Stuffing and NRZI encoding 11b: Reserved
4	RW	0h	USB	Termination Select (UTMITERMSEL): Termination Select in test mode. This signal selects between the FS and HS terminations: 0b: HS termination enabled 1b: FS termination enabled
3:2	RW	0h	USB	Transceiver Select (UTMIXCVRSELECT_1_0): Transceiver Select in test mode. This signal selects between the LS, FS and HS transceivers: 00b: HS transceiver enabled 01b: FS transceiver enabled 10b: LS transceiver enabled 11b: Reserved
1:0	RW	0h	USB	UTMI+ Loopback Status (UTMILPBKSTS): Loopback Status for port selected by UTMIDFTPS 00b: Reset condition 01b: Comparator has started receiving data and the received data matches with the TX pattern. 10b: Comparator has started receiving data the received data does not match with the TX pattern but there was no assertion of RC error from UTMI. 11b: Comparator has started receiving data and RX ERROR was asserted for at least one clock by UTMI. Note that this does not reflect the status of pattern comparison since RX error from UTMI is unexpected for loopback.

Table 313. DFT3: DFT Register3

Address Offset:8438h-843Bh
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RW	0h	USB	Loopback Pattern (UTMILPBKPAT): 2-byte pattern for loopback Note: This 2-byte pattern will be replicated to the upper 2-byte to form the DW pattern
15:2	RW	0h	USB	Reserved.
1	RW	0h	USB	Loopback Pattern (UTMILPBKPATSEL): Near end loopback pattern generation type: 0b: Fixed pattern 1b: USB2 test packet
0	RW	0h	USB	Loopback Type (UTMILPBKTYPE): Loopback Type in test mode. This signal selects between DNELB and ANELB, and will only take effect if DTUTMILPBKEN is set. 0b: Digital Near-End Loopback (DNELB) 1b: Analog Near-End Loopback (ANELB) Note: Analog Far-End Loopback (AFELB) is not supported

Table 314. DFT4: DFT Register4

Address Offset:843Ch-843Fh
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:NumUSB2	RW	0h	USB	Reserved
(NumUSB2-1):0	RW	0h	USB	Loopback Lane Select (UTMILPBKSEL): Port is selected if the corresponding bit (zero based) is selected Bit 0 = Port 1 Bit 1 = Port 2 Etc.

Table 315. DFT5: DFT Register5

Address Offset:8440h-8443h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:28	RW/L	0h	USB	High Speed Bypass Enable 0000 - Disable all HBP 0001 - Enable SS HBP 0010 - Enable HS HBP 0011 - Enable HSIC HBP 0100 - Enable SSIC HBP Others – Reserved Access is controlled by the “Access Control” lock bit in config space.
27	RW	0h	USB	DFTIDPINSEL Select Between Device and Host Controller in HBP mode 0h : Device Controller is selected 1h : Host Controller is selected
26	RO	0b	USB	Reserved
25	RW	0h	USB	Loopback Enable (UTMILPBKEN): Enable loopback test mode. If asserted, loopback test mode is enabled
24:0	RO	0h	USB	Rsvd

Table 316. XECP_CMDM_STS0 - XECP_CMDM_STS0

Address Offset:8448h-844Bh
Default Value:00000CC1h

Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31	RO	0h	USB	Indicates that IDMA module currently owns the context access :
30	RO	0h	USB	Indicates that ODMA module currently owns currently the context access
29	RO	0h	USB	Indicates that TRM modules owns the context access currently
28	RO	0h	USB	Indicates that Command Manager has requested a context lock
27	RO	0h	USB	Indicates that Command Ring stop command is in progress
26	RO	0h	USB	Indicates that clearing an EP out of schedule is in progress
25	RO	0h	USB	Indicates that current address device command is done by ODMA
24	RO	0h	USB	Indicates that ODMA has an address device command in progress
23	RO	0h	USB	Indicates that updating of EP state is in progress
22	RO	0h	USB	Indicates that doorbell manager is issuing and EP update due to a doorbell ring on an EP that is in stop state
21	RO	0h	USB	Indicates that transfer ring manager is isuing and EP update due to an EP error condition detected
20	RO	0h	USB	Ondicates that transfere ring manager is issuing and EP state update due to stall received
19	RO	0h	USB	Reserved
18	RO	0h	USB	Indicates that a STOP on the Command Ring is in progress
17	RO	0h	USB	Indicates that command ring has a dorrbell pending
16	RO	0h	USB	Indicates that the commend ring is running
15:8	RO	0Ch	USB	Command next capability offset
7:0	RO	C1h	USB	Vendor defined capability ID

Table 317. XECP_CMDM_STS1 - XECP_CMDM_STS1

Address Offset:844Ch-844Fh
Default Value:03FC0000h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:0	RO	03FC0000h	USB	Internal xhci engine status bits: {6'b0,evtm_pcs[7:0], trb_count[96:91], trb_count[83:78], trb_count[70:65]}

Table 318. XECP_CMDM_STS2 - XECP_CMDM_STS2

Address Offset:8450h-8453h
Default Value:00000000h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:0	RO	0h	USB	Internal command manager status bits: { 3'b0, reset_endpt_pst, // 5 bits 29-bits total force_header_pst, // 3 bits reset_device_pst, // 5 bits stop_endpt_pst, // 4 bits update_endpt_pst, // 4 bits set_tr_dequeue_ptr_pst, // 4 bits get_port_bw_pst }; // 4 bits

Table 319. XECP_CMDM_STS3 - XECP_CMDM_STS3

Address Offset:8454h-8457h
Default Value:00000000h
Access: RO;

Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:0	RO	0h	USB	Internal command manager status bits: 8'b0, 1'b0, ep_state, // 3 bits slot_en_ary, 1'b0, slot_state, //2 2'b0, ep_id, // 5 bits internal_cmd_slot_id_extended }; // 8 bits

Table 320. XECP_CMDM_STS4 - XECP_CMDM_STS4

Address Offset:8458h-845Bh
Default Value:00000000h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:0	RO	0h	USB	Internal command manager status bits: cmd_ring_pointer[31:4], 3'b0, cmd_ccs

Table 321. XECP_CMDM_STS5 - XECP_CMDM_STS5

Address Offset:845Ch-845Fh
Default Value:00000000h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:0	RO	0h	USB	Internal command manager status bits: cmd_ring_pointer[63:32]

Table 322. UPORTS_PON_RST_REG - AUX Power PHY Reset

Address Offset:8460-8463h
Default Value:00000000h
Access: WO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:6	RO	0h	USB	RESERVED
3:0	WO	0h	USB	Allow a USB PHY reset being issued by software. Writing to this register with bit set to 1 will reset the USB PHY that is connected to the port. Bit3:0 indicates the port number of the USB PHY

Table 323. HOST_IF_LAT_TOL_CTRL_REG0 - Latency Tolerance Control 0

Address Offset:8464-8467h
Default Value:0h
Access: RW;
Size:32 bits

The Latency Tolerance Control Register is used by SW to control which BELT is returned when this register is read. SW shall write to this register to program a Slot-ID, Port-ID and BELT Select to determine which BELT is selected. When this register is read the selected BELT is returned.

Bit	Access	Default Value	RST/PWR	Description
31:30	WO	0h	USB	BELT Select (): This field determines what value will be selected to read back from SW when reading this register 0: Returns the SW programmed Latency Tolerance Value 1: Returns the Lowest BELT in the Host 2: Returns the BELT for the requested Slot-ID (Slot Select) 3: Returns the BELT for the requested Port-ID (Port Select)
29:20	RO	0h	USB	Rsvd1 (Rsvd1):
19:16	WO	0h	USB	Port Select (): Used to select the BELT for a given Port # when the BELT Select is programmed to select the Port-ID (this field is 0 based)
15:12	RO	0h	USB	Rsvd1 (Rsvd1):
11:5	RO	0h	USB	BELT Value (BELTV) [11:5]: Value of selected BELT is return in this field
4:0	RW	0h	USB	Reads will return: BELT Value (BELTV) [4:0]: Value of selected BELT is return in this field Writes will control : Slot Select (): Used to select the BELT for a given Slot # when the BELT Select is programmed to select the Slot-ID (this field is zero based)

4.7.4.4 Legacy Support Extended Capability

Base Offset of this capability from MBAR is 846Ch

Table 324. USBLEGSUP - USB Legacy Support Capability

Address Offset:846C-846Fh
Default Value:00000001h
Access: RO; RW;
Size:32 bits
This register is modified and maintained by BIOS

Bit	Access	Default Value	RST/PWR	Description
31:25	RO	0h	USB	Rsvd2 (Rsvd2):
24	RW	0h	USB	HC OS Owned Semaphore (HCOSOS):
23:17	RO	0h	USB	Rsvd1 (Rsvd1):
16	RW	0h	USB	HC BIOS Owned Semaphore (HCBIOSOS):
15:8	RW/S	22h / 25h See Note	USB	Next Capability Pointer (NextCP):
7:0	RO	1h	USB	Capability ID (CID):

Note:

If PDOCapability = 0, Next Capability Pointer = 25h

Table 325. USBLEGCTLSTS - USB Legacy Support Control Status

Address Offset:8470-8473h
Default Value:00000000h
Access: RO; RW; RW1C;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31	RW1C	0h	USB	SMI on BAR (SMIBAR):
30	RW1C	0h	USB	SMI on PCI Command (SMIPCIC):
29	RW1C	0h	USB	SMI on OS Ownership Change (SMIOSOC):
28:21	RO	0h	USB	Rsvd4 (Rsvd4):

Bit	Access	Default Value	RST/PWR	Description
20	RO	0h	USB	SMI on Host System Error (SMIHSE):
19:17	RO	0h	USB	Rsvd3 (Rsvd3):
16	RO	0h	USB	SMI on Event Interrupt (SMIEI):
15	RW	0h	USB	SMI on BAR Enable (SMIBARE):
14	RW	0h	USB	SMI on PCI Command Enable (SMIPCICE):
13	RW	0h	USB	SMI on OS Ownership Enable (SMIOSOE):
12:5	RO	0h	USB	Rsvd2 (Rsvd2):
4	RW	0h	USB	SMI on Host System Error Enable (SMIHSEE):
3:1	RO	0h	USB	Rsvd1 (Rsvd1):
0	RW	0h	USB	USB SMI Enable (USBSMIE):

4.7.4.5 Port Disable Override Capability

If this Extended Capability exists, it must be located in the Always ON power well to retain the "Write Once" attribute – which is necessary to maintain the integrity of the Port Disable setting.

Base Offset = 84F4h

Capability Register
Address Offset: 00 - 03

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	0h	NA	Reserved
15:8	RW/S	3h	USB	Next Capability Pointer
7:0	RW/S	C6h	USB	Capability ID

Table 326. USB2 – Port Disable Override
Address Offset: 04 – 07h

Bit	Access	Default Value	RST/PWR	Description
31: NumUSB2 (NumUSB2-1):0	RO RWO	0h 0h	USB USB	Rsvd1 (Rsvd1) : USB2 Port Disable Override (USB2PDO) : A '1' in a bit position prevents the corresponding USB2 port from reporting a Device Connection to the XHC. This applies across all USB2 protocol ports

Table 327. USB3 Port Disable Override
Address Offset: 08 – 0Bh

Bit	Access	Default Value	RST/PWR	Description
31: NumUSB3 (NumUSB3 -1):0	RO RWO	0h 0h	USB USB	Rsvd1 (Rsvd1) : USB3 Port Disable Override (USB3PDO) : A '1' in a bit position prevents the corresponding USB3 port from reporting a Device Connection to the XHC. This applies across all USB3 protocol ports

4.7.4.6 HW State Access Capability

This memory range is reserved for use by the Host Controller HW to assist in save and restore of HW state. This memory range is not intended to be read or written by SW.

Base Offset = 8500h
This capability starts at offset 8500h from MBAR.

Table 328. Capability ID register
Address Offset: 00 – 03h

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	00h	USB	Reserved
23:16	RO	4h	USB	Save Length Indicates the number of DWords in this capability starting at offset 04h, that need to be saved and restored
15:8	RO	40h	USB	Next Capability Pointer
7:0	RO	C7h	USB	Supported Protocol ID

Table 329. HWST1 - HW State 1
Address Offset 04- 07h

Bit	Access	Default Value	RST/PWR	Description
31:00	RW	X	USB	Implementation defined HW state: SW must not access this register.

Table 330. HWST2 - HW State 2
Address Offset 08- 0Bh

Bit	Access	Default Value	RST/PWR	Description
31:00	RW	X	USB	Implementation defined HW state: SW must not access this register.

Table 331. HWST3 - HW State 3
Address Offset 0C- 0Fh

Bit	Access	Default Value	RST/PWR	Description
31:00	RW	X	USB	Implementation defined HW state: SW must not access this register.

Table 332. HWST4 - HW State 4
Address Offset 10- 13h

Bit	Access	Default Value	RST/PWR	Description
31:00	RW	X	USB	Implementation defined HW state: SW must not access this register.

4.7.4.7 Config Space Register Mirror

Base Offset: 8600h

Table 333. Capability Register
Address Offset: 00 – 03 (from the base offset)

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	0h	NA	Reserved
15:8	RW/S	40h*	USB	Next Capability Pointer See Note below on configurability
7:0	RW/S	C2h	USB	Capability ID

Note:
Next Capability Pointer=80h if XHCIDbC = False, but NumSSICports>0.
Next Capability Pointer=00h if XHCIDbC = False and NumSSICports=0.

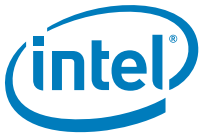


Table 334. FSLSPS – FS/LS Port Staggering Control

Table 335. Address Offset: 98-9Ch **HSCFG1 - High Speed Configuration 1**
Address Offset: A0-A3h

Table 336. HSCFG2 - High Speed Configuration 2
Address Offset: A4-A7h

Table 337. SSCFG1 - SuperSpeed Configuration 1
Address Offset: A8-ABh

Table 338. U2OCM<N> - XHCI USB2 Overcurrent Pin N Mapping
Address Offset: B0-B3h, ... (B0h+(NumOC-1)*4) to (B3h+(NumOC–1)*4) <upto C7h>

Table 339. U3OCM<N> - XHCI USB3 Overcurrent Pin N Mapping
Address Offset: D0-D3h, ... (D0h+(NumOC-1)*4) to (D3h+(NumOC–1)*4) <upto E7h>

Table 340. MANID - Manufacturing Process ID
Address Offset: F8-FBh

4.7.4.8 XHCI Debug Capability

Base Offset = 8700h

Table 341. Debug Capability ID Register (DCID)
Memory Mapped IO Space
Address Offset:00-03h
Access: RO; RW/S;
Size:32 bits
This register is modified and maintained by BIOS

Bit	Access	Default Value	RST/PWR	Description
31:21	RW	0h	NA	Reserved
20:16	RW/S	05h	USB	Debug Capability Event Ring Segment Table Max (DCERST Max)
15:8	RW/S	10h	USB	Next Capability Pointer
7:0	RW/S	0Ah	USB	Capability ID

Table 342. Debug Capability Doorbell Register (DCDB)
Memory Mapped IO Space
Address Offset:04h-07h
See xHCI spec for details

Table 343. Debug Capability Event Ring Segment Table Size Register (DCERSTSZ)
Memory Mapped IO Space
Address Offset:08h-0Bh
See xHCI spec for details

Table 344. Debug Capability Event Ring Segment Table Base Address Register (DCERSTBA)
Memory Mapped IO Space
Address Offset:10-17h
See xHCI spec for details

Table 345. Debug Capability Event Ring Dequeue Pointer Register (DCERDP)
Memory Mapped IO Space
Address Offset:18-1Fh
See xHCI spec for details

Table 346. Debug Capability Control Register (DCCTRL)
Memory Mapped IO Space

Address Offset:20-23h
Default Value:0005_000Ah
Access: RO; RW1C; RW1S; RW
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31	RW	0h	USB	Debug Capability Enable (DCE)
30:24	RO	00h	USB	Device Address
23:16	RO	00h	USB	Debug Max Burst Size: LPT-LP USB Debug Device does not support bursting.
15:5	RO	000h	NA	Reserved
4	RW1C	0	USB	DbC Run Change (DRC)
3	RW1S	0	USB	Halt IN TR (HIT)
2	RW1S	0	USB	Halt OUT TR (HOT)
1	RW	0	USB	Link Status Event Enable (LSE)
0	RO	0	USB	DbC Run (DCR)

Table 347. Debug Capability Status Register (DCST)

Memory Mapped IO Space
Address Offset:24-27h
See xHCI spec for details

Table 348. Debug Capability Port Status and Control Register (DCPORTSC)

Memory Mapped IO Space
Address Offset:28-2Bh
See xHCI spec for details

Table 349. Debug Capability Context Pointer Register (DCCP)

Memory Mapped IO Space
Address Offset:30-37h
See xHCI spec for details

Table 350. Debug Capability Device Descriptor Info Register 1 (DCDDI1)

Memory Mapped IO Space
Address Offset:38-3Bh
See xHCI spec for details

Table 351. Debug Capability Device Descriptor Info Register 2 (DCDDI2)

Memory Mapped IO Space
Address Offset:3C-3Fh
See xHCI spec for details

4.7.4.9 Vendor Defined Debug Capability Config Registers

This section describes configuration bits that provide proprietary control for USB Debug Device.
Note: bU1DevExitLat and bU2DevExitLat fields returned in BOS Descriptor read will be taken from the corresponding fields from the Host Controller space.

Base Offset = 8740h

Table 352. Debug Capability Descriptor Parameters

Memory Mapped IO Space
Address Offset:00-03h
Default Value:0000_0000h
Access: RO; RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	0h	NA	Reserved

Bit	Access	Default Value	RST/PWR	Description
23:16	RW	00h	USB	Max Power Field This field will be used by USB Debug Device to report maximum power consumption when the device is fully operational. This value is returned by bMaxPower field in response to Configuration Descriptor read from the debug device.
15:8	RW/S	30h*	USB	Next Capability Pointer See Note below for configurability
7:0	RW/S	C3h	USB	Capability ID

Note:
Next Capability pointer = 00h if NumSSICPorts = 0

Table 353. DBGDEV_CTRL_TRM_REG1 – Debug Device Control Transfer Manager (TRM)

Memory Mapped IO Space
Address Offset:04-07h
Default Value:0C20 1103h
Access: RW;
Size:32 bits
This register contains fields which control the behavior of the Transfer Manager in the Debug Device logic implemented in DbC.

Bit	Access	Default Value	RST/PWR	Description
31	RW	0h	USB	Reserved. It must set to 0 .
30:28	RO	0h	USB	RESERVED
27	RW	1h	USB	This bit has been modified for its usage since PPTA0. It is used to allow NO-OP TRB to be treated in a same way as link TRB. In other words, it will update the internal context when it is fetched while the internal context cache TRB FIFO is empty. 1: enabled the cache function 0: disable the function
26	RW	1h	USB	This is a special internal condition enable for CPL engine which it enables all EP halt conditions detected to cause the proper actions in a response. 1: enabled 0: disabled Note: only default condition of 1 is validated.
25	RO	0h	USB	RESERVED
24	RW	0h	USB	This is a special internal branch condition control in XFER engine which does the EP transfer ring process. When this bit is set, the XFER will not continue even if the next TRB is identified as a non DMA TRB. The engine will then wait for the next scheduled request for this EP. 1: enabled the branch condition 0: disabled.
23	RW	0h	USB	When ERDP register is updated by software, it is expected as an atomic function since this is a 64bit register. It is expected that the ERDP (64bits register) is updated together when ERDP high 32 is written. We have this bit designed to ignore the atomic operation required from software for ERDP low 32bits. When this bit is set to 1, it will update the ERDP low 32bits when software issues a CPU write to the ERDP low 32 bit. 1: ignore atomic operation 0: not ignore.
22	RW	0h	USB	Setting this bit to 1 will force an internal doorbell ring on the EP that it has received a response.
21	RO	0h	USB	RESERVED
20	RW	1h	USB	0: Disable timeout of TRB error processing. 1: Enable timeout of a TRB processing in few critical states that possibly have a deadlock for unexpected reason. A vendor defined completion code is generated in the event of a timeout during TRB processing.
19	RO	0h	USB	RESERVED
18	RW	0h	USB	This bit is modified to enable the NOOP TRB as a TD when Missing Service Interval Error has encountered. This is only for PPT B0, LPT and CB. 1: enabled 0: disabled

Bit	Access	Default Value	RST/PWR	Description
17:14	RO	0h	USB	RESERVED
13	RW	0h	USB	0: Bulk and interrupt endpoints use burst size defined by endpoint context. 1: Force the Bulk and Interrupt endpoints use a burst size of 1.
12	RW	1h	USB	0: ENT bit is ignored. 1: ENT bit is processed. The transfer engine will service the next TRB.
11	RW	0h	USB	Setting this bit to 1 will force the transfer engine to set the packet boundary flag. This flag is an important flag which may cause a deadlock. This is a safety feature that we pluged in.
10	RO	0h	USB	RESERVED
9	RW	0h	USB	Setting this bit to 1 will force the transfer engine state machine to exit the CPL_WAIT state. This is designed to avoid unexpected deadlock in CPL_WAIT state.
8	RW	1h	USB	0: Disable internal TRB cache invalidation. 1: Enable internal TRB cache invalidation auto detect function This will allow engine to handle more than 4TRBs per packet.
7:6	RO	0h	USB	RESERVED
5	RW	0h	USB	Enable a function which we can clear mask of an EP on any response of that EP. 0: Clear the scheduler mask normally. 1: Clear the scheduler mask on each received packet.
4	RW	0h	USB	This bit is designed to allow XFER engine to do a transfer without checking against the available port credit. 0: Advertises accurate buffer credit information to the scheduler. 1: Advertises non-zero buffer credits to the scheduler. (e.g. never backpressure back on buffer credit information)
3	RO	0h	USB	RESERVED
2	RW	1h	USB	Generation of Completion Code for LINK/NOOP TRB
1	RO	0h	USB	RESERVED
0	RW	1h	USB	0: Disable TD pacing for IN endpoint. 1: Enable TD pacing for IN endpoints.

Table 354. DBGDEV_CTRL_ODMA_REG – Debug Device Control ODMA

Memory Mapped IO Space
Address Offset: 08- 0Bh
Default Value:0004 2000 h
Access: RO; RW;
Size:32 bits
This register contains a number of fields that provide a specific level of configurability for the OUT DMA that is part of Debug Device logic.
This configurability is above and beyond that defined in the xHCI specification.

Bit	Access	Default Value	RST/PWR	Description
31:19	RO	0h	USB	RESERVED
18	RW	1h	USB	Setting this field will enable ACK FIFO credit accounting. ODMA will ensure that ample room exists in the ACK FIFO for expected device responses prior to initiating a given DP
17:14	RO	0h	USB	RESERVED
13	RW	1h	USB	Setting this field will enable ACK FIFO individual credit accounting mechanisms for Async vs. Periodic Endpoints. ODMA will ensure that ample room exists in the ACK FIFO for expected device responses prior to initiating a given DP
12:9	RO	0h	USB	RESERVED
8	RW	0h	USB	Setting this field generates a pulse that clears the ownership of the context semaphore that is shared between the Out DMA Response and Completion Finite State Machines
7	RW	0h	USB	Setting this field generates a pulse that implicitly returns all of the Out DMA ACK credits on all ports
6	RO	0h	USB	RESERVED

Bit	Access	Default Value	RST/PWR	Description
5	RW	0h	USB	Setting this field generates a pulse that returns the Out DMA Completion Finite State Machine into the IDLE state
4	RW	0h	USB	Setting this field generates a pulse that returns the Out DMA Response Finite State Machine into the IDLE state
3	RW	0h	USB	Setting this field generates a pulse that returns the Out DMA Read Finite State Machine into the IDLE state
2:0	RO	0h	USB	RESERVED

Table 355. DBGDEV_CTRL_IDMA_REG – Debug Device Control IDMA

Memory Mapped IO Space
Address Offset: 0C- 0Fh
Default Value:0000 0000h
Access: RW;
Size:32 bits
This register contains a number of fields that provide a specific level of configurability for the IN DMA in the Debug Device logic.

Bit	Access	Default Value	RST/PWR	Description
31	RO	0h	USB	RESERVED
30	RW	0h	USB	Setting this field will allow the Event Manager to treat either Transfer Manger (when 1) or Completion Engine (when 0) Event requests with higher priority. This bit is used by Event Manager
29	RW	0h	USB	Setting this field will allow the Doorbell Manager to post events on a given transfer ring
28:25	RO	0h	USB	RESERVED
24	RW	0h	USB	0: Flush the Asynchronous Address FIFO when bit[18] is strobed 1: Flush the Periodic Address FIFO when bit[18] is strobed
23:19	RO	0h	USB	RESERVED
18	RW	0h	USB	Setting this field will generate a strobe causing a give Periodic or Asynchronous Address FIFO to flush. FIFO flushed is a function of bits [25:19]
17	RO	0h	USB	RESERVED
16	RW	0h	USB	0: Default IDMA Pointer Buffer Room to a default value of 8. Requires a strobe of bit[3] to take effect. 1: Default IDMA Pointer Buffer Room to a default value of 4. Requires a strobe of bit[3] to take effect.
15	RW	0h	USB	Setting this field will prohibit IDMA from automatically dropping received DPs when a given endpoint currently has no outstanding transactions
14	RW	0h	USB	Setting this field will prohibit IDMA from automatically dropping received DPs when a given endpoint is currently in a flow controlled state
13:8	RO	0h	USB	RESERVED
7	RW	0h	USB	Setting this field generates a pulse that clears the ownership of the context semaphore that is shared between the IN DMA Acknowledge and Data Mover Finite State Machines
6	RW	0h	USB	Setting this field generates a pulse that returns the IN DMA Data Mover Finite State Machine into the IDLE state
5	RW	0h	USB	Setting this field generates a pulse that returns the IN DMA Acknowledge Finite State Machine into the IDLE state
4	RW	0h	USB	Setting this field generates a pulse that implicitly returns all of the IN DMA Data Packet credits on all ports
3	RW	0h	USB	Setting this field generates a pulse that clears all the Read and Write Pointers associated with the various DMA Address FIFOs causing them to appear empty
2:0	RO	0h	USB	RESERVED

Table 356. DGGDEV_CTRL_TRM_REG2 – Debug Device Control Transfer Manager (TRM)

Memory Mapped IO Space
Address Offset: 10- 13h
Default Value:F080 0084h

Access: RW;
Size:32 bits
This register contains fields which control the behavior of the Transfer Manager in the Debug Device logic. The functions controlled by this register are made available largely for debug/diagnostic purposes.

Bit	Access	Default Value	RST/PWR	Description
31	RW	1h	USB	This bit is added for bug FR2601. It is for cache invalidate case where xHC engine needs to insert wait states for completion engine when the completion has received a short packet before XFER engine has finished the TRB fetch for this packet at its packet boundary. 1: enables the feature 0: disabled
30	RW	1h	USB	This bit is added for bug FR2642. It is to delay the completion engine to generate an event due to internal error conditions that halted an EP until XFER engine has reached a packet boundary. 1: enabled 0: disabled
29	RW	1h	USB	This bit is added for bug FR2639. It enables the internal functions where xHC engine needs to immediatedly serve the EP again. 1: enabled 0: disabled
28	RW	1h	USB	This bit is added for bug FR2495. It enables that error completion code of the first error condition detected within an TD so that we can report the same error completion codes for all other TRBs within this TD. 1: enables the feature 0: disabled
27	RW	0h	USB	This bit disables a new feature where xHC engine will have an ODMA FIFO added for the commands between TRM and ODMA so that we can avoid the back-pressure situation due to the number of outstanding PCIe read limitation. This is for performance enhancement. 1: feature disabled 0: enabled
26:24	RO	0h	USB	RESERVED
23	RW	1h	USB	This bit is added for bug FR2283. This is to ensure only 1 clear pulse generated when a completion has received. 1: enabled 0: disabled
22:21	RO	0h	USB	RESERVED
20	RW	0h	USB	This bit enables a new feature where the completion engine of TRM can check the credit returned from remote device to not excced its max burst size. If it does, we will keep the internal credits in the context to the max burst size so that xHC engine will not transmit more than max burst size. Note: CB has this bit default set to 0 PPT B0 and LPT will have this bit set to 1. 1: enabled 0: disabled
19	RW	1h	USB	This bit enables an internally detected deadlock situation being treated as an TRB_ERR when reports the event. This is an internal debug function. 1: enabled 0: disabled
18	RO	0h	USB	RESERVED
17	RW	0h	USB	This bit enables xHC engine to evaluate the next TRB even if the EP is at the end of a TD. 1: enables the feature 0: disables the feature
16:15	RO	0h	USB	RESERVED
14	RW	0h	USB	New feature added to prevent the back-pressure from ODMA due to the fact that it ran out of ODMA timeout timer resources. This is for performance enhancement. We have put into the ODMA credit is part of resource calculation before TRM allows the next scheduling for OUT EP. 1: enables this feature 0: Disables this feature

Bit	Access	Default Value	RST/PWR	Description
13	RW	0h	USB	The xHC engine has a feature that can check with Receive Port Credit per root port to whether or not allowed the next schedule onto this port. This is for performance enhancement. This bit enables this feature 1: Feature enabled 0: Feature disabled
12:8	RO	0h	USB	RESERVED
7	RW	1h	USB	1: enable a packet pace function under a special condition. This is an internal feature to XFER engine. It is not expected to be used other than default. 0: disable this function.
6:4	RO	0h	USB	RESERVED
3	RW	0h	USB	1: enable the address device command to query a port credit before it is executed in ODMA engine. 0: Disable this function.
2	RW	1h	USB	1: enable the credit redeem when a port is in NC state. 0: Disable the credit redeem
1	RO	0h	USB	RESERVED
0	RW	0h	USB	1: enable XFER engine to process a reserved TRB type as a NO-OP TRB 0: report TRB ERR for reserved TRB type.

Table 357. DBGDEV_CTRL_REG1 – Debug Device Control Register 1

Memory Mapped IO Space
Address Offset: 14- 17h
Default Value:0000 000Ch
Access: RW;
Size:32 bits
This register contains fields which control the behavior of the Debug Device logic

Bit	Access	Default Value	RST/PWR	Description
31:16	RW	0h	USB	Per SS Port masking of Debug Capability. When a bit is set, the corresponding SS port will not attempt training as a Debug Device Capable upstream device. When a bit is not set, the corresponding SS port will train as Debug Device capable upstream port when DCE = 1
15: 4	RW	0h	USB	Reserved
3	RW	1h	USB	1: enable setting of Halt flag on TD Babble error. TD Babble will trigger Stall event. 0: disable setting of Halt flag on Babble error. TD Babble will not trigger a Stall event
2	RW	1h	USB	1: enable setting of Halt flag on TRB Error event. TRB error will trigger Stall event 0: disable setting of Halt flag on TRB Error. TRB error will not trigger Stall event
1	RW	0h	USB	1: enable generation of STALL event for vendor defined errors. Vendor defined errors are treated as halt condition. 0: Disable generation of STALL event for vendor defined errors. Vendor defined errors are not treated as halt conditions
0	RW	0h	USB	1: disable handling of TD Babble as a fatal error 0: TD Babble is handled as fatal error, and EP is stalled.

Table 358. DBCCTL – DbC Control

MMIO Space
Address Offset : 18 – 1Bh

Bit	Access	Default Value	RST/PWR	Description
31:02	RO	0h	USB	Reserved
1	RW	0b	USB	Force DCE Mode 0: When DCE is set, the DbC switches to Mode 2 1: When DCE is set, the DbC switches to Mode 3

Bit	Access	Default Value	RST/PWR	Description
0	RW	0b	USB	Force Disconnect upon DCE : If this bit is set by BIOS, the DbC will temporarily Disconnect from the remote host if the DCE is set, and shortly thereafter re-connect. This allows the DbC to switch from Mode1 to Mode2 or Mode 3 operation upon DCE being set.

4.7.4.10 SSIC Policy and Implementation Specific Registers

Chicken bits and Policy bits associated with SSIC.
This capability starts at offset 8800h from MBAR.

Table 359. Capability ID Register
Address Offset: 00 – 03h

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	00h	USB	Reserved
15:8	RO	40h	USB	Next Capability Pointer
7:0	RO	C4h	USB	Supported Protocol ID

Table 360. SSIC Global Configuration Control
Address Offset:04h – 07h,

Bit	Access	Default Value	RST/PWR	Description
31:18	RO	0h	NA	Reserved
17:16	RW	See Description	USB	T_ACT_H8_MARGIN Specifies the margin time added to the tActivate spec time of 100us in T_ACT_H8_TIME. 11: Reserved 10: 50us 01: 20us (default for ModPHY) 00: 10us (default for MIPI MPHY)
15:4	RO	0h	NA	Reserved
3	RW	See Description	USB	BB_PLL_OVRD_DURING_PWM Override BB PLL clock gating during PWM mode. 1: Keep BB PLL up during PWM mode (default for ModPHY) 0: No override (default for MIPI MPHY)
2	RW	0h	USB	CMN_LANE_PWRGATE_DIS This will disable the MPHY common lane power gate.
1	RW	0h	USB	HS_CLK_GATE_DIS This will disable the HS Clock gate request from XHCI to MIPI PLL.
0	RW	0h	USB	PWM_CLK_GATE_DIS This will disable the PWM Clock gate request from XHCI to MIPI PLL.

Table 361. SSIC Configuration Register 1
Address Offset: 08h-0bh
Port 1 ... N : 08h, 38h, ... ,(08h + (NumSSICPorts-1)*30h)
Upto a maximum of 4 SSIC Ports

Bit	Access	Default Value	RST/PWR	Description
31:30	RW	2/h	USB	NUM_RRAP_ATTEMPT Specify the number of RRAP access attempt if there was tRRAPInitiatorResponse timeout.

Bit	Access	Default Value	RST/PWR	Description
29:22	RW	08h	USB	TX_MIN_STALL (TX_Min_STALL_NoConfig_Time_Capability in MIPI PHY Spec). PA will ensure TX_MIN_STALL time in STALL before entering HS-BURST or HIBERN8. Specifies minimum time in SI in STALL state.
21:17	RW	14h	USB	PWM_EXIT_TIME This will be max of RX_Min_ActivateTime_Capability and TX_Min_SAVE_Config_Time_Capability in MIPI PHY Specs) Specifies minimum activate time needed in 10us steps. PA will wait PWM_EXIT_TIME time after exiting PWM to start HS-BURST. SSIC spec requires it to be at 100us. 0000 – 10us 0001 – 20us ..... 1110 – 150us 1111 – 1ms For speedup mode this time would be in 1us steps.
16	RW	0		DSP_DISC_BURST_CLOSE_RRAP Send BURST Closure RRAP for DSP Disconnect Don't send Burst Closure RRAP for DSP Disconnect. For device PWM exit would be indication for DSP Disconnect.
15:13	RW	03h	USB	TX_MIN_ACTIVATE_DEFAULT (TX_Min_ActivateTime in MIPI PHY Spec) Specifies minimum activate time pwm_exit_timeneeded in 500us steps. PA will wait TX_MIN_ACTIVATE time after DISABLE H8 exit to start of PWM Burst. 000 – 0.5ms 001 – 1ms ..... 111 – 3.5ms SSIC spec requires it to be at 1.5ms. For speedup mode this time would be 50us to 350us in steps of 50us.
12	RW	0h	USB	RRAP_BYPASS Enables DFx Loopback test mode where RRAP command / response is bypassed for HS_CONFIG and PWM_BURST_CLOSURE. Host will still perform initial enter and exit PWM mode with no RRAP transfers.
11			USB	Reserved
10:8	RW	0h	USB	T_ACT_H8_EXIT Specifies minimum time in 100us steps for T_ACTIVATE_TIME to exit H8 , with margin added from register T_ACT_H8_MARGIN based on PHY characteristic. Val: Si Time / Fast Sim Time 000: 110us / 10us 001: 210us / 20us ... 110: 710us / 70us 111: 5ms / 500us Spec required timing is 100us.
7:5	RW	0h	USB	MIN_HIBERN8_TIME Minimum time in HIBERN8 state Val: Si Time / Fast Sim Time 000 – 110us / 10us 001 – 210us / 20us ..... 110 – 710us / 70us 111 – 5ms / 500us PA will ensure MIN_HIBERN8_TIME in its TX HIBERN8. For speedup mode this time will be from 10us to 80us in steps of 10us.
4	RW	0b/1b SPT uses '1b'	USB	SSICRATE 1 – A Series (default for ModPHY) 0 – B Series (default for MIPI MPHY)

Bit	Access	Default Value	RST/PWR	Description
3:2	RW	0h	USB	HSGEAR 0=HS-G1 1=HS-G2 2=HS-G3 HS Gear information will be latched for controller use once program done is asserted and later when PWM is done.
1:0	RW	0h	USB	SSICLANE 0=Single lane 1=Bi-lane 2=Quad-lane

Table 362. SSIC Configuration Register 2

Address Offset: 0Ch-0Fh
Port 1 ... N : 0Ch, 3Ch, ... ,(0Ch + (NumSSICPorts-1)*30h)
Upto a maximum of 4 SSIC Ports

Bit	Access	Default Value	RST/PWR	Description
31	RW	0	USB	SSIC_PORT_UNUSED This indicates that no SSIC device is connected to the port and PORTSC register would always reflect DISCONNECTED. Once PROG_DONE is set, this bit cannot be changed.
30	RW	0	USB	PROG_DONE BIOS will program this bit once SSIC profile programming is done. SSIC will enable the MPHY and local PLL once this bit is set.
29:26	RW	1h	USB	NUM_OF_MK0 Number of MK0 which transmitter will send before sending any data. . This field is multiple of 4. e.g. 0000 – 4 MK0 0001 – 8 MK0 ..... 1111 – 64 MK0
25	RW	0h	USB	DISABLE_SCRAMBLING This bit will disable scrambling in HS-BURST. The Driver should program DISABLE_SCRABLING on the remote side through profile.
24:21	RW	4h	USB	RETRAIN_TIME Corresponds to time in 10us to detect improper training of the local and remote M-RX as part of HS-BURST entry. 0000 – Disabled 0001 – 10us 1110 – 140us ..... 1111 – 1ms SSIC Spec specific 40 to 50us
20:16	RW	1h	USB	PHY_RESET_TIME Corresponds to time in 100ns, PA will drive PHY RESET for MIPI PHY. This is the minimum time PA will ensure PHY reset is asserted.
15:8	RW	1Fh	USB	LRST_TIME Corresponds to time in 100us PA will drive DIF-P for line reset. MIPI PHY specifies 3.1 ms Minimum. When this time is changed the corresponding tx line reset timer MPHY registers need to be matched.0x00 – 100us 0x01 – 200us ... 0x1E – 3.1ms ... 0xFE – 25.5ms 0xFF – 100ms For speedup mode this time will be in steps of 5us.

Bit	Access	Default Value	RST/PWR	Description
7:0	RW	46h	USB	ACTIVATE_LRST_TIME (Corresponds to tResetDIFN) Specifies in step of 1ms period of time a DSP is required to drive a DIF-N prior to a LINE-RESET. SSIC spec defined range is 60-80ms. For speedup mode this time will be from 5us to 400us in steps of 5us.

Table 363. SSIC Configuration Register 3

Address Offset: 10h-13h
Port 1 ... N : 10h, 40h, ... ,(10h + (NumSSICPorts-1)*30h)
Upto a maximum of 4 SSIC Ports

Bit	Access	Default Value	RST/PWR	Description
31:28	RW	4h	USB	U0_STALL_TO Time in 2^[U-STALL_TO] clock for U0 STALL entry. If there is no packet in arbiter for U0_STALL_TO time, PA will enable U0 STALL if DISABLE_U0_STALL is not set. 0000 – 0011 (Not recommended) 0100 – 16 SSIC HS CLK .... 1111 – 32768 SSIC HS CLK
27	RW	0h	USB	MPHY TEST_MODE_EN When this bit is set, controller would not initiate any PWM once it enters PWM Mode. It will wait for tester to send Loopback RRAP Command.
26	RW	0h	USB	DL_PWR_GATE_DIS This will disable the MPHY data lane power gate. This will be effective in DISBALED, U3 and U2 state and it will override SSIC_PG_U3_DIS and SSIC_PG_U2_DIS.
25:21	RW	2h	USB	HIBERN8_ENTER_TX The time PA will drive DIF-N after last bit of Line-CFG before entering H8. In steps of 50ns. Legal range is 50 to 1000ns.
20:19	RW	1h	USB	LUP_LDN_TIMER_MAX 00: 10 us 01: 250 us 10: 1000us /1ms 11: (Timer is disable and don’t transmit LDN)
18:3	RO	0	USB	Reserved
2	RW	0h	USB	DISABLE_U0_STALL This bit will disable the STALL entry in U0
1	RW	0	USB	SSIC_PG_U3_DIS This disables MPHY DL PG during U3. For S0IX, this bit should remain cleared.
0	RW	0	USB	SSIC_PG_U2_DIS This disables MPHY DL PG during U2.

Table 364. SSIC Configuration Register 4

Address Offset: 14h-17h
Port 1 ... N : 14h, 44h, ... ,(14h + (NumSSICPorts-1)*30h)
Upto a maximum of 4 SSIC Ports

Bit	Access	Default Value	RST/PWR	Description
31:24	RW	64h	USB	LC_MAX_TIMER In steps of 1us. Default 100us
23:16	RW	64h	USB	ENTRY_TIMER_MAX In steps of 1us. Default 100us

Bit	Access	Default Value	RST/PWR	Description
15:8	RW	64h	USB	HP_PEND_TIMER_MAX In steps of 1us. Default 100us
7:0	RW	64h	USB	CRD_PEND_TIMER_MAX In steps of 1us. Default 100us

Table 365. SSIC Loopback Config Register

Address Offset: 18h-1Bh
Port 1 ... N : 18h, 48h, ... ,(18h + (NumSSICPorts-1)*30h)
Upto a maximum of 4 SSIC Ports

Bit	Access	Default Value	RST/PWR	Description
32:8			USB	RESERVED
7:4	RO	0h	USB	LOOPBACK_EN This Register is used to enable Conformance Loopback in the Target in the specified PAIR.. Bit [0]: • Writing 1'b1 enables the loopback mode in PAIR0. • Writing 1'b0 shall have no effect. Bit [1]: • Writing 1'b1 enables the loopback mode in PAIR1. • Writing 1'b0 shall have no effect. Bit [2]: • Writing 1'b1 enables the loopback mode in PAIR2. • Writing 1'b0 shall have no effect. Bit [3]: • Writing 1'b1 enables the loopback mode in PAIR3. • Writing 1'b0 shall have no effect.
3:0	RO	0h	USB	RX LOOPBACK CNTR RESET Reset RX_BURST_COUNT and RX_ERR_COUNT, write only, self-clearing. Bit [0] for PAIR0 Bit [1] for PAIR1 Bit [2] for PAIR2 Bit [3] for PAIR3

Table 366. SSIC Loopback Burst Count Register

Address Offset: 1Ch-1Fh
Port 1 ... N : 1Ch, 4Ch, ... ,(1Ch + (NumSSICPorts-1)*30h)
Upto a maximum of 4 SSIC Ports

Bit	Access	Default Value	RST/PWR	Description
31:24	RO	00h	USB	RX_BURST_COUNT_LANE3 RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET.
23:16	RO	00h	USB	RX_BURST_COUNT_LANE2 RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET.

Bit	Access	Default Value	RST/PWR	Description
15:8	RO	00h	USB	RX_BURST_COUNT_LANE1 RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET.
7:0	RO	00h	USB	RX_BURST_COUNT_LANE0 RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET.

Table 367. SSIC Loopback Error Count Register

Address Offset: 20h-23h
Port 1 ... N : 20h, 50h, ... ,(20h + (NumSSICPorts-1)*30h)
Upto a maximum of 16 SSIC Ports

Bit	Access	Default Value	RST/PWR	Description
32:24	RO	00h	USB	RX_ERR_COUNT_LANE3 RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET.
23:16	RO	00h	USB	RX_ERR_COUNT_LANE2 RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET.
15:8	RO	00h	USB	RX_ERR_COUNT_LANE1 RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET.
7:0	RO	00h	USB	RX_ERR_COUNT_LANE0 RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET.

4.7.4.11 SSIC Local and Remote Profile Registers

This capability starts at offset 8900h from MBAR.

Table 368. SSIC Capability Register

Address Offset: 00h - 03h

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	0h	NA	Reserved
15:8	RW/S	FFh*	USB	Next Capability Pointer See Note below
7:0	RW/S	C5h	USB	Capability ID

*Note: The next capability pointer is 00h if EPPortLock = False

Table 369. SSIC Port N Register Access Control

Address Offset:04h – 07h,
Port 1 ... N : 04h, 114h, 224h
Port N = 04h + (NumSSIClanes-1)* 110h

Upto a maximum of 3 SSIC ports

Bit	Access	Default Value	RST/PWR	Description
31:26	RO	0h	USB	Reserved
25	RW	0b	USB	Register Bank Valid 0 = No valid Commands in the Lane N register bank. Host Controller can close the PWM burst once commands from this register are completed. 1 = Valid commands present in the Lane N register bank. Host controller must complete commands from the register bank before closing the burst.
24	RW	0b	USB	Target Phy: 0 = Remote Phy 1 = Local Phy Setting this bit to '1' allows the use of this command mechanism to write to local Phy profile and AFE tuning registers – Primarily as a back up option.
23	RW	1b	USB	HS_Config: When this bit is set to '1' the host controller will issue an RRAP write with HS_Config=1 once it sees "Command Phase Done" = 1
22	RW	1b	USB	Command Phase Done When set to '1', this indicates that SW has completed performing RRAP cycles through the command register. SW can set this bit initially to indicate auto mode for Local and Remote MIPI MPHY registers. For Remote MIPI MPHY auto mode SW should ensure that CONFIG_FOR_HS is executed via HS_Config or through command.
21	RW	0b	USB	Command Valid: When written to '1' indicates that the Attribute ID and Attribute Data (for writes) fields are valid. This is set by SW and cleared by HW once command operation is done. SW should only program the next read/ write operation after that.
20	RW	0b	USB	Read_Write 0 = Write 1= Read
19:8	RW	000h	USB	Attribute ID Attribute ID that is being written or read
7:0	RW	00h	USB	Attribute Write Data Data byte that is required to be written to either the local phy or the remote phy

Table 370. SSIC Port N Register Access Status

Address Offset: 08h-0Bh
Port 1 ... N : 08h, 118h, 228h
Port N = 08h + (NumSSIClanes-1)* 110h
Upto a maximum of 3 SSIC Ports

Bit	Access	Default Value	RST/PWR	Description
31:10	RO	0h	USB	Reserved
9:8	RW	0b	USB	Command Completion Status 00 = Command not complete 01 = Command complete with Success 10 = Command complete with Error These bits must be cleared before a new command is initiated.
7:0	RO	00h	USB	Read Data Data read as a result of the RRAP operation

Table 371. Profile Attributes: Port 1 ... N

Address Offsets:0Ch – 0Fh, upto 108h – 10Bh (for Port 1)
Default Value:00h
Access: RW;
Size:32 bits
64 Dwords per Port, upto a max. of 3 Ports.

Port 1: 0Ch,10h,...,108h

Port 2: 11Ch, 120h, … , 218h

Port 3: 22Ch, 230h, … , 328h

Repeat for NumSSIClanes ports,
Port N = 0Ch + (N-1)* 110h to 108h+(N-1)*110h
(where N = NumSSIClanes)

This bank of registers provides 64 Dwords per port to be used to store attributes that need to be written into the local and remote phy every time the link enters the PWM state.

Bit	Access	Default Value	RST/PWR	Description
31:28	RO	0h	USB	Reserved
27:16	RW	00h	USB	Attribute ID {Upper Address [3:0], Lower Address [7:0]}
15	RW	0b	USB	Valid When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	RW	0b	USB	Target Phy 0 = Remote Phy 1 = Local Phy
13:8	RO	0h	USB	Reserved
7:0	RW	0h	USB	Attribute Value

Table 372. Reserved Addresses: Ports 1 ... N

Address Offsets:10Ch – 113Fh, upto 32Ch – 333h
Default Value:00h
Access: RO;
Size:32 bits
2 Dwords per Port,
Port 1: 10Ch, 110h
Port 2: 21Ch, 220h
Port 3: 32Ch, 330h
Repeat for NumSSIClanes
Port N = 10Ch + (N-1)* 110h to 110h+(N-1)*110h
Where N = 1 to 3
Upto a max. of 3 ports

These two DWORDs are left reserved per Port.

4.7.4.12 USB3.1 Policies

Base Offset = 8E58h

Table 373. USB3p1 Policies Capability Register

Address Offset: 00h - 03h
Default Value:00h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:16	RO	0h	NA	Reserved
15:8	RW/S	00h	USB	Next Capability Pointer
7:0	RW/S	CAh	USB	Capability ID

Table 374. HOST_CTRL_SSP_LINK_PORT_REG1

Address Offset: 04 – 07h
Default Value:00h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:25	RO	0h	USB	Rsvd2 (Rsvd2):
24	RW	0h	USB	HC OS Owned Semaphore (HCOSOS):

Table 375. HOST_CTRL_SSP_LINK_PORT_REG2

Address Offset: 08 – 0Bh
Default Value:00h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
[31:USB3_PORTS]			PGD	RESERVED
[SSP-PORTS-1:0]	RW	0	PGD	SSP_LPBK_REPEATER: This will set the local loopback in repeater bit (Bit 4) set in Symbol 5 of TS1/TS2. (Bit2 and Bit3 will be controlled by HOST_CTRL_PORT_LINK_REG)

Table 376. HOST_CTRL_SSP_LINK_REG1

Address Offset: 0C – 0Fh
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:17			PGD	RESERVED
16:14	RW	7	PGD	SKP_THRESHOLD 000 – SKP OS every 20 Blocks 001 – SKP OS every 30 Blocks 010 – SKP OS every 35 Blocks 011 – SKP OS every 36 Blocks 100 – SKP OS every 37 Blocks 101 – SKP OS every 38 Blocks 110 – SKP OS every 39 Blocks 111 – SKP OS every 40 Blocks (Default)
13:12	RW	01	PGD	SKP_OS_LENGTH 00 – 16 Symbol OS Block 01 – 24 Symbol OS Block (Default) 10 – 32 Symbol OS Block
11	RW	1	PGD	DIS_PTM_GEN1 0 – Enable PTM as per specification. 1 – Disable PTM (Do not generate LDM LMP)
10	RW	0	PGD	DIS_PTM_GEN2 0 – Enable PTM as per specification. 1 – Disable PTM (Do not generate LDM LMP)
9	RW	0	PGD	SYNC_POLICY_FOR_TS 0 – 1st SYNC will be sent out after 16384 TSEQ or 32 TS1/TS2. (Default) 1 – 1st SYNC will be set out at start of POLLING or RECOVERY. (Simulation)
8	RW	0	PGD	DC_BAL_POLICY 0 – Spec defined Section 6.4.1.2.2 1 – Treat DC Balance of > 15 same as > 31
7	RW	0	PGD	DIS_DC_BALANCE 0 – DC Balance is Enabled 1 – DC Balance is Disabled
6	RW	1	PGD	TS1_TS2_IS_COUNT 0 – 16 TS1/TS2/IS are transmitted (Default) 1 – 32 TS1/TS2/IS are transmitted This is valid for Polling, Recovery and Hot Reset.
5:4	RW	2	PGD	TSEQ_OS_COUNT 0 – 32 (For Simulation) 1 – 262143(Default) 2 – 524288 (Default) 3 – 1048576
3:2	RW	3	PGD	SYNC_FREQ 0 – 8 for TSEQ and 8 for TS1/TS2 (Simulation Mode) 1 – 4096 for TSEQ and 16 for TS1/TS2 2 – 8192 for TSEQ and 16 for TS1/TS2 3 – 16384 for TSEQ and 32 for TS1/TS2 (Default)

Bit	Access	Default Value	RST/PWR	Description
1	RW	0	PGD	DIS_SSP_SCRAMBLE_TS This will Disable the SSP scramble for TSEQ, TS1 and TS2. This is not a spec defined mode and can only be used for validation. If set scrambling will remain disabled over riding the Link Configuration in TS1 and TS2. Disabling Scrambling will not impact DC Balance. HOST_CTRL_PORT_LINK_REG[5] will control the disable scrambling configuration for Data Phase.
0	RW	0	PGD	RESERVED

Table 377. HOST_CTRL_SSP_LINK_REG2

Address Offset: 10 – 13h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:29			PGD	Reserved
28	RW	0	PGD	RXSTANDBY_TX_LFPS If set to '1', it will enable the rx receiver, while controller has started transmitted LFPS. This will only work if RXSTANDBY_UX_EXIT is set. This is not a recommended setting by the USB3 PHYs.
27	RW	1	PGD	RXSTANDBY_U3_EXIT If set to '1', it will enable rx receiver during U3 Exit when starting receiving RxElectIdle.
26	RW	1	PGD	RXSTANDBY_U2_EXIT If set to '1', it will enable rx receiver during U2 Exit when starting receiving RxElectIdle.
25	RW	1	PGD	RXSTANDBY_U1_EXIT If set to '1', it will enable rx receiver during U1 Exit when starting receiving RxElectIdle.
24:23	RW	00	PGD	RXSTANDBY_RECOV_TO Time to keep rxstandby on while entering Recovery 00 – Disabled, turn off immediately 01 – 1us-2us 10 – 4us-5us 11 – 7us-8us If set to nonzero value, RXSTANDBY_UX_EXIT should be kept 0.
22:20	RW	101	PGD	RXSTANDBY_RXEQ_TO Time to keep rxstandby on while entering RXEQ 000 – Disable, turn off immediately 001 – 1us-2us (Simulation time) 010 – 16us 011 – 32us 100 – 128us 101 – 160us 110 – 192us 111 – 256us
19:18	RW	00	PGD	RXSTANDBY_POLICY Force RXSTANDBY to ON or OFF 00 – Default (set / clear by LTSSM operation) 01 – Always Set 10 – Always Clear 11 – Illegal
17:0	RW	00000h	PGD	SSP_TXDEEMPH

Table 378. HOST_CTRL_LDM_DELAY_REG

Address Offset: 13 – 17h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:24	RW	00h	PGD	LDM_Datapath_SS_TX_Delay This is value in tIsochTimestampGranularity (16.667ns) units the delay between initiating the LDM response to the last symbol getting transmitted on the wire Calculating the Response Delay, this value is added to the response delay.
23:16	RW	00h	PGD	LDM_Datapath_SS_RX_Delay This is value in tIsochTimestampGranularity (16.667ns) units the delay between receiving the last symbol of LDM Request on the wire and the time that is latched internally. This value is calculated based on Path delay. Calculating the Response Delay, this value is subtracted from the actual latched time.
15:8	RW	00h	PGD	LDM_Datapath_SSP_TX_Delay This is value in tIsochTimestampGranularity (16.667ns) units the delay between initiating the LDM response to the last symbol getting transmitted on the wire Calculating the Response Delay, this value is added to the response delay.
7:0	RW	00h	PGD	LDM_Datapath_SSP_RX_Delay This is value in tIsochTimestampGranularity (16.667ns) units the delay between receiving the last symbol of LDM Request on the wire and the time that is latched internally. This value is calculated based on Path delay. Calculating the Response Delay, this value is subtracted from the actual latched time.

Table 379. HOST_CTRL_SSP_LFPS_REG1

Address Offset: 18 – 1Bh
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:29			PGD	Reserved
28:23	RW	31d	PGD	TXLFPS_SCD_END_TREP Repeat time between two LFPS Bursts for SDC END. For normal mode of operation this will be multiple of 1us. For speedup mode, it will be multiple of 64ns starting from 384ns. 0: 1us / 256ns .... 31: 32us / 2240ns .... 63: 64us / 4480ns
22:18	RW	11d	PGD	TXLFPS_SCD1_TREP Repeat time between two LFPS Bursts for SDC1. For normal mode of operation this will be multiple of 1us. For speedup mode, it will be multiple of 64ns starting from 832ns. 0: 1us / 256ns .... 9: 10us / 832ns .... 31: 32us / 2240ns

Bit	Access	Default Value	RST/PWR	Description
17:13	RW	6d	PGD	TXLFPS_SCD0_TREP Repeat time between two LFPS Bursts for SDC0. For normal mode of operation this will be multiple of 1us. For speedup mode, it will be multiple of 64ns starting from 384ns. 0: 1us / 256ns .... 9: 10us / 832ns .... 31: 32us / 2240ns
12:10	RW	2d	PGD	TXLFPS_PING_TBURST Burst duration for Ping LFPS in order of 32ns. 0: 32ns ... 2: 96ns (Default) .. 7: 256ns Speedup: 32ns
9:5	RW	9d	PGD	TXLFPS_TREP Repeat time between two LFPS Bursts during POLLING. For normal mode of operation this will be multiple of 1us. For speedup mode, it will be multiple of 64ns starting from 256ns. 0: 1us / 256ns .... 9: 10us / 832ns .... 31: 32us / 2240ns
4:0	RW	8d	PGD	TXLFPS_TBURST Duration for which one LFPS burst will be transmitted during POLLING. For normal mode of operation this will be multiple of 128ns. For speedup mode, it will be multiple of 32ns. 0: Illegal 1: 128ns/32ns .... 8: 1.024us/256ns 31: 3.968us/992ns

Table 380. HOST_CTRL_SSP_LFPS_REG2

Address Offset: 1C – 1Fh
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:28	RW	5d	PGD	TXLFPS_PING_TREP Repeat time for Ping LFPS. 0: 32ms / 8us 1: 64ms / 16us ..... 5: 192ms / 48us(Default) ..... 15: 512ms / 128us

Bit	Access	Default Value	RST/PWR	Description
27:23	RW	13d	PGD	RXLFPS_TREP_MAX Max duration for detection of Polling LFPS Repeat between bursts. For normal mode of operation this will be multiple of 1us. For speedup mode, it will be multiple of 128ns. 0: 1us / 256ns .... 13: 14us / 1088ns (Default) 31: 32us / 2240ns
22:18	RW	4d	PGD	RXLFPS_TBURST_MIN Min duration for detection of Polling LFPS. For normal mode of operation this will be multiple of 128ns. For speedup mode, it will be multiple of 32ns. 0: 0.128us / 32ns .... 4: 0.640us / 160ns (Default) .... 31: 4.096us / 1024ns
17:13	RW	10d	PGD	RXLFPS_TBURST_MAX Max duration for detection of Polling LFPS. For normal mode of operation this will be multiple of 128ns. For speedup mode, it will be multiple of 32ns. 0: 128ns / 32ns .... 10: 1.408us / 352ns (Default) .... 31: 4.096us / 1024ns
12:9	RW	11d	PGD	TXLFPS_TLBPS1 LFPS Burst time for transmitting 1 for LBPS. For normal mode of operation this will be multiple of 128ns. For speedup mode, it will be multiple of 32ns. 0: 128ns / 32ns .... 11: 1.536us/384ns (Default) 15: 2.048us/512ns
8:5	RW	4d	PGD	TXLFPS_TLBPS0 LFPS Burst time for transmitting 0 for LBPS. For normal mode of operation this will be multiple of 128ns. For speedup mode, it will be multiple of 32ns. 0: 128ns / 32ns .... 4: 640ns / 160ns (Default) .... 15: 2.048us / 512ns
4:0	RW	16d	PGD	TXLFPS_TPWM Transmit PWM Period. For normal mode of operation this will be multiple of 128ns. For speedup mode, it will be multiple of 32ns. 0: 128ns / 32ns .... 16: 2.176us / 544ns (Default) .... 31: 4.096us / 1024ns

Table 381. HOST_CTRL_SSP_LFPS_REG3

Address Offset: 20 – 23h
Access: RW;

Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31			PGD	Reserved
30:27	RW	9d	PGD	RXLFPS_TLBPS1_MIN Min LFPS Burst time for detecting 1 for LBPS. For normal mode of operation this will be multiple of 128ns. For speedup mode, it will be multiple of 32ns. 0: 0.128us / 32ns .... 9: 1.280us / 320ns (Default) .... 15: 2.048us / 512ns
26:23	RW	14d	PGD	RXLFPS_TLBPS1_MAX Max LFPS Burst time for detecting 1 for LBPS. For normal mode of operation this will be multiple of 128ns. For speedup mode, it will be multiple of 32ns. 0: 0.128us / 32ns ..... 15: 2.048us / 512ns
22:19	RW	2d	PGD	RXLFPS_TLBPS0_MIN Min LFPS Burst time for detecting 0 for LBPS. For normal mode of operation this will be multiple of 128ns. For speedup mode, it will be multiple of 32ns. 0: 0.128us / 32ns .... 2: 0.384us / 96ns (Default) .... 15: 2.048us / 512ns
18:15	RW	6d	PGD	RXLFPS_TLBPS0_MAX Max LFPS Burst time for detecting 0 for LBPS. For normal mode of operation this will be multiple of 128ns. For speedup mode, it will be multiple of 32ns. 0: 0.128us / 32ns .... 6: 0.896us / 224ns (Default) .... 15: 2.048us / 512ns
14:10	RW	10d	PGD	RXLFPS_TGAP_SCD1_MIN Min duration for detection of Polling LFPS Gap between bursts to identify SCD Logic 1. For normal mode of operation this will be multiple of 1us. For speedup mode, it will be multiple of 64ns. 0: 1us / 256ns .... 10: 11us / 896ns (Default) .... 31: 32us / 2240us
9:5	RW	8d	PGD	RXLFPS_TGAP_SCD0_MAX Max duration for detection of Polling LFPS Gap between bursts to identify SCD Logic 0. For normal mode of operation this will be multiple of 1us. For speedup mode, it will be multiple of 64ns. 0: 1us / 256ns .... 8: 9us / 768ns (Default) .... 31: 32us / 4288ns

Bit	Access	Default Value	RST/PWR	Description
4:0	RW	5d	PGD	RXLFPS_TREP_MIN Min duration for detection of Polling LFPS Repeat between bursts. For normal mode of operation this will be multiple of 1us. For speedup mode, it will be multiple of 64ns. 0: 1us / 256ns …. 5: 6us / 576ns (Default) …. 31: 32us / 4288ns

Table 382. HOST_CTRL_SSP_LFPS_REG4

Address Offset: 24 – 27h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:24			PGD	Reserved
23:17	RW	60d	PGD	SCD_LFPS_TIMEOUT This corresponds to the tPollingSCDLFPSTimeout as defined in the USB3.1 Spec. For normal mode, this is multiple of 1us and for fast sim, it is multiple of 32ns. If set to '0', this timeout is disabled and LTSSM will move to RXEQ when other conditions are met.
16:14	RW	2d	PGD	SCD_TX_COUNT Number of SCD TX COUNT before moving to next state.
13:11	RW	4d	PGD	LBPM_TX_COUNT Number of LBPM TX COUNT before moving to next state.
10:5	RW	16d	PGD	RXLFPS_GEN2_BAILOUT_CNT Number of LFPS Burst after which LFPS FSM will stop looking for Gen2. 0 – Disabled, Keep looking for Gen2 forever.
4:0	RW	18d	PGD	RXLFPS_TDELIM_MAX Max PWM Period for detecting a delimiter. For normal mode of operation this will be multiple of 128ns. For speedup mode, it will be multiple of 32ns. 0: 0.128us / 32ns …. 18: 2.432us / 608ns (Default) …. 31: 4.096us / 1024ns

Table 383. HOST_CTRL_SSP_CONFIG_REG1

Address Offset: 28 – 2Bh
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
Bit	Access	Default Value	RST/PWR	Description
31:0	RW	0	PGD	Reserved

Table 384. HOST_CTRL_USB3_ERR_COUNT

Address Offset: 2C – 2Fh
Port 1 …. N: 2Ch,30h,….(2Ch + (USB3_NPORT-1)*4h)
Access: RW;
Size:32 bits

Upto a maximum of 16 USB3 Ports

Bit	Access	Default Value	RST/PWR	Description
31:16		0	PGD	Reserved
15:0	RW	0	PGD	USB3_SOFT_ERR_CNT This register will keep count of soft errors on SS and SSP ports for a particular port. This register is read/write by software and it can be cleared by software by writing to it. Once reached to maximum value, it will stop incrementing.

Table 385. HOST_CTRL_USB3_DEBUG_REG1

Address Offset: 80 – 83h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
[31:USB3_PORTS]			PGD	RESERVED
[USB3_PORTS-1:0]	RW	0	PGD	DEBUG_PORT_SEL One hot bit to enable a port for which Software / BIOS would update the HOST_CTRL_USB3_DEBUG_REG2 and HOST_CTRL_USB3_DEBUG_REG3. Once cleared for a port, port will consider BP and forces for that port anymore.

Table 386. HOST_CTRL_USB3_DEBUG_REG2

Address Offset: 84 – 87h
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31			PGD	Reserved
30:25	RW	0	PGD	BP_RHUB_VAL
24:20	RW	0	PGD	BP_LFPS_CTRL_VAL
19:13	RW	0	PGD	BP_AUXPM_VAL
12:8	RW	0	PGD	BP_LTSSM_VAL
7	RW	0	PGD	BP_RHUB This bit is set by software / BIOS along with BP_RHUB_VAL and cleared by hardware when BP is hit.
6	RW	0	PGD	BP_LFPS_CTRL This bit is set by software / BIOS along with BP_LFPS_CTRL_VAL and cleared by hardware when BP is hit.
5	RW	0	PGD	BP_AUXPM This bit is set by software / BIOS along with BP_AUXPM_VAL and cleared by hardware when BP is hit.
4	RW	0	PGD	BP_LTSSM This bit is set by software / BIOS along with BP_LTSSM_VAL and cleared by hardware when BP is hit.
3	RW	0	PGD	NEXT_COMP_PATTERN Set by software to switch to next compliance pattern instead of waiting for the Ping.LFPS. This is self-clearing bit set by software and cleared by hardware when switching is complete.
2:1	RW	00	PGD	FORCE_RATE Once set, this will update the rate and pclkrate signals without rate change handshake through PIPE signals. 00 – Disabled 01 – Force Gen1 Rate 10 – Force Gen2 Rate 11 – N/A

Bit	Access	Default Value	RST/PWR	Description
0	RW	0	PGD	POLLING_TIMEOUT_DIS If set to '1', it disables various LTSSM timeouts during Polling states: - tPollingLFPSTimeout - tPollingSCDLFPSTimeout - tPollingLBPMLFPSTimeout - tPollingActiveTimeout - tPollingConfigurationTimeout - tPollingIdleTimeout

Table 387. HOST_CTRL_USB3_DEBUG_REG3

Address Offset: 88 – 8Bh
Access: RW;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31			PGD	Reserved
30	RW	0	PGD	WAIT_RHUB Set and clear by software / BIOS to keep the state machine in the state once BP is hit.
29	RW	0	PGD	WAIT_LFPS_CTRL Set and clear by software / BIOS to keep the state machine in the state once BP is hit.
28	RW	0	PGD	WAIT_AUXPM Set and clear by software / BIOS to keep the state machine in the state once BP is hit.
27	RW	0	PGD	WAIT_LTTSM Set and clear by software / BIOS to keep the state machine in the state once BP is hit.
26:21	RW	0	PGD	FORCE_RHUB_VAL
20:16	RW	0	PGD	FORCE_LFPS_CTRL_VAL
15:9	RW	0	PGD	FORCE_AUXPM_VAL
8:4	RW	0	PGD	FORCE_LTSSM_VAL
3	RW	0	PGD	FORCE_RHUB This bit is set by software / BIOS along with FORCE_RHUB_VAL and cleared by hardware when transitions into new state
2	RW	0	PGD	FORCE_LFPS_CTRL This bit is set by software / BIOS along with FORCE_LFPS_CTRL_VAL and cleared by hardware when transitions into new state
1	RW	0	PGD	FORCE_AUXPM This bit is set by software / BIOS along with FORCE_AUXPM_VAL and cleared by hardware when transitions into new state
0	RW	0	PGD	FORCE_LTSSM This bit is set by software / BIOS along with FORCE_LTSSM_VAL and cleared by hardware when transitions into new state

4.7.5 Host Controller Private Configuration Space

The private configuration space is a register space that lies outside the PCI configuration or Host MMIO address spaces. It is a HW private address space that is accessible only via the IOSF-SB channel.

Table 388. EXI Base Address Low (0Ch)

Address Offsets:0Ch – 0Fh
Default Value: 0h
Access: RO;

Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:0	RO	0h	NA	This is the base address in the host address space of the DbC registers that support the EXI function. This register provides the lower 32b of the address. The address is hardcoded and is exposed in this register to enable BIOS to appropriately set this block of memory aside.

Table 389. EXI Base Address High (10h)

Address Offsets:10h – 14h
Default Value: 0h
Access: RO;
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:0	RO	0h	NA	This is the base address in the host address space of the DbC registers that support the EXI function. This register provides the upper 32b of the address. The address is hardcoded and is exposed in this register to enable BIOS to appropriately set this block of memory aside.

Table 390. Private - EP Type Lock Policy 1 (14h)

Address Offsets:14h – 17h
Default Value:00h
Access: RW/L; (this register can be written until the access control is set)
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:8	RO	0h	NA	Reserved
7	RW/L	0	USB	Interrupt IN EP Type: 0 – Interrupt IN EP is allowed 1 – Interrupt IN EP is not allowed
6	RW/L	0	USB	Bulk IN EP Type 0 – Bulk IN EP is allowed 1 – Bulk IN EP is not allowed
5	RW/L	0	USB	Isochronous IN EP Type 0 – Isoch IN EP is allowed 1 – Isoch IN EP is not allowed
4	RW/L	0	USB	Control EP Type 0 – Control EP is allowed 1 – Control IN EP is not allowed
3	RW/L	0	USB	Interrupt OUT EP Type 0 – Interrupt OUT EP is allowed 1 – Interrupt OUT EP is not allowed
2	RW/L	0	USB	Bulk OUT EP Type 0 – Bulk OUT EP is allowed 1 – Bulk OUT EP is not allowed
1	RW/L	0	USB	Isochronous OUT EP Type 0 – Isoch OUT EP is allowed 1 – Isoch OUT EP is not allowed
0	RW/L	0	USB	Policy 1 Enable When set, enables Policy #1 to be globally enabled.

Table 391. Private - EP Type Lock Policy 3 (1Ch)

Address Offsets:1Ch – 1Fh
Default Value:00h
Access: RW/L; (this register can be written until the access control is set)
Size:32 bits

Bit	Access	Default Value	RST/PWR	Description
31:8	RO	0h	NA	Reserved

Bit	Access	Default Value	RST/PWR	Description
7	RW/L	0	USB	Interrupt IN EP Type: 0 – Interrupt IN EP is allowed 1 – Interrupt IN EP is not allowed
6	RW/L	0	USB	Bulk IN EP Type 0 – Bulk IN EP is allowed 1 – Bulk IN EP is not allowed
5	RW/L	0	USB	Isochronous IN EP Type 0 – Isoch IN EP is allowed 1 – Isoch IN EP is not allowed
4	RW/L	0	USB	Control EP Type 0 – Control EP is allowed 1 – Control IN EP is not allowed
3	RW/L	0	USB	Interrupt OUT EP Type 0 – Interrupt OUT EP is allowed 1 – Interrupt OUT EP is not allowed
2	RW/L	0	USB	Bulk OUT EP Type 0 – Bulk OUT EP is allowed 1 – Bulk OUT EP is not allowed
1	RW/L	0	USB	Isochronous OUT EP Type 0 – Isoch OUT EP is allowed 1 – Isoch OUT EP is not allowed
0	RW/L	0	USB	Policy 3 Enable When set, enables Policy #1 to be globally enabled.

Table 392. Private - Port Lock Control – Port 1 … N (20…upto 11Ch)

Address Offsets:10h, 14h, … extend to Maxports count.
Default Value:00h
Access: RW/L; (this register can be written until the access control is set)
Size:32 bits
Repeat Maxports times
Addresses:

Port 1 = 20h,

Port 2 = 24h,

Port 3 = 28h …

Port (Maxports) = 20+(Maxports – 1) * 4

Maxports is no more than 64

Bit	Access	Default Value	RST/PWR	Description
31:8	RO	0h	NA	Reserved
7	RW/L	0	USB	Enable USB Lock Policy on root port number N: 00h – Port lock not enabled on port N 01h – Policy 1 enabled on port N 02h – Policy 2 enabled on port N 03h – policy 3 enabled on port N 4h to FFh - Reserved

4.7.6 DbC Private Memory Mapped Address Space Registers

The DbC interfaces that support the EXI transport function use addresses in the Host Address space that are set hard coded and set aside for it by BIOS. This address range does not fall within the MEMBAR of the XHCI host controller and is not affected by the value of the MSE in the XHCI functions PCI config space.

4.7.6.1 Base Address (DbCPrivateMemBase)

The base address for the DbC private memory mapped space is hard coded as an integration parameter.

Table 393. DbC GP2 OUT Payload Pointer (low)

Address Offset: 00h

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	USB	Lower DW of payload address pointer

Table 394. DbC GP2 OUT Payload Pointer (high)

Address Offset: 04h

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	USB	Upper DW of payload address pointer

Table 395. DbC GP2 OUT Payload Qualifiers

Address Offset: 08h

Bit	Access	Default Value	RST/PWR	Description
31:16	RW	00h	USB	Reserved
15:8	RW	00h	USB	Destination ID
7:4	RO	0h	USB	Reserved
3:0	RW	0h	USB	Root Space

Table 396. DbC GP2 OUT Payload Transfer Length

Address Offset: 0Ch

Bit	Access	Default Value	RST/PWR	Description
31	RW	0b	USB	Data Valid This bit indicates the presence of a valid data buffer and is the “doorbell” that allows the DbC to initiate a DMA transaction. This bit is cleared by HW upon completion of the DMA upto either the specific transfer length, or the host controller sending a short packet.
30:00	RW	00h	USB	Payload Transfer Length Length of the payload buffer in bytes. This is a ‘1’ based count.

Table 397. DbC GP2 OUT Status Pointer (low)

Address Offset: 10h

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	USB	Lower DW of Status address pointer

Table 398. DbC GP2 OUT Status Pointer (high)

Address Offset: 14h

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	USB	Upper DW of Status address pointer

Table 399. DbC GP2 OUT Status Qualifiers

Address Offset: 18h

Bit	Access	Default Value	RST/PWR	Description
31:16	RW	00h	USB	Reserved
15:8	RW	00h	USB	Destination ID
7:4	RO	0h	USB	Reserved
3:0	RW	0h	USB	Root Space

Table 400. DbC GP2 IN Payload Pointer (low)

Address Offset: 1Ch

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	USB	Lower DW of payload address pointer

Table 401. DbC GP2 IN Payload Pointer (high)

Address Offset: 20h

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	USB	Upper DW of payload address pointer

Table 402. DbC GP2 IN Payload Qualifiers

Address Offset: 24h

Bit	Access	Default Value	RST/PWR	Description
31:16	RW	00h	USB	Reserved
15:8	RW	00h	USB	Destination ID
7:4	RO	0h	USB	Reserved
3:0	RW	0h	USB	Root Space

Table 403. DbC GP2 IN Payload Transfer Length

Address Offset: 28h

Bit	Access	Default Value	RST/PWR	Description
31	RW	0b	USB	Data Valid This bit indicates the presence of a valid data buffer and is the “doorbell” that allows the DbC to initiate a DMA transaction. This bit is cleared by HW upon completion of the DMA upto the specific transfer length.
30:00	RW	00h	USB	Payload Transfer Length Length of the payload buffer in bytes. This is a ‘1’ based count.

Table 404. DbC GP2 IN Status Pointer (low)

Address Offset: 2Ch

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	USB	Lower DW of Status address pointer

Table 405. DbC GP2 IN Status Pointer (high)

Address Offset: 30h

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	USB	Upper DW of Status address pointer

Table 406. DbC GP2 IN Status Address Qualifiers

Address Offset: 34h

Bit	Access	Default Value	RST/PWR	Description
31:16	RW	00h	USB	Reserved
15:8	RW	00h	USB	Destination ID
7:4	RO	0h	USB	Reserved
3:0	RW	0h	USB	Root Space

Table 407. DbC DFX OUT Control

Address Offset: 38h

Bit	Access	Default Value	RST/PWR	Description
31:04	RO	00h	USB	Reserved
3:0	RW	00h	USB	Available Credits THe EXI Bridge writes the absolute value of the available credit count into this register field each time it drains an entry from its buffers. Each credit represents a 64 byte EXI packet.

Table 408. DbC DFX IN Payload Pointer (low)

Address Offset: 3Ch

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	USB	Lower DW of payload address pointer

Table 409. DbC DFX IN Payload Pointer (high)

Address Offset: 40h

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	USB	Upper DW of payload address pointer

Note: Qualifiers are not needed for the DFX IN interface, since the qualifiers will be identical to those used for the DFx OUT interface, which are hardcoded.

Table 410. DbC DFX IN Payload Transfer Length

Address Offset: 44h

Bit	Access	Default Value	RST/PWR	Description
31	RW	0b	USB	Data Valid This bit indicates the presence of a valid data buffer and is the "doorbell" that allows the DbC to initiate a DMA transaction. This bit is cleared by HW upon completion of the DMA upto the specific transfer length.
30:00	RW	00h	USB	Payload Transfer Length Length of the payload buffer in bytes. This is a '1' based count.

Table 411. DbC DFX IN Status Pointer (low)

Address Offset: 48h

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	USB	Lower DW of Status address pointer

Table 412. DbC DFX IN Status Pointer (high)

Address Offset: 4Ch

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	USB	Upper DW of Status address pointer

Table 413. DbC TRACE IN Payload Base Pointer (low)

Address Offset: 50h

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	USB	Lower DW of payload base pointer

Table 414. DbC TRACE IN Payload Base Pointer (high)

Address Offset: 54h

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	USB	Upper DW of payload base pointer

Table 415. DbC TRACE IN Payload Qualifiers

Address Offset: 58h

Bit	Access	Default Value	RST/PWR	Description
31:16	RW	00h	USB	Reserved
15:8	RW	00h	USB	Destination ID
7:4	RO	0h	USB	Reserved
3:0	RW	0h	USB	Root Space

Table 416. DbC TRACE IN Transfer Doorbell

Address Offset: 5Ch

Bit	Access	Default Value	RST/PWR	Description
31:19	RW	00h	USB	Reserved
18:11	RW	00h	USB	Payload Offset The Offset in multiples of 1024B from the base pointer – from which to transfer the payload referenced by this doorbell.
10:0	RW	00h	USB	Length of Transfer Payload The Trace Handler writes the length of the payload in the "entry" referenced by this doorbell.The length has an allowed maximum of 1024B

Table 417. DbC TRACE IN Status Pointer (low)

Address Offset: 60h

Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	USB	Lower DW of Status address pointer

Table 418. DbC TRACE IN Status Pointer (high)

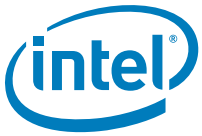
Address Offset: 64h

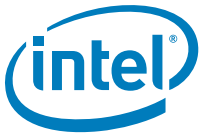
Bit	Access	Default Value	RST/PWR	Description
31:0	RW	00h	USB	Upper DW of Status address pointer

Table 419. DbC TRACE IN Status Address Qualifiers

Address Offset: 68h

Bit	Access	Default Value	RST/PWR	Description
31:16	RW	00h	USB	Reserved
15:8	RW	00h	USB	Destination ID
7:4	RO	0h	USB	Reserved
3:0	RW	0h	USB	Root Space





5.0 Electrical Specifications

5.1 Introduction

This chapter describes Alpine-Ridge DP DC and AC (timing) electrical characteristics. This includes absolute maximum rating, recommended operating conditions, power sequencing requirements, DC and AC timing specifications and TBT test electrical specification. The DC and AC characteristics include generic digital 3.3V IO specification, as well as other specifications supported by Alpine-Ridge DP.

5.2 Operating Conditions

5.2.1 Recommended Operating Conditions

See Table 420:

Table 420. Recommended Operating Conditions

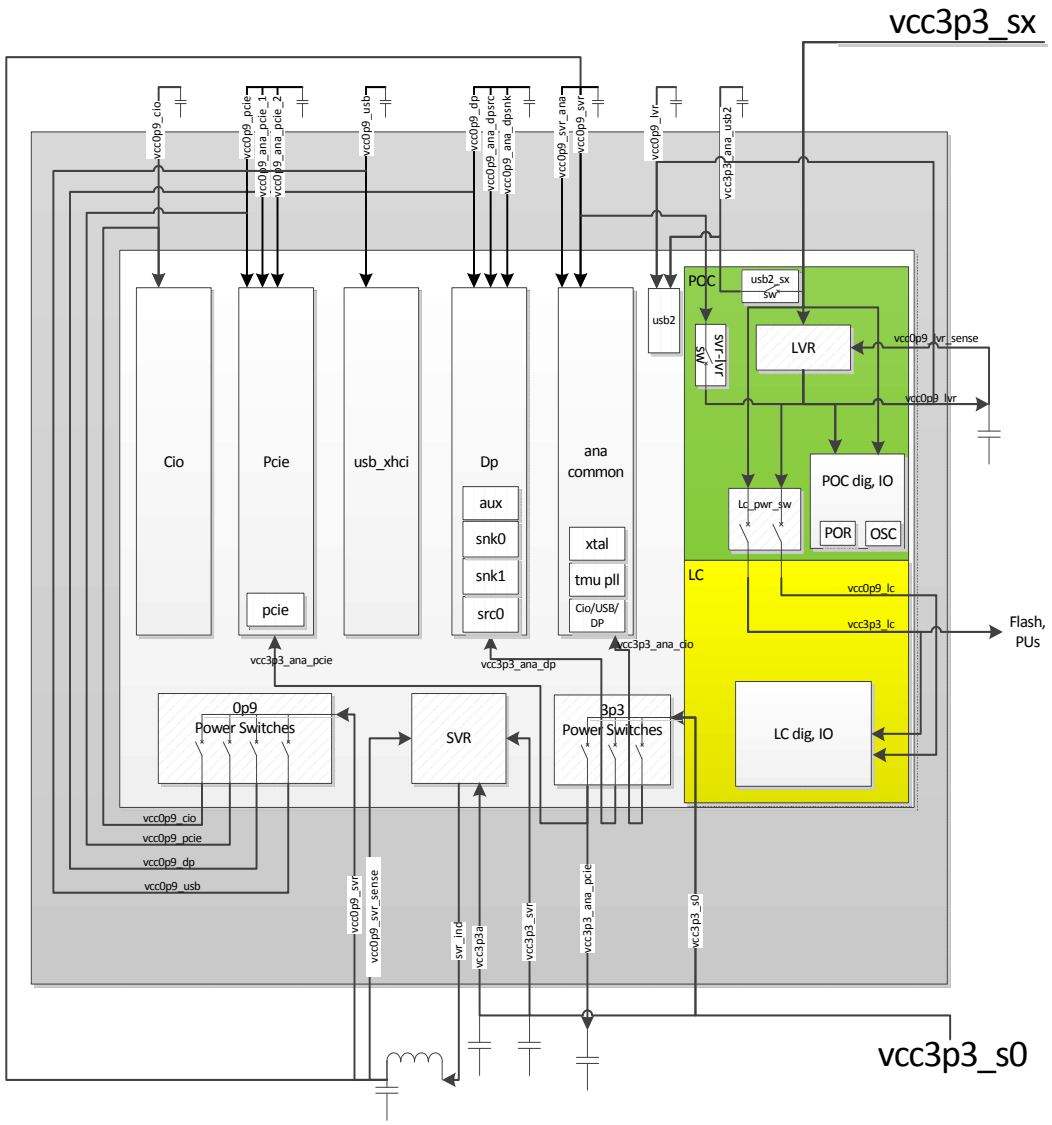
Symbol	Parameter	Min.	Typ.	Max.	Units
Ta	Operation Temperature Rang Commercial (Ambient; 0 CFS airflow)	0		65	°C
Tj	Junction Temperature			110	°C

5.3 Power Delivery

5.3.1 Power Delivery Introduction

Alpine-Ridge DP has two sources of 3.3v power supplies, which supply the power to the Alpine-Ridge DP seven power domains that are regulated and controlled within Alpine-Ridge DP. Alpine-Ridge DP controls its own power, based on the connectivity and system state/indications.

Figure 72. Alpine-Ridge DP Power Delivery



5.3.2 Power Supply specification

5.3.2.1 Power On Sequence

Figure 73. Power On Sequence

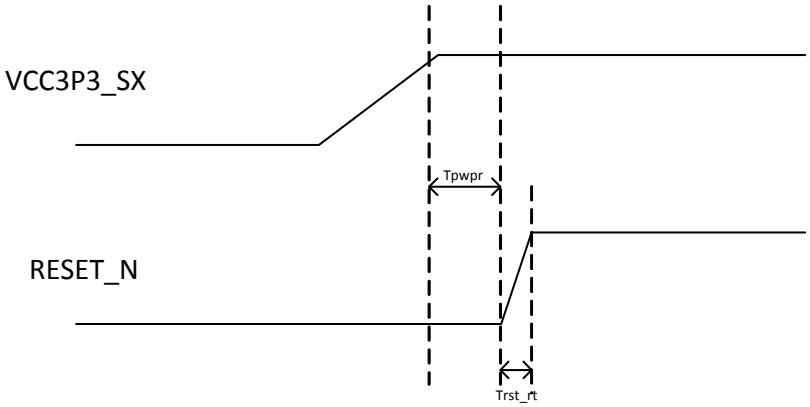


Table 421. Power On Sequence

Parameter	Description	Min	Max	Units	Comments
Tpwpr	From VCC3P3_SX at 90% to RESET_N de-assertion	100	-	us	
Trst_rt	RESET_N rise time	0.1	500	ns	

5.3.2.2 External Power Supply Specification

Table 422. External Power Supply Specification

VCC3P3 (3.3V) Parameters				
Title	**Description**	**Min.**	**Max.**	**Units**
Rise Time	Time from 10% to 90% mark	0.1	100	mS
Monotonicity	Voltage dip allowed in ramp	n/a	0	mV
Slope	Ramp rate at any given time between 10% and 90% Min: 0.8*V(min)/Rise time (max) Max: 0.8*V(max)/Rise time (min)	24	28,800	V/S
Operational Range	Operational range for VCC3P3_SX	3.07	3.465	V
	Operational range for VCC3P3_S0, VCC3P3_SVR, VCC3P3A	3.135	3.465	V

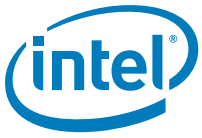


Table 422. External Power Supply Specification

VCC3P3 (3.3V) Parameters				
Title	**Description**	**Min.**	**Max.**	**Units**
Ripple	Maximum voltage ripple (peak to peak)	n/a	7	mV
Overshoot	Maximum overshoot allowed	n/a	140	mV
Overshoot Settling Time	Maximum overshoot allowed duration. (At that time delta voltage should be lower than 5mv from steady state voltage)	n/a	0.05	mS

5.3.2.3 Internal Voltage Regulator specifications

The Internal Voltage Regulator supplies Alpine Ridge core voltage (0v9). The voltage levels are internally adjusted in order to keep the unit power within target. The following voltage levels are expected on VCC0P9_SVR when active (for example, when TBT/USB/DP cables are connected):

Min[V]	Max[V]
0.87	0.99

The Voltage Regulator requires an external Inductor which should be selected according to the following specification:

- Saturation Current - Recommended L=0.6uH to 0.68uH. Inductance decreasing should be less than 10% @ (2.5A).
- Switching Frequency - Between 600KHz to 1.4MHz. Typical 1MHz.
- Inductor Losses - It is recommended to use the manufacturer calculators to calculate total losses, and not only copper losses. Also need to take into account that for some inductors, R@1MHz R_DC).

5.3.2.4 Power Consumption

Table 423. Power Consumption

Alpine-Ridge DP SKU	Mode of Operation	Chip Power	Solution Power	Units
DP/SP	Cable Disconnect / Sleep w/o Wake	-	1	mW
DP/SP	Cable Disconnect / Sleep w/ Wake	-	2	mW
DP/SP	Cable Disconnect S0 / Cable connect CS/RTD3 w/ Wake	-	3	mW

Alpine-Ridge DP SKU	Mode of Operation	Chip Power	Solution Power	Units
DP/SP	Single Re-drive	375	400	mW
DP/SP	Dual Re-drive	600	675	mW
DP/SP	1x USB2	900	975	mW
DP/SP	1x USB3.1	1000	1100	mW
DP/SP	1x TBT, x2 PCIe, DP Sink	1400	1600	mW
DP/SP	1x TBT, x4 PCIe, DP Sink-SRC	1550	1750	mW
DP/SP	1x TBT, x4 PCIe, 2x DP Sink tunnel	1700	1900	mW
DP/SP	1x TBT, x4 PCIe, DP Sink-SRC, DP Sink tunnel	1750	1950	mW
DP	2x USB2	950	1025	mW
DP	2x USB3.1	1100	1200	mW
DP	2x TBT, x4 PCIe, DP Sink-SRC	2050	2300	mW
DP	2x TBT, x4 PCIe, 2x DP Sink tunnel	2150	2400	mW
DP	2x TBT, x4 PCIe, DP Sink-SRC, DP Sink tunnel	2200	2500	mW

5.4 DC/AC Specification

5.4.1 Digital I/Os DC specifications

See Table 424 and Table 420.

Table 424. Digital I/Os DC Specification

Symbol	Parameter	Conditions	Min.	Type	Max.	Unit
VCC3P3	Periphery supply		3.135	3.3	3.465	V
VOH	Output High Voltage	IOH = -8mA; VCC3P3 = Min	2.4			V
VOL	Output Low Voltage	IOL = 8mA; VCC3P3=Min			0.4	V
VIH	Input High Voltage		2.0		3.6	V
VIL	Input Low Voltage		-0.3		0.8	V

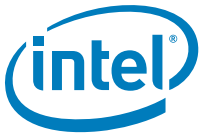


Table 424. Digital I/Os DC Specification

Symbol	Parameter	Conditions	Min.	Type	Max.	Unit
PU	Internal pullup		59	86	135	kΩ
Cin	Input Pin Capacitance				2	pF

5.4.2 XTAL/Clock Specification

See Table 425:

Table 425. XTAL/Clock Specification

Parameter Name	Symbol	Value
Nominal Frequency		25.000 MHz @ 25^0C
Vibration Mode		Fundamental
Operating/Calibration mode		Parallel
Frequency Tolerance @ 25^0 C	Δf/fo @ 25^0C	±30ppm
Temperature Tolerance	Δf/fo	±30ppm
Operating Temperature	Topr	-20˚C to 70˚C
Equivalent Series Resistor	ESR	50Ω maximum
Load Capacitance	Cload	20pF
Shunt Capacitance	Cshunt or Co	6pF maximum
Drive Level	DL	0.5mW maximum
Insulation Resistance	IR	500 M Ω minimum at DC 100V
Aging	Δf/fo	±5ppm per year maximum
External on-board Capacitors	C1,C2	20pF
Board Resistance	Rs	0.1Ω maximum

5.4.3 PCIe Electrical Specification

Alpine-Ridge DP PCIe interface supports the PCIe electrical as defined by the PCI Express Base Specification 3.0.

Note: Alpine-Ridge DP PCIe Gen3 electrical capabilities supports only the short reach and medium reach channels as defined by the PCI Express Base specification.

5.4.4 DisplayPort Electrical Specification

Alpine-Ridge DP Display interfaces supports the DisplayPort electrical as defined by the DP 1.2a Specification.

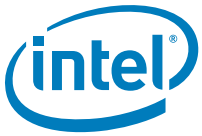
5.5 Absolute Maximum Ratings

See Table 426.

Table 426. Absolute Maximum Rating

Symbol	Parameter	Min	Max	Units
Tcase	Case temperature under bias	0	105	C
Tstorage	Storage temperature	-65	140	C
Vi/Vo	3.3 V dc Compatible I/Os Voltage	VSS–0.5	4	V
VCC3P3	3.3 V dc Periphery DC Supply Voltage	VSS–0.5	4	V

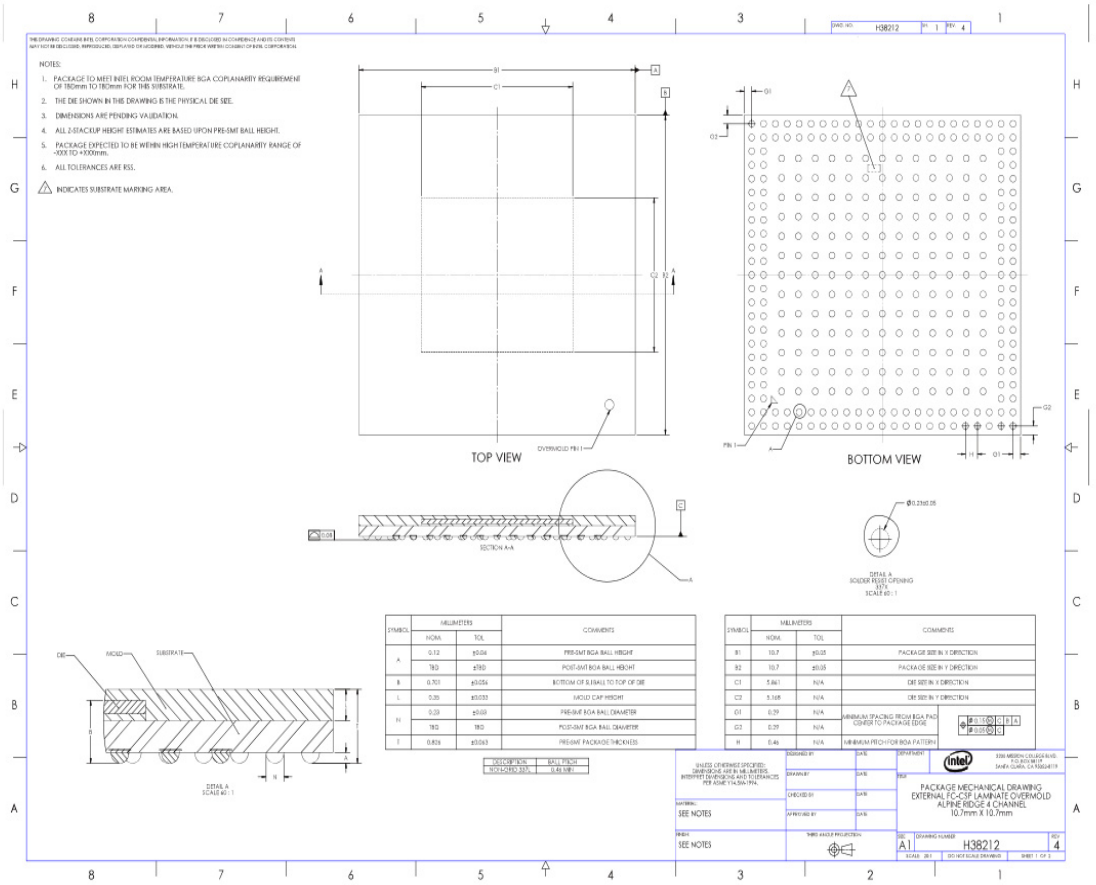
Note: Ratings in this table are those beyond which permanent device damage is likely to occur. These values should not be used as the limits for normal device operation. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



6.0 Mechanical Specification

6.1 Package Information

Figure 74. Alpine-Ridge DP package

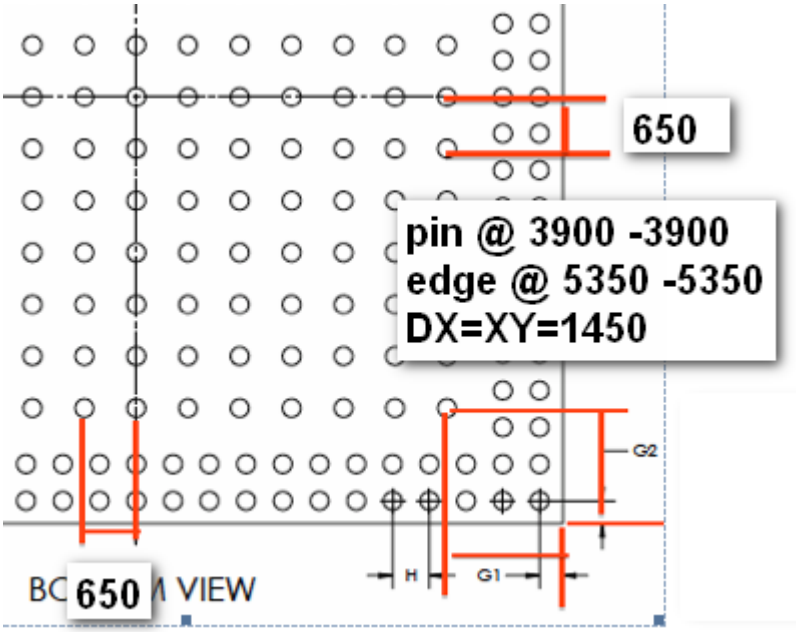


Ball-out is symmetrical In all directions. Outer pitch (X and Y) is 460u. Inner pitch (X and Y) is 650u.

UBM (for bumps) is 80u.

See Figure 75

Figure 75. Inner Pitch distances



7.0 Power Up and Wake Flows

7.1 Power Up Sequences

Figure 76 and Figure 77 illustrate the power up sequences with Alpine-Ridge DP as host.

Figure 76. Host Power up sequence

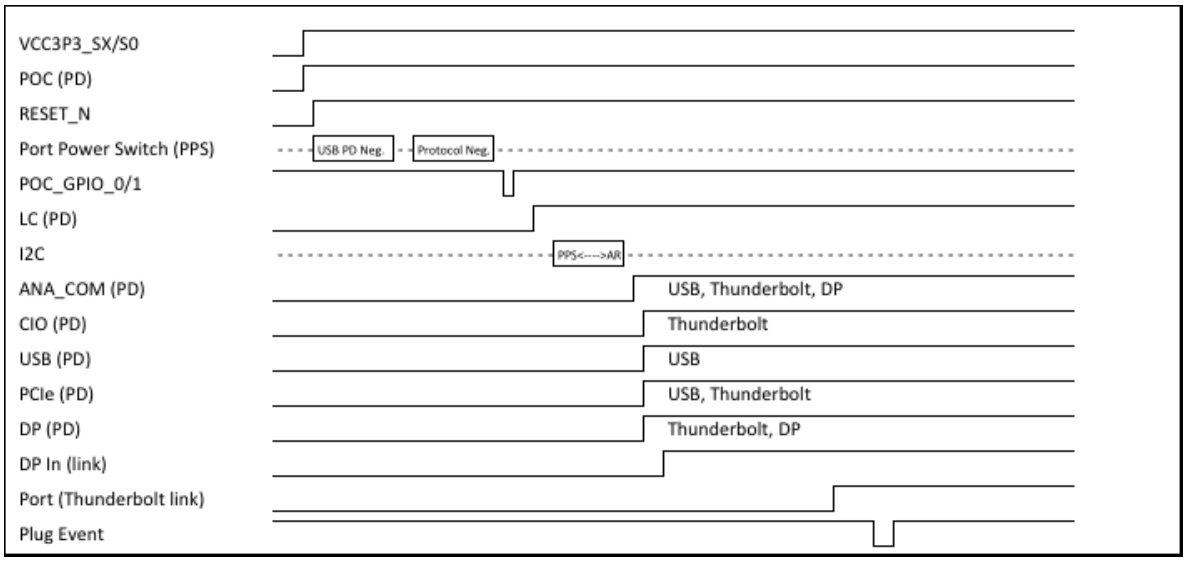
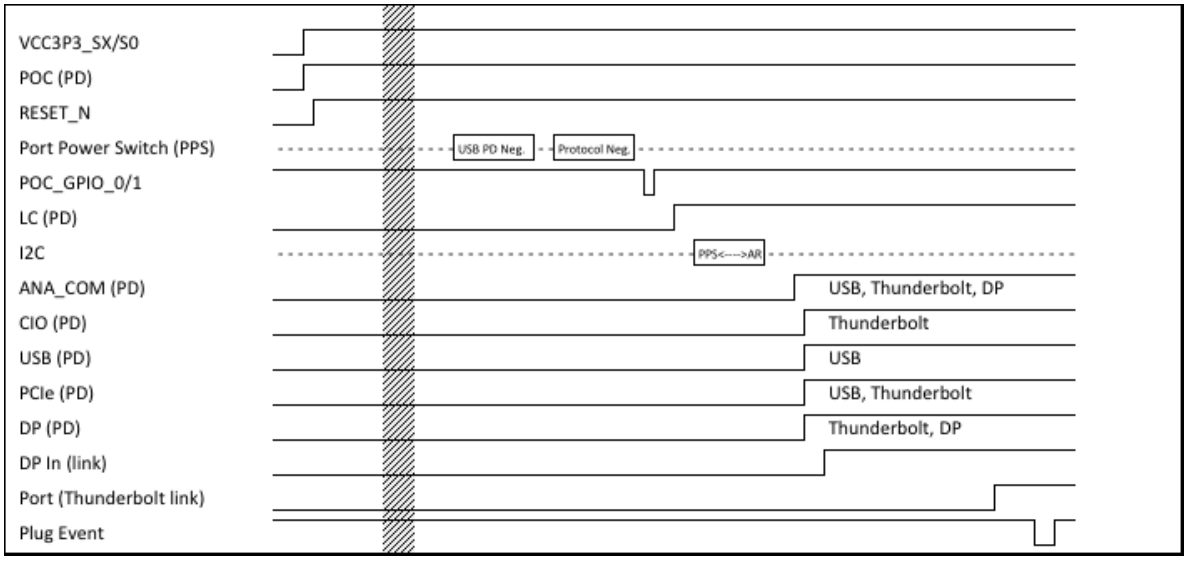


Figure 77. Host power up sequence with no Thunderbolt device connected, and later on connected



7.2 Sx Entry/Exit Flow

The following section describes the Sx entry/exit flow for Alpine-Ridge DP hosts and devices. The required interfaces are defined.

For systems that provide Alpine-Ridge DP power from two separate rails (VCC3P3_SX from a sustain rail while VCC3P3_S0 from S0 rail) the system must perform a pre-notice Sx entry procedure through the TBT2PCIe mailbox. For the case Alpine-Ridge DP is not powering the CIO domain the BIOS needs to force Alpine-Ridge DP power using POC_GPIO_3 to enable the mailbox functionality.

7.2.1 Sx Entry/Exit Flow for Alpine-Ridge DP Host with internal CM

Separate procedures apply for Sx entry with Thunderbolt wake support or no Thunderbolt wake support. A system may choose to implement both options.

7.2.1.1 Sx Entry Flow for Alpine-Ridge DP Host with Thunderbolt wake support

The Sx entry process of the Thunderbolt topology is performed automatically by the Alpine-Ridge DP Host after the system entered Sx. It does not require any BIOS intervention.

The Alpine-Ridge DP Host monitors the SLP_S3# (connected to Alpine-Ridge DP/POC_GPIO_5) and triggers the Sx entry when it is asserted.

The Internal CM configures the Thunderbolt tree for Sx, after the configurations are done, the CIO, PCIe, USB, DP, ANA_COM and LC domains are shut down.

Host providing power should retain both VCC3P3_S0 and VCC3P3_SX power rails similar to S0.

7.2.1.2 Sx Exit Flow for Alpine-Ridge DP Hosts with Thunderbolt wake support

An Alpine-Ridge DP host will wake from Sx on the following events:

- SLP_S3# deasserted
- LSRX toggle - indicating Thunderbolt wake - a wake event from a Thunderbolt device in the Thunderbolt domain.

Upon Thunderbolt wake, Alpine-Ridge DP will assert GPIO_4 until PERST_N is deasserted. GPIO_4_ will not be asserted if Alpine-Ridge DP Host woke up due to SLP_S3# deassertion.

In case of thunderbolt wake, Alpine-Ridge DP host will delay CIO, PCIe, USB, DP, ANA_COM domains power on until SLP_S3# is deasserted.

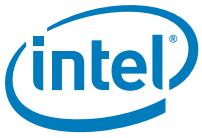
7.2.1.3 Sx Entry Flow for Alpine-Ridge DP Host when Wake is not Enabled/ Supported

When wake from Thunderbolt is not enabled/supported a system entering Sx should do the following (Connected Thunderbolt devices will shut down):

1 Assert RESET_N.

2 Completely power off Alpine-Ridge DP.

A system may wish to keep power to Alpine-Ridge DP and devices during Sx, but still not support Thunderbolt wake. In this case the system can skip the above requirements, and send a Go2Sx_No_Wake Command through the PCIE2TBT Mailbox before entering Sx.



7.2.1.4 Sx Exit flow for Alpine-Ridge DP Host when Wake is not Enabled/ Supported

When wake from Thunderbolt is not enabled/supported a system exiting Sx should indicate to Alpine-Ridge DP whether there was a Thunderbolt device connected before entering Sx.

This update is done by the BIOS, through the PCIE2TBT mailbox (Sx_Exit_TBT_Connected or Sx_Exit_No_TBT_Connected messages). Alpine-Ridge DP will fully power up after any Sx exit to allow this update.

According to the BIOS message, Alpine-Ridge DP will perform either a fast link bring-up (if there were Thunderbolt devices connected before Sx entry) or a regular link bring-up (if there were no Thunderbolt devices connected before entering Sx).

7.2.2 Sx Entry/Exit Flows for Alpine-Ridge DP Host with external Connection Manager

The following sections describe the Sx entry/exit flows for Alpine-Ridge DP hosts with an external CM.

Further details required for External Connection Manager (CM) implementation are detailed in Appendix A: External Connection Manager Guidelines: A.1 Sx Entry/ Exit Flow - Implementation Details.

7.2.2.1 7.2.2.1Sx Entry Flow for Alpine-Ridge DP Host

Entering Sx is a 2 phase process:

1. Phase 1 - Sx setup - The Alpine-Ridge DP host receives a go2sx message through the PCIE2TBT mailbox. It then prepares the entire Thunderbolt topology for Sx entry. When all preparations are done an ok2go2sx message is sent through the TBT2PCIE mailbox. Active re-drivers are shut down during this phase.
2. Phase 2 - Sx entry - Host Alpine-Ridge DP PERST_N is asserted and the entire topology goes to Sx. Alpine-Ridge DP shuts down all its domains keeping the POC domain up.

Host system should not assert PERST_N before the ok2go2sx message is received. Alpine-Ridge DP controller will power off its CIO, PCIe, USB, DP, ANA_COM and LC domains within a few ms after PERST_N assertion.

Alpine-Ridge DP host will not assert GPIO_5 during Sx entry.

Sx entry in case no Thunderbolt cable is attached is a single phase procedure. Alpine-Ridge DP host will not wait for PERST_N assertion in order to shut down its CIO, PCIe, USB, DP, ANA_COM and LC domains.

Host providing power should retain both VCC3P3_S0 and VCC3P3_SX power rails similar to S0.

7.2.2.2 Sx Exit Flow for Alpine-Ridge DP Hosts

An Alpine-Ridge DP host will wake from Sx on the following events:

- POC_GPIO_3 asserted
- LSRX toggle - indicating Thunderbolt wake - a wake event from a Thunderbolt device in the Thunderbolt domain.

Upon Thunderbolt wake, Alpine-Ridge DP will assert GPIO_4 until PERST_N is deasserted. GPIO_4 will not be asserted if host woke up due to POC_GPIO_3 assertion.

Host system is expected to power on as soon as it was instructed to wake (from Thunderbolt or any other source).

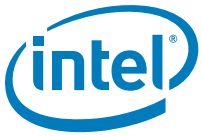
In case of Thunderbolt wake, Alpine-Ridge DP host will delay CIO, PCIe, USB, DP, ANA_COM domains power on until POC_GPIO_3.

7.2.3 Host S5 handling

During S5, Host system should:

1 Assert RESET_N

2 Completely power off Alpine-Ridge DP (optional).



8.0 In-line Functionality

8.1 Thunderbolt Base Protocol Functionality

The Alpine-Ridge DP controller implements the Thunderbolt base protocol functionality as defined by the Thunderbolt protocol specification, this includes the base protocol as well as the Thunderbolt Host interface adapter, PCIe adapter and DisplayPort adapter.

For more details please refer to the Thunderbolt Protocol Specification.

8.2 Lane Speed

Alpine-Ridge DP controllers supports two lane speeds 10Gbps and 20Gbps. By default, Alpine-Ridge DP publishes support for lane speed of 20Gbps. Lane speed may be changed by the connection manager.

Both lanes of the same port (P1+P2 or P3+P4) should always use the same lane speed. Different ports may use different lane speeds. A lane will come up at 20Gbps only if both the cable and link partner support 20Gbps. Upon cable plug the link controller sets the link speed, before the lane is enabled

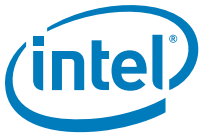
8.2.1 Lane Speed Transition

Speed transition is usually initiated by the connection manager by following the steps below:

- Connection Manager configures the required speed at the down facing ports, by setting PHY_PORT_CS_1/Target_Link_Speed[3:0]. The same setting should be set in both lanes of the down facing port
- Connection Manager sets Link Controller SW_FW_MAILBOX_IN/sw_force_lstx_low[6] (on hosts, cio power should be forced during this stage)
- The Link Controller will force lstx low and disable the high speed link
- Connection Manager clears Link Controller SW_FW_MAILBOX_IN/sw_force_lstx_low[6]
- After at least 100ms. The Link Controller releases lstx and enables the high speed link
- The speed is set to the maximum of the value set in PHY_PORT_CS_1/Target_Link_Speed[3:0], the link partner and the cable
- The negotiated speed is reported at PHY_PORT_CS_1/Current_Link_Speed[19:16]

8.3 Lane Bonding

Lane Bonding or Lane Aggregation is the process of joining 2 physical lanes (running between two Thunderbolt ports) into a single, double width, logical link. Alpine-Ridge DP supports Lane Bonding. The double width link allows better utilization of the Thunderbolt link by the tunneled protocols.



8.3.1 Lane Bonding Enablement

Lane Bonding is enabled when both ends of the link support and publish dual lane capability. By default, in order to support Legacy hosts, all devices will initially publish single lane capability. It is the responsibility of the CM (internal or external) to upgrade the link to Dual width if both ends support it.

Lane bonding is supported for each port pair (P1+P2, and P3+P4) separately.

Note: Lane bonding when lane speed is 10Gbps creates a link of 20Gbps, when lane speed is 20Gbps the logical link speed will be 40Gbps.

8.3.2 Lane Width Transitions

CM may change the link width or disable a port as long as it follows the directions in the table below. The required actions column refers to fields in PHY_PORT_CS_1 (Target Link Width[7:4], Link disable[14], Link Retrain[15]) of the relevant port. The negotiated width is published at the same register (Negotiated Link Width [23:20]). When transiting between single and bonded modes, CM must teardown all active paths prior to width transition.

The table lists the required actions to control ports P1+P2. Controlling ports P3+P4 is done in the same manner, respectively. The table also includes the expected plug/unplug events per transition.

Table 427. Required actions to control ports P1+P2

#	Strat Mode	Require Mode	Require Actions	Results	Comments
1	Bonded Link up	2 Single Lanes up	P1 width=1 P2 width=1, retrain=1	Plug event on P2	TS only. Takes ~640ns. No link drop
2	2 Single Lanes Up	Bonded Link up	Partner P1 width=3 Partner P2 width=3 P1 width=3 P2 width=3, retrain=1	Unplug event on P2	TS only. Takes ~640ns. No link drop
3	Bonded Link up	Both lanes disabled	P2 disable=1 P1 disable=1	Unplug event on P1	
4	Single Lane Up	Single Lane disabled	Pn disable=1, width=1	Unplug event on Pn	Same as in Old-Ridge
5	Single Lane Disabled	Single Lane up	Pn disable=0, width=1	Plug event on Pn	Same as in Old-Ridge
6	Lanes Disabled	Bonded Link up	Do flow 5 for P1, P2. Wait for both plug events Do flow 2		(upstream unplug will cause the partner ports to reset to single)
7	Bonded Link up	Single Lane up, Single Lane disabled	Do flows 1, 4		
8	Single Lane up, Single disabled	Bonded Link up	Do flow 5, wait for plug event, do flow 2		

8.3.3 Lane Monitoring of a Bonded Link

Lane monitoring is enabled also for a bonded link. In case of a Dual link stuck at training or increasing HEC errors count, both ports will be enabled/disabled.

8.4 Security Schemes

Alpine-Ridge DP supports different levels of security for device connection and PCIe tunneling.

See Table 428 for Alpine-Ridge DP defined security levels.

Table 428. Defined Security Levels

Value	Description
0x0	No Security - Allow legacy Thunderbolt devices auto connect – at this mode the connection manager auto connects to a new device plugged in
0x1	User Authorization - Allow User Notification devices at minimum – at this mode the connection manager requests connection approval from the host SW, auto approval may be given based on the Unique ID of the connecting device
0x2	Secure Connect - Allow One time saved key devices at minimum – at this mode the connection manager requests connection approval from the host SW, auto approval is only given if the host challenge to the device is acceptable
0x3	Display Port Only - Allow only DP sinks to be connected (re-driver or DP tunnel, no PCIe tunneling) – at this mode no tunneling is done for PCIe devices
0xF:4	Reserved

Alpine-Ridge DP Unique ID is fused in the Thunderbolt controller as part of the manufacturing process. Once set the Unique ID can't be altered.

The default value of the security level for the Alpine-Ridge DP device is loaded from flash memory. The default security level is 0x1

8.4.1 User Authorization

At this security level the connecting device indicates the CM of the Thunderbolt link connection; the CM requests host driver approval for the specific Unique ID that got connected prior to the PCIe tunnel creation. During the first connection of a unique ID the user will be prompt to approve.

The user will need to approve the interface and choose between a single/permanent/no connection approval.

Once a device is approved for permanent auto connect, its unique ID is saved by the SW as part of an ACL list for future auto connection (no user involvement).

8.4.2 Secure Connect

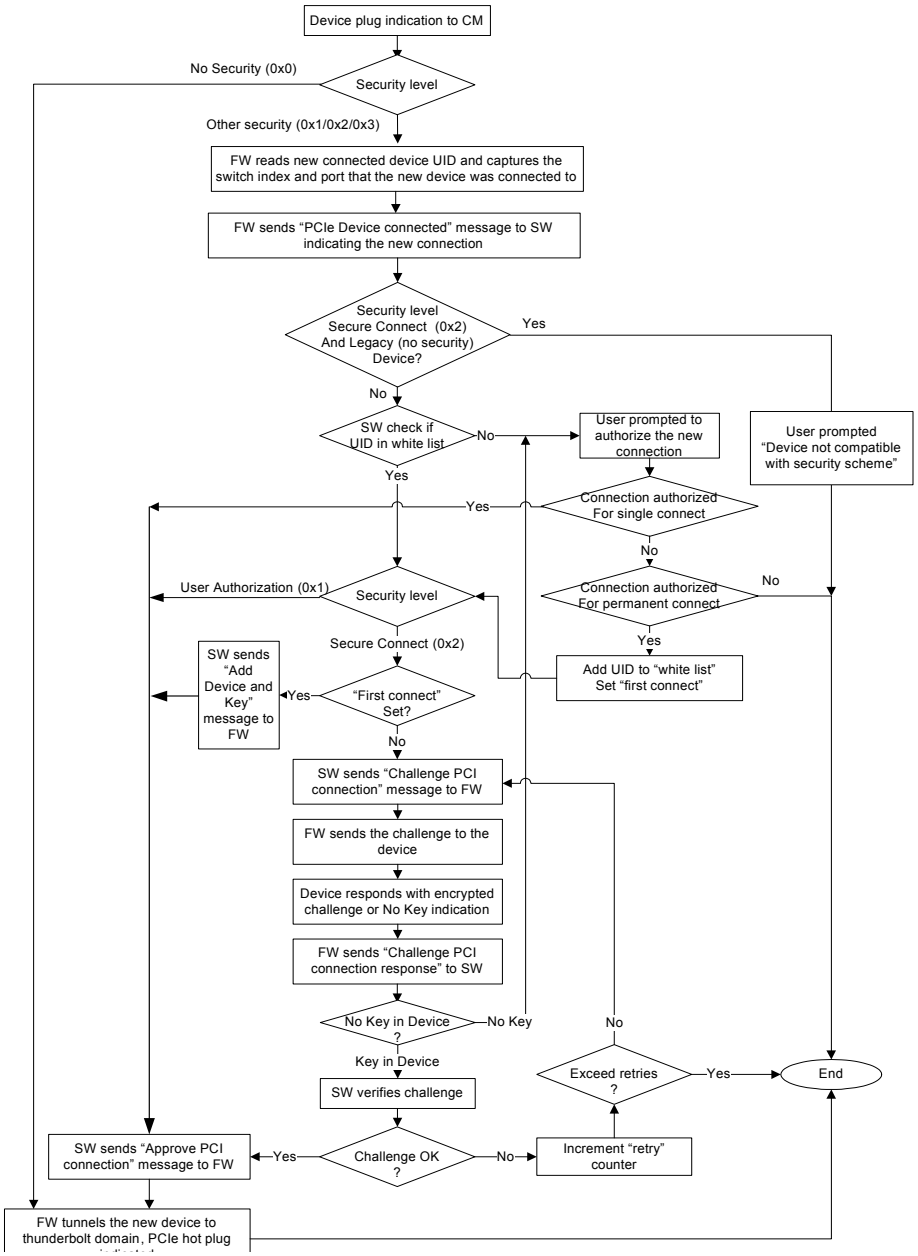
This level of security will not be available on Controllers prior to Falcon-Ridge generation.

At this security level the connecting device indicates the CM of the Thunderbolt link connection; the CM requests host driver approval for the specific Unique ID that got connected prior to Thunderbolt tunnel creation. During the first connection of a unique ID the user will be prompt to approve.

Once a device is approved by the user, the host would generate and send to the device a random Key. Together with the Unique ID the device will be added to the ACL list for future auto connection (no user involvement). On future connections of the same device the Unique ID is sent to the host, the host sends the device a challenge (random number value) and expects to get the value encrypted using the pre assigned key. Once received, the host checks the encryption and approves/rejects the tunnel creation to the CM.

If the process fails a pre-set number of times - the SW would treat the device as a new device connected and prompt the user to re-approve.

Figure 78. Device Authorization Sequence



8.4.3 Security Level Change

As needed the security levels can be changed by the user at the BIOS menu by communicating with the CM through the PCIE2TBT/TBT2PCIE mailbox utilizing the following flow:

- BIOS drives POC_GPIO_3 high
- BIOS enumerates the Host Router (if needed)
- BIOS uses the PCIE2TBT mailbox to set the new security level (Command = "Set security level")
- CM gets the new security settings
- CM verifies POC_GPIO_3 is set by checking gpio_data_in[3]
- If set CM updates the new security mode in NVM
- If cleared security setting will not be updated in NVM
- CM completes the SW transaction by indicating Set security level Done in the TBT2PCIE register with the security settings as received from the PCIE2TBT command
- On a security mode change CM disconnects all PCIe paths, PCIe paths can re-connect on security level 0x0 only, other security levels will require user approval as the ACL list should be cleared
- BIOS polls the TBT2PCIE register to get the "Done" indication
- BIOS should use the PCIE2TBT mailbox to verify the new security level was set (Command = “Get security level”)
- CM completes the SW transaction by indicating Get security level Done in the TBT2PCIE register with the security settings from NVM
- BIOS drives POC_GPIO_3 low
- Driver should clear the saved ACL list on any security mode change
- The driver is notified of the current security level in the Driver Ready Response message

8.5 Quality of Service (QoS) support

Thunderbolt protocol tunnels DisplayPort and PCIe protocol across the Thunderbolt domain, DisplayPort traffic is isochronous and as such is given the highest priority when tunneled over Thunderbolt. PCIe traffic can be either isochronous or bulk/best effort. Alpine-Ridge DP implements quality of service features to enable different PCIe traffic types/streams get different priorities and/or allocation as part of the Thunderbolt tunneled PCIe traffic for devices that require such capabilities.

The capabilities added in Alpine-Ridge DP include:

- Two virtual channels (VC) within the PCIe domain to be used for upstream Rd/Wr and downstream completions to enable higher priority (ISOC) traffic to bypass bulk PCIe traffic
- Completion Allocation buffers inside DN bridges per VC to allow draining downstream completion from UP bridge Flow control buffer
- Ability to restrict the outstanding upstream reads sent from an upstream/downstream bridge to the amount of buffering supported in the completion buffer of that UP/DN bridge

8.5.1 Completion Allocation Buffers (CAB)/Memory read moderation

Preallocate completion buffers in downstream bridges, prior to sending read request up to root complex so a downstream port doesn’t block other downstream ports, and limit the amount of memory read requests sent to the Root complex

When read request is processed, completions stream at wire speed down and do not block other requesters completions. If no space in completion buffers, read request is not sent upstream, Such preallocation is needed only in DS bridges that face PCIe over TBT tunnels. Physical devices are expected to be ready to drain completions without back pressure

Preallocation buffers (and configurations) are provided for both VC0 and VC1 priority channels.

8.5.1.1 CAB SW Control

CAB control contains enabling of Completion Allocation Buffer inside Downstream Port and option to limit the amount of outstanding read requests in upstream direction. The read moderation can be applied in Downstream Port or Upstream Port.

Two Vendor Registers (per bridge) controls these (one for each VC):

- VESC_REG 18 (Offset 550h): CAB VC0 register
- VESC_REG 19 (Offset 554h): CAB VC1 register

The structure of these two register is identical, main controls described below (for the full register description"VESC_REG 18 (Offset 50h): CAB VC0 register"and "VESC_REG 18 (Offset 50h): CAB VC0 register")

- Bit 0 enables the Completion Allocation Buffer (valid for DN port), When 0, completions flowing towards this DN port will be stored only in the common completion buffer of the US port (legacy mode)
- Bit 1 enables the MemRd moderation
- Bits 31:16 is the threshold of outstanding data in DW (loaded with bit 2)

These registers enable the configuration of the following functionalities:

Downstream Port:

- Ability to enable (per VC) the completion buffer
- Ability to control (per VC) the outstanding upstream read request data in each downstream port

Upstream Port:

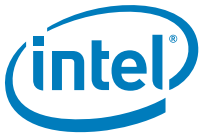
- Ability to control (per VC) the outstanding upstream read request data in the upstream port

8.5.2 Virtual Channel Support

Virtual channel implementation is according to PCIe 3.0 specification, for all traffic types (Posted, None Posted, Completions). Two virtual channels have been implemented VC0, VC1 including VC Extended Capability, Flow Control buffers per VC and VC arbitration inside PCIe Switch.

VC0/VC1 fully supported within PCIe in Thunderbolt along with set of custom capabilities to enable:

- Ability to configure VC1 from Vendor Register, that act as shadow registers for the VC Extended Capability, to hide from PCIE Software any existence of VC1 channel.
- Custom Weighted Round Robin VC Arbitration control from Vendor Registers instead VC Extended Capability tables.
- Physical PCIe links to support only VC0 and still route ingress / egress traffic to VC0 or VC1 channel (these for the links connecting to the root port, end point or legacy Thunderbolt devices)
- Ingress and Egress TC re-mapping, including some flexible configuration per Requester ID, to be used on the physical facing downstream bridges



These can be summarized by four traffic flows:

1. Upstream memory requests (MemWr / MemRd)
   — Memory TC can be remapped to TCx inside the Downstream Port facing endpoint to flow on VC1
   — Upstream Port facing Root Complex will remap only MemWr TCx back to TC0
2. Upstream completions (Cpl / CplD) stay as is with TC0 on VC0 channel, and additional custom implementation will allow upstream VC0 Completion to push upstream VC0 and VC1 posted packets.
3. Downstream completions (CplD)
   — Root complex returns completions with the same TCx value of the respective request
   — Downstream ports facing Endpoint will remap Cmpl TCx back to TC0
4. Downstream memory request (MemWr / MemRd) stay as is with TC0 on VC0 channel.

8.5.2.1 Custom VC SW Control

QoS by default is controlled from VC Extended Capability (VC1 enable and TC/VC mapping) as described in PCIe Specification.

But for supporting of custom VC in Thunderbolt there are additional custom set of controls.

Several bits and registers controls these custom additional features:

- VESC_REG 2 (Offset 510h) bit 2 - Master VC1 enable for PCIe Switch and should be set in Upstream Port

Per Bridge configuration:

- VESC_REG 21 (Offset 55Ch): QoS - Load priority & Custom mode register
- VESC_REG 22 (Offset 560h): Shadow port VC Capability and VC Resource Control register
- VESC_REG 23 (Offset 564h): TX and Rx TC remapping register
- VESC_REG 24-31 (Offset 568h - 584h): Rx remapping BDF tables.

8.5.2.2 Custom Mode Control

PCIe Port (Upstream or Downstream) can be configured either to custom VC mode in which both VC0 and VC1 are enabled on the PCIe link and the only difference from Specification mode is that it is controlled from vendor registers or Port can be configured to be in custom VC0 only mode in which only VC0 is enabled externally on the link, while internally it has VC1 channel + VC1 Flow Control Buffers and Ingress / Egress TC remapping is used to adapt between these two parts.

There would be four modes of configuration/operation and any Thunderbolt PCIe Bridge that is enabled for custom VC will need to be configured as one of these 4 options:

1. Upstream facing Root (physical link of Host controller or upstream Alpine-Ridge DP port facing legacy Thunderbolt device) custom VC0 only mode + Egress TC remapping + Upstream read moderation
2. Downstream facing TBT (Downstream Alpine-Ridge DP port facing Alpine-Ridge DP device) custom VC0 + VC1 mode + TC/VC mapping + CAB + DN read moderation
3. Upstream facing TBT (Upstream Alpine-Ridge DP port facing Alpine-Ridge DP Host/Device) - custom VC0 + VC1 mode + upstream read moderation

4. Downstream facing Endpoint (physical link of Alpine-Ridge DP Device port or downstream Alpine-Ridge DP port facing Thunderbolt legacy device) custom VC0 only mode + Ingress / Egress TC remapping + CAB + DN read moderation

General Port mode is controlled with VESC_REG 21 bits 25,24 (custom mode is enabled through bit 24 and setting also bit 25 will put the port to custom VC0 mode)

8.5.2.3 VC Arbitration control

There are two stages of VC arbitration in egress of each PCIE Bridge.

1. First stage resides in PCIE Switch interconnection and it is WRR within each VC per packet type (NP,P,CMPL)
2. Second stage resides in PCIE Bridge before Retry Buffer and it is WRR between VC over all packet types (NP/P/CMPL)

VC arbitration is controlled by simple priority value of each stage which defines the ratio between VC1 and VC0 packets.

First arbitration stage is controlled by stage VESC_REG 21 bits [7:0] (which is loaded with bit 16)

Second arbitration stage is controlled by stage VESC_REG 21 bits [15:8] (which is loaded with bit 18)

Actual Use:

- Downstream
  - — Weighted Round Robin arbitration (control) of data completion between VCs
  - — Weighted Round Robin arbitration (control) over all Types (C, P, NP) between VCs
- Upstream
  - — Round Robin arbitration between downstream Ports per type per VC (no SW control)
  - — Weighted Round Robin arbitration (control) per Type (P, NP) between VCs
  - — Weighted Round Robin arbitration (control) over all Types (P, NP) between VCs

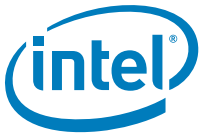
8.5.2.4 Shadow VC1 control

When custom mode is enabled VC Extended Capability doesn’t have any effect and should stay as if only VC0 is enabled (with all TC mapped to VC0).

VESC_REG 22 acts as minimized shadow register for several registers in VC Extended Capability and controls the VC1 enable + TC/VC remapping.

- Bits [15:0] are used as shadow for Port VC Capability Register 1.
  - — Bits [2:0] and [6:4] are Extended VC count fields and should be loaded to 001b
- Bits [31:16] are used as shadow VC Resource Control Register for VC1.
  - — Bit 31 is VC1 enable and bits [26:24] is the VC ID, which should be loaded to 001b
  - — Bits [23:16] are the TC/VC1 mapping (TC/VC0 mapping will be complement to this configuration)

Note: these configuration should be done in all VC1 related ports (in regular custom mode and also in custom VC0 mode)



8.5.2.5 TC Remapping control

VESC_REG 23 is the main register that controls Ingress / Egress TC remapping which should be used at ports in custom VC0 only modes in order to prioritize some traffic and rout it to VC1 channel within PCIE Switch.

VESC_REG 23 Bits [15:0] are used to control Tx/Egress TC remapping.

- Bits 3:0 are per packet type bits that enables to remap all TC to TC0, before packet is transmitted
- Bits 7:4 are per packet type bits that enables to remap one specific TC (bits 10:8) to TC0, before packet is transmitted

VESC_REG 23 Bits [31:16] are used as shadow Rx / Ingress TC remapping.

- Bits 19:16 are per packet type bits that enables to remap all incoming packets to specific TC (bits 22:20)
- Bits 26:23 are per packet type bits that enables to remap incoming packets with non-matching BDF to BDF table to specific TC (bits 29:27)

Note: If Ingress TC remapping is not enabled globally, then BDF table is used and if packet doesn't match the table the default option is used.

VESC_REG 24-31 are registers that acts as 8 entry table for the Ingress TC remapping and enables to do the remapping based on

The structure of each entry is similar:

- Bits 3:0 are per packet type bits that enables to remap TC of incoming packets that their BDF matches bits 31:16 to specific TC (bits 6:4)
- Bit 7 enables to ignore function number, which enables to treat Multi-function Device as one unit and remap all its packets.

These registers enable the configuration of the following functionalities:

- Downstream Port
  - Ingress TC remapping per type either for whole traffic or per Requester ID (to be used for P, NP)
  - Egress TC remapping per type (to be used only for Cmpl)
- Upstream Port
  - Egress TC remapping per type (to be used only for P)

8.5.3 QoS Configuration flow

The configuration flow should be done according to the following steps

- Power up of Host/Device
- NVM based configurations - General VC1 settings, initial setup of WRR arbitration + default TC re-mapping + default CAB and read moderation, none of these features is enabled
- Thunderbolt link established
- CM reads host/device characteristics from NVM (DROM)
- CM updates the configuration as needed and enables the proper functionalities (Impacted by upstream/downstream device type and topology in the daisy chain)
- PCIe tunnel created, PCIe link up, PCIe enumerated

- CM/SW updates last configurations as needed - TC remapping on BDF configuration (if needed), read moderation throughout the Thunderbolt tree (as needed), need to avoid this configuration during traffic (device needs to be idle/paused), Dynamic Host upstream configuration could change (enable VC1/TC remapping) if a QoS device was connected

DROM content should add characteristics that would help CM configuration and should reflect:

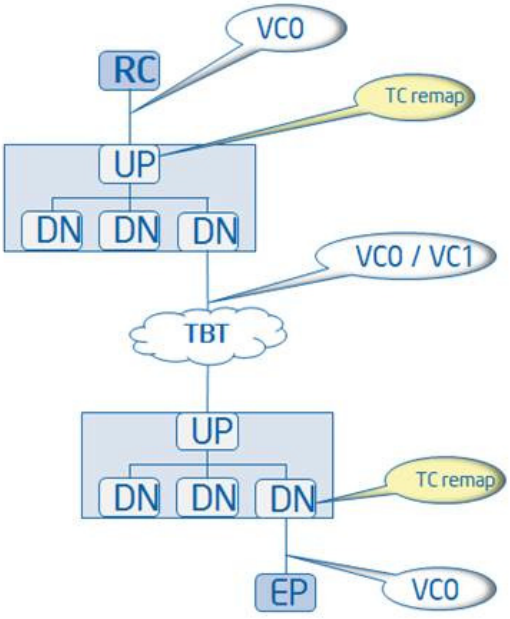
- Per downstream bridge information:
- Per direction (Up/Dn) Max BW (global)
- Per direction (Up/Dn) Min BW (ISOC)
- Number of PCIe functions (for MFD)
- Max outstanding read data (in Bytes)

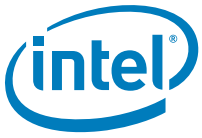
8.5.4 Basic register configuration for the four different modes of operation (Example):

As indicated there are basically four main options to enable custom VC1 depends on Port type and if it faces Thunderbolt link or not.

Over Thunderbolt link with partner that supports as well VC1 the link can be with two channels (Same as regular Spec mode, just controlled from vendor registers).

Port that faces physical link (or legacy Thunderbolt device that doesn't support VC1) the custom VC will be configured internally only, using TC remapping.





8.5.4.1 Upstream facing physical link (Root)

This port is in custom VC0 only mode with additional configuration of Egress (P) TC remapping and TC/VC mapping.

MemRd moderation can be configured to limit overall outstanding read request that flows toward Root.

- VESC_REG 18 (offset 0x550)
  - vesc_reg18[1] - VC0 MemRd moderation enable in Upstream Port
  - vesc_reg18[2], [31:16] - Load MemRd moderation threshold for VC0 in units of DW
- VESC_REG 2 (offset 0x510)
  - vsec_reg2[30] - Enable VC1 in PCIE Switch
  - vesc_reg2[28] - Bypass Credit Check
- VESC_REG 21 (offset 0x55C)
  - vsec_reg21[25], [24] - Custom VC0 only mode (VC0 only)
  - vsec_reg21[30], [29], [26] - Rx TC/VC map according to Spec (0xFF) + map according to source
  - vesc_reg21[16], [7:0] = 08h to set per type arbitration (or other required priority value)
  - vesc_reg21[18], [15:8] = 08h to set over all type arbitration (or other required priority value)
- VESC_REG 22 (offset 0x560)
  - vsec_reg22[31], [26:24] = 001b, [23:16] = 02h - Shadow Register to map TC1 to VC1 (also possible other mapping, for example 0xFE)
- VESC_REG 23 (offset 0x564)
  - vsec_reg23[0] - Re-Map all Posted back to TC = 0

8.5.4.2 Downstream facing link over TBT domain

This port is in custom VC0 + VC1 mode with configuration of TC/VC mapping (VC0 and VC1 credits are exchanged with partner over TBT link)

CAB buffer along with MemRd moderation can be configured to limit outstanding read request that flows toward Root.

- VESC_REG 18 (offset 0x550)
  - vesc_reg18[0] - VC0 CAB enable in Downstream Port
  - vesc_reg18[1] - VC0 MemRd moderation enable in Downstream Port
  - vesc_reg18[2], [31:16] = 0080h - Load MemRd moderation threshold for VC0 in units of DW (to 4K bit = 128 DWs)
- VESC_REG 21 (offset 0x55C)
  - vsec_reg21[24] - Custom VC mode
  - vsec_reg21[30], [29], [26] - Rx TC/VC map according to Spec (0xFF) + map according to source
  - vesc_reg21[16], [7:0] = 08h to set per type arbitration (or other required priority value)
  - vesc_reg21[18], [15:8] = 08h to set over all type arbitration (or other required priority value)
- VESC_REG 22 (offset 0x560)

  - vsec_reg22[31], [26:24] = 001b, [23:16] = 02h - Shadow Register to map TC1 to VC1 (also possible other mapping, for example 0xFE)

8.5.4.3 Upstream facing link over TBT domain

This port is in custom VC0 + VC1 mode with configuration of TC/VC mapping (VC0 and VC1 credits are exchanged with partner over TBT link).

- VESC_REG 2 (offset 0x510)
  - vsec_reg2[30] - Enable VC1 in PCIE Switch
- VESC_REG 21 (offset 0x55C)
  - vsec_reg21[24] - Custom VC mode
  - vsec_reg21[30], [29], [26] - Rx TC/VC map according to Spec (0xFF) + map according to source
  - vesc_reg21[16], [7:0] = 08h to set per type arbitration (or other required priority value)
  - vesc_reg21[18], [15:8] = 08h to set over all type arbitration (or other required priority value)
- VESC_REG 22 (offset 0x560)
  - vsec_reg22[31], [26:24] = 001b, [23:16] = 02h - Shadow Register to map TC1 to VC1 (also possible other mapping, for example 0xFE)

8.5.4.4 8.5.4.4 Downstream facing physical link (Endpoint)

This port is in custom VC0 only mode with additional configuration of Ingress (NP/P) / Egress (Cmpl) TC remapping and TC/VC mapping.

- VESC_REG 2 (offset 0x510)
  - vesc_reg2[28] - Bypass Credit Check
- VESC_REG 21 (offset 0x55C)
  - vsec_reg21[25], [24] - Custom VC0 only mode (VC0 only) + map according to source + Rx TC/VC map according to Spec FF reg
  - vsec_reg21[30], [29], [26] - Rx TC/VC map according to Spec (0xFF) + map according to source
  - vesc_reg21[16], [7:0] = 08h to set per type arbitration (or other required priority value)
  - vesc_reg21[18], [15:8] = 08h to set over all type arbitration (or other required priority value)
- VESC_REG 22 (offset 0x560)
  - vsec_reg22[31], [26:24] = 001b, [23:16] = 02h - Shadow Register to map TC1 to VC1 (also possible other mapping, for example 0xFE)
- VESC_REG 23 (offset 0x564)
  - vsec_reg23[2] - Re-Map all Completions back to TC = 0.
  - vsec_reg23[16], [17], [22:20] = 001b - Re-Map all Rx Posted and Non-Posted to TC1 (also possible to configure the BDF table instead)

8.6 PCIe Phy Eye Monitor

The Alpine-Ridge DP PHY features the capability to perform on-chip eye diagram scan at the receiver, which allows the user to "see" the eye opening (height and width) of the received data after equalization. This is a frequently utilized tool enabling characterization of the receiver equalizer.

8.6.1 Overview

The on-chip eye feature works by sweeping the time-axis (x) and the voltage-axis (y), and the corresponding bit error ratio is calculated by comparing "roaming" sample with the data sample. BER is a function of x-offset and y-offset, and it is calculated at each (x-offset, y-offset) point. The result of a BER scan eye diagram is a two-dimensional matrix that can be displayed using different color shades representing varying BER values.

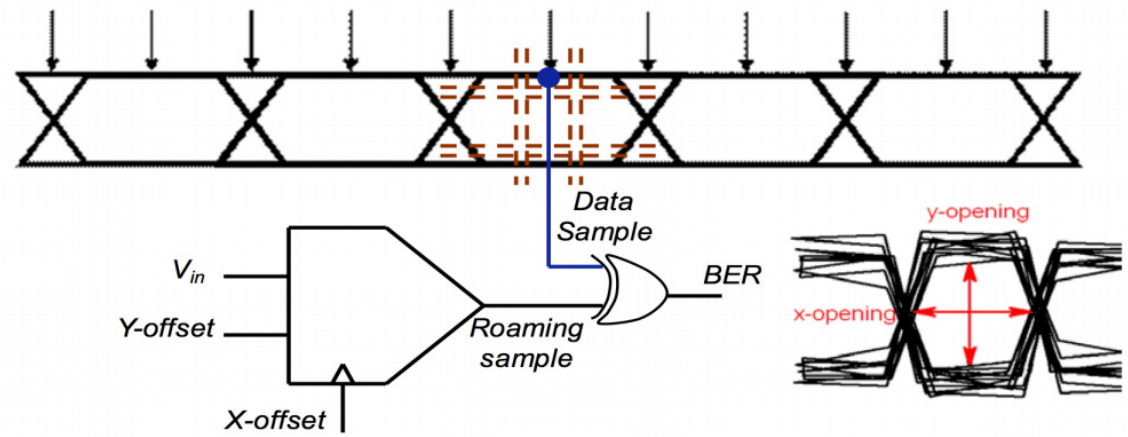


Figure 1. Overview of On-chip Eye Measurement

The on-chip eye measurement can occur during normal operation of the link, and is non-destructive to the link. The on-chip eye is "data-agnostic" - it does not require any specific data sequence and can be used with any PRBS sequence.

The measurement procedure is intended to be implemented in software on the host system. The software needs to read/write the registers that program the x- and y-offset sweeps, and read out the BER measurement for each corresponding point. Once all of the data points have been captured, a 2-D image may be plotted based on the results. An example eye plot captured for 10Gbps data using x-offset of 3ps, y-offset of 20mV, and 562 receive data bits is shown in Figure 2.

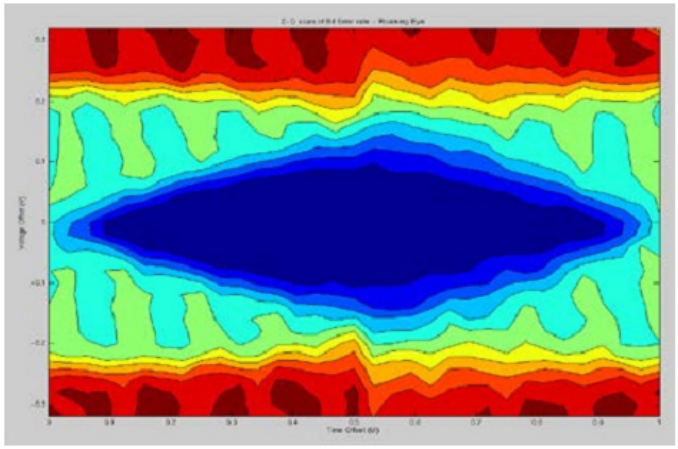


Figure 2. Example BER Eye Plot

Although BER scan eye diagram shows the eye opening of the received signal after equalization, it is not as intuitive as the eye diagrams generated on an oscilloscope. To gain better understanding of the variation in BER captured in the entire range, we need to know the rate of change when the x-offset steps into the next bit or when the y-offset crosses the next level. This is achieved by taking derivatives of the BER in both x-offset and y-offset directions, and combing the two gradient maps into a single map by calculating the root of the square sum of the two gradients. Aside from the eye opening information, this gradient plot also lets you know the transitions and crossing points. As an example, Figure 3 shows a simulated eye on the left and its corresponding gradient plot on the left.

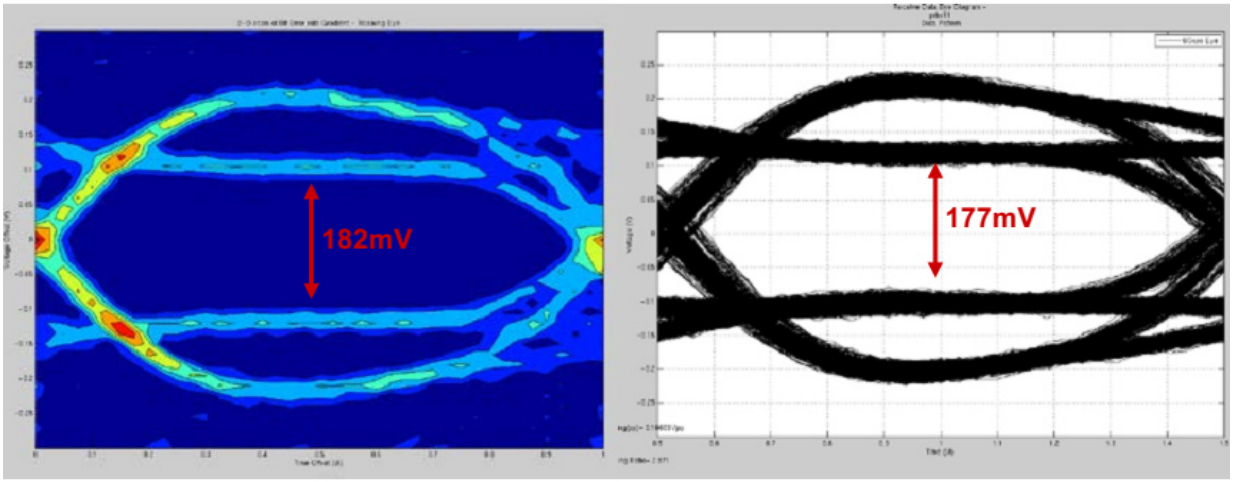
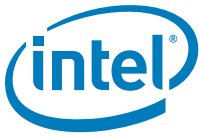


Figure 3. Left – Gradient of BER Plot, Right – Simulated Eye

For the x-offset (time), the offset can be set to address the full horizontal eye opening; for the y-offset (amplitude), the offset can be set to address ±256mV.

X-offset (Time) - Resolution: 2ps ± 1ps, Range: 1UI

Y-offset (Amplitude) - Resolution: 4mV, Range: +/-256mV



8.6.2 Measurement Procedure

The on-chip eye measurement can be made either in a test environment where the PHY TX sends out test patterns that are looped back externally off-chip to the RX, or in a normal link environment where the RX is receiving data from the TX at the other end of the link.

To measure the on-chip eye:

1. RX serial data pattern is provided either directly through the RX pads or through the loop back of the TX serial output (one of the available patterns used in the BIST must be provided).

2. Setup the x/y-offset resolution, the number of bits to accumulate for each measurement point, and the color-coding scheme representing the number of errors accumulated.

3. Use the AHB interface to shift the y-offset and x-offset relative to the sampling clock.

4. For each shift, wait the amount of time needed to accumulate the number of bits specified and count the number of bit errors by reading the AHB register eye_scan_wait_len.

5. After all sweeps are done, post-process the data and display the eye.

8.6.3 Measurement procedure pseudo-code

```
##########################################################
## Psudo code
##########################################################

write_ahb(Device, Address, value, mask)
- values in hex
- mask is an active enable signal (allows writing to the bits that are high)
read_ahb(device, address)
read_tbus(device, address)

#############################################
## Step1 - Setup PMA for eye monitor mode
#############################################

write_ahb(LANE,0x34,0x01,0x03)
write_ahb(LANE,0x38,0x04,0x0c)
write_ahb(LANE,0x63,0x10,0x10)
write_ahb(LANE,0x6A,0x01,0x03)
write_ahb(LANE,0x23,0x40,0xC0)
write_ahb(LANE,0x23,0x30,0x30)
write_ahb(LANE,0x65,0x10,0x10)
write_ahb(LANE,0x28,0x01,0x01)

#############################################
## Step2 - Setup Eye monitor Digital logic
#############################################

write_ahb(COMLANE,0x31,0x02,0x02)
write_ahb(COMLANE,0x35,0xFF,0xFF)
write_ahb(COMLANE,0x36,0x0F,0x0F)
write_ahb(COMLANE,0x31,0x04,0x04)
write_ahb(COMLANE,0x31,0xFB,0xFF)
write_ahb(COMLANE,0x32,0xFF,0xFF)
write_ahb(COMLANE,0x33,0x07,0x07)

#############################################
## Step3 - Eye monitor Loop
#############################################

write_ahb(LANE,0x65,0x00,0x01) // Select the coarse clock to use for X sweep
write_ahb(LANE,0x64,0x00,0x80)

For X = 0 to 127{
```

```
write_ahb(LANE,0x64,X,0x7F) // writes delay line value to be used for this instance of the eye monitor sweep
For Y = 0 to 256{
   write_ahb(LANE,0x28,2*Y,0xFE) // writes VSCAN offset value, I am attempting to capture left shift with 2*Y
   write_ahb(COMLANE,0x31,0x02,0x02) // enable eye scan run
   read_tbus(Lane, 0x8D)// Check that bit [8] eye_scan_cntr_ready_i = 1'b1
                        // Note you can wait for a programmable amount of time if you ensure it is longer than the dwell time
   read_tbus(Lane, 0x19)
   read_tbus(Lane, 0x1A)// Read Error count out of test bus. Typically this is recorded into a text file with X-location, y-location and error count
   write_ahb(COMLANE,0x31,0x00,0x02) // disable eye scan run
            }
   }
```

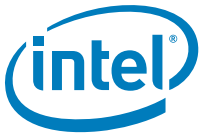
8.7 Display Port Phy Eye Monitor

The Alpine-Ridge DP controller implements integrated eye monitors capabilities to enable on chip eye diagram scan at the receiver. This simplifies the characterization and allows the user to see the eye opening (height and width) of the received data after equalization.

Note: The lanes denoted are all physical lanes. Writing to lane 0 will be directed to physical lane 0 regardless of the lane swapping indications.

8.7.1 Measurement procedure pseudo-code

```
#############################################################
## Pseudo code example for Lane0
#############################################################

write (Address, bits, Data)
read (Address, bits)

##############################################
## Step1 - Allow SW Control
##############################################

write_(0xD810, [7:0], 0x00)// ALLOW_RTL_EYEMON_CTRL
write (0xD811, [7:0], 0x00)// ALLOW_RTL_CTRLE_CTRL_ADR

##############################################
## Step2 - Read calibration point (eye's center)
##############################################

CAL_PI[7:0] = read (0xD613, [7:0]) // Read PI_CALIB_CACHE0L[7:0]
CAL_PI[9:8] = read (0xD614, [1:0]) // Read PI_CALIB_CACHE0H[1:0]

##############################################
## Step3 - Read Current location
##############################################

CUR_PI[7:0] = read (0xD642, [7:0]) // Read CUR_LOCATION0L[7:0]
CUR_PI[9:8] = read (0xD643, [1:0]) // Read CUR_LOCATION0H[1:0]

##############################################
## Step4 - Configure Eye monitor
##############################################

write_(0xD61F, [7:0], 0x10)// EYEMON_SYMBOL_COUNT_0L
write_(0xD620, [7:0], 0x27)// EYEMON_SYMBOL_COUNT_0M
write_(0xD621, [7:0], 0x00)// EYEMON_SYMBOL_COUNT_0H
write_(0xD61C, [7:0], 0x00)// EYEMON_MASK_SEL0

##############################################
## Step5 - Set the checking point at CHK_VT, CHK_PI
##############################################

If CHK_PI < CUR_PI {
        write (0xD652, [0], 0b) // Left (decrement phase)
        for I= 1 to (CHK_PI - CUR_PI) {
           write (0xD653, [0], 1b) // Single Step Strobe
```



```
        }
}
        else if CHK_PI > CUR_PI {
            write (0xD652, [0], 1b) // Right (increment phase)
            for I= 1 to (CUR_PI - CHK_PI) {
                    write (0xD653, [0], 1b) // Single Step Strobe
            }
        }
write_(0xD65C, [7:0], CHK_VT[7:0])// GP_LANE_REG0
        // The height to check: [7] is sign bit (1 is negative). [6:0] is magnitude. 1.87mV per step

write_(0xD61B, [1:0], 00b)// EYEMON_MODE0 (alignment)
write_(0xD617, [0], 1b)   // EYEMON_GO0
Poll and wait for the done bit to rise
        read (0xD634, [0])// EYEMON_DONE0

##############################################
## Step6 - Run the Check
##############################################

write_(0xD61B, [1:0], 01b)// EYEMON_MODE0
write_(0xD617, [0], 1b)   // EYEMON_GO0
Poll and wait for the done bit to rise
        read (0xD634, [0])// EYEMON_DONE0
Read the Error counters to check the number of errors in that location
        read (0xD62B, [7:0])// EYEMON_ERR_COUNT_0L
        read (0xD62C, [7:0])// EYEMON_ERR_COUNT_0M
        read (0xD62D, [7:0])// EYEMON_ERR_COUNT_0H
        read (0xD62E, [1:0])// EYEMON_ERR_COUNT_0VH

##############################################
## Step7 - Run the full Eye monitor test
##############################################

Scan the BER results across the 48 phase points 24 points from calibration, across the different voltage levels:

Get to the starting point:
Run Step5 with CHK_PI = CAL_PI-24
write (0xD652, [0], 1b) // Right (increment phase)

Run the full test:
For X = 0 to 47 {
        write (0xD653, [0], 1b) // Single Step Strobe
        write_(0xD61B, [1:0], 00b)// EYEMON_MODE0 (alignment)
        write_(0xD617, [0], 1b)  // EYEMON_GO0
        Poll and wait for the done bit to rise
            read (0xD634, [0])      // EYEMON_DONE0
        For Y = 0 to 255 {
            write_(0xD65C, [7:0], Y)// GP_LANE_REG0
            // The height to check: [7] is sign bit (1 is negative). [6:0] is magnitude. 1.87mV per step
            write_(0xD61B, [1:0], 00b)// EYEMON_MODE0
            write_(0xD617, [0], 1b)   // EYEMON_GO0
            Poll and wait for the done bit to rise
                    read (0xD634, [0])// EYEMON_DONE0
            Read (and capture) the Error counters to check the number of errors in each location
                    read (0xD62B, [7:0])// EYEMON_ERR_COUNT_0L
                    read (0xD62C, [7:0])// EYEMON_ERR_COUNT_0M
                    read (0xD62D, [7:0])// EYEMON_ERR_COUNT_0H
                   read (0xD62E, [1:0])// EYEMON_ERR_COUNT_0VH
        }
}
```

8.8 CIO Phy

8.8.1 CIO Phy NVM Configuration section

The cio phy config NVM section is located at beginning of the cio phy controller dram section, after the 2 size bytes. It holds phy configurations for PA and PB, as described in table below. Note that the offsets are in Bytes.

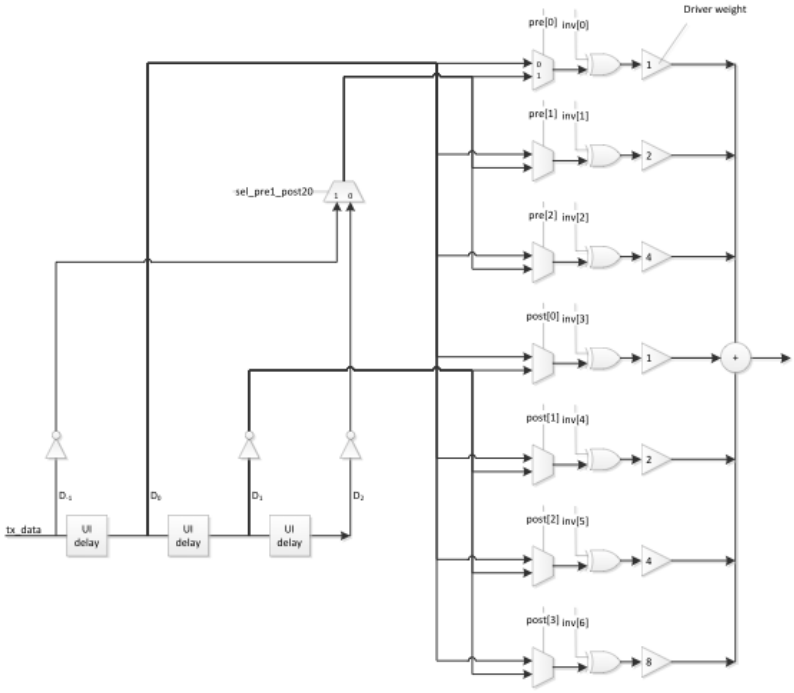
Byte Offset	Field Name	Description	Default
15:0	Header	holds a string to allow easy identification in the image	CIO_PHY_SECTION
16	PA_lane_np_swap	[7] -PA_RX1 NP swap [6] -PA_RX0 NP swap [5,4] -reserved. [3] -PA_TX1 NP swap [2] -PA_TX0 NP swap [1,0] -reserved.	0x0
17	PB_lane_np_swap	[7] -PB_RX1 NP swap [6] -PB_RX0 NP swap [5,4] -reserved. [3] -PB_TX1 NP swap [2] -PB_TX0 NP swap [1,0] -reserved.	0x0
19:18	Reserved		
23:20	Default_txffe_cio_20g_active_index[lane]	Default preset for a 20Gbps cio link when connected to an active cable. Byte per lane	0x0B0B0B0B
27:24	Reserved		
31:28	Default_txffe_cio_10g_active_index[lane]	Default preset for a 10Gbps cio link when connected to an active cable. Byte per lane	0x0
35:32	Default_txffe_cio_10g_passive_index[lane]	Default preset for a 10Gbps cio link when connected to a passive cable. Byte per lane	0x0B0B0B0B
43:36	usb3_lfps_txffe[lane]	Txffe settings for usb3 during lfps (see txffe section for more details). Word per lane. [15..12] – tx_sw_post1 [11] – tx_sw_sel_pre1_post20 [10..3] – tx_sw_inv [2:0] – tx_sw_pre	0x0

Byte Offset	Field Name	Description	Default
51:44	usb3_gen1_txffe[lane]	Txffe settings for usb3 gen1 (see txffe section for more details) Word per lane [15:12] - tx_sw_post1 [11] - tx_sw_sel_pre1_post20 [10:3] - tx_sw_inv [2:0] - tx_sw_pre	0x4800480048004800
59:52	usb3_gen2_txffe[lane]	Txffe settings for usb3 gen2 (see txffe section for more details). Word per lane [15:12] - tx_sw_post1 [11] - tx_sw_sel_pre1_post20 [10:3] - tx_sw_inv [2:0] - tx_sw_pre	0x3802380238023802
63:60	Reserved		

8.8.2 Transmitter Equalization (TXFFE)

8.8.2.1 Introduction

Alpine-Ridge DP transmitters at PA, PB and SRC0 share the same transmitter equalization structure, as shown in the figure below



Each transmitter consists of 7 drivers of different weights. Total weight of all drivers (full swing) is 22.

Three drivers (of weight 1, 2, 4) can be configured to drive either the main tap, pre-tap or post2 tap (controlled by tx_sw_pre[2:0], tx_sw_sel_pre1_post20).

Four drivers (of weight 1, 2, 4, 8) can be configured to drive either the main tap or the post1 tap (controlled by tx_sw_post[3:0])

Any driver can also be configured to driver the opposite value (tx_sw_inv[6:0]).

Example A: Full swing - C0=1 (22/22):

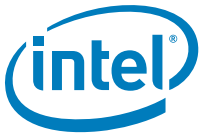
- tx_sw_pre= 3'b0
- tx_sw_post= 4'b0
- tx_sw_inv= 7'b0
- tx_sw_sel_pre1_post20= 1'b0 (or 1'b1).

Example B: C-1=-0.09 (-2/22), C0=0.77 (17/22), C1=-0.14 (-3/22):

- tx_sw_pre= 3'b010
- tx_sw_post= 4'b0011
- tx_sw_inv= 7'b0
- tx_sw_sel_pre1_post20= 1'b1

Example C: Low swing configuration, with post2: C0=0.68 (15/22), C1=-0.09 (-2/22), C2=-0.05(-1/22):

- tx_sw_pre= 3'b001



- tx_sw_post= 4'b0010
- tx_sw_inv= 7'b0000010
- tx_sw_sel_pre1_post20= 1'b0

8.8.2.2 CIO TXFFE Setup

Alpine-Ridge DP implements the CIO TXFFE presets table as defined in the TBT Interconnect Specification.

The default TXFFE preset can be configured in NVM (see cio phy NVM configuration), per connection type - 20Gbps, 10Gbps active or 10Gbps passive.

8.8.2.3 USB TXFFE Setup

Alpine-Ridge DP implements the USB TXFFE settings as defined in the USB Spec. The TXFFE settings are read from NVM, and can be modified per usb3 gen1 or gen2 (see cio phy NVM configuration section).

8.8.2.4 TXFFE Setup for DFT

User may change the TXFFE settings on-the-fly by directly modifying the per_lane.tx_ctrl_swing register once the transmitter is active. The settings may be overwritten upon enabling of the transmitter (reset to the NVM configuration), or upon partner request (CIO only).

8.8.3 Lane Swap Considerations

Alpine-Ridge DP port B (PB) is internally swapped in order to match the USB-C receptacle pin order. As a result, port B lane 0 is mapped to PB_TX1/PB_RX1 balls, and port B lane 1 is mapped to PB_TX0/RX0 balls. Any per_lane register access should consider this swap. For example, to enable PRBS on PB_TX0, port B lane1 registers should be used.

8.8.4 PRBS configuration

The sections below describe the procedure for enabling/disabling PRBS on PA/PB for CIO testing.

8.8.4.1 Enabling PRBS at the Transmitter

The following steps are required in order to transmit PRBS on PA/PB.

Note that some of the commands are per port and others are per lane. Repeat the commands as required.

1. Set the port to CIO mode with the required speed. Unless done externally, use the following LC registers (in this order):
   — Set LC.SW_FW_MAILBOX_IN.debug_halt_fw = 1'b1

— Set LC.LINK_MODE.lc_cio_speed (1'b0 for 10G, 1'b1 for 20G)
— Set LC.LINK_MODE.lc_cio_mode = 1'b1

Wait for per_port.common_lc_link_mode.phy_port_init_done == 1'b1

2. Enable the required lane transmitter. Unless done externally, use the following LC register:
   — Set LC.PHY_RX_TX_EN_REG.fw_en_tx_phy_l0/1 = 1'b1
   — Wait for per_lane.TX_CTRL.tx_is_active == 1'b1
3. Select the PRBS pattern to transmit by setting per_lane.TX_DFT_CTRL.dft_tx_prbs_sel
4. Enable the PRBS by setting per_lane.TX_DFT_CTRL.dft_en_tx_prbs = 1'b1
5. Disable the PRBS when done, by setting per_lane.TX_DFT_CTRL.dft_en_tx_prbs = 1'b0
6. Release the LC registers if needed, in the opposite order

8.8.4.2 Enabling the PRBS Checker at the Receiver

The following steps are required in order to check the received PRBS on PA/PB.

Note that some of the commands are per port and others are per lane. Repeat the commands as required.

1. Set the port to CIO mode with the required speed. Unless done externally, use the following LC registers (in this order):
   — Set LC.SW_FW_MAILBOX_IN.debug_halt_fw = 1'b1
   — Set LC.LINK_MODE.lc_cio_speed (1'b0 for 10G, 1'b1 for 20G)
   — Set LC.LINK_MODE.lc_cio_mode = 1'b1.

Wait for per_port.common_lc_link_mode.phy_port_init_done == 1'b1.

2. Make sure there is valid high speed data and enable the required receiver lane. Unless done externally, use the following LC register:
   — Set LC.PHY_RX_TX_EN_REG.fw_en_rx_phy_l0/1 = 1'b1
   — Wait for per_lane.CAR_CTRL.rx_eq_done == 1'b1
3. Select the PRBS pattern to compare by setting per_lane.RX_DFT_CTRL.dft_rx_prbs_sel
4. Enable the PRBS checker by setting per_lane.RX_DFT_CTRL.dft_en_rx_prbs = 1'b1

Verify that per_lane.RX_DFT_STATUS.dft_rx_prbs_ber_lock == 1'b1

5. Clear the error and symbol counters by setting per_lane.RX_DFT_CTRL.rx_ber_counter_clr = 1'b1
6. Enable the error and symbol counters by setting per_lane.RX_DFT_CTRL.rx_ber_counter_en = 1'b1
7. Stop the error and symbol counters after the required test time, by setting per_lane.RX_DFT_CTRL.rx_ber_counter_en = 1'b0
8. Verify that per_lane.RX_DFT_SYMBOL_COUNTER_HIGH/LOW match the test time
9. Read BER counter from per_lane.RX_DFT_BER_COUNTER.ber_cntr
10. Release the LC registers if needed, in the opposite order

8.8.5 PA/PB Rx Eye Quality

Once lock process is completed (per_lane.CAR_CTRL.rx_eq_done == 1'b1), the width of the equalized eye is available.

The eye opening in percentage is given by 100*(Width)/(Steps_per_UI).

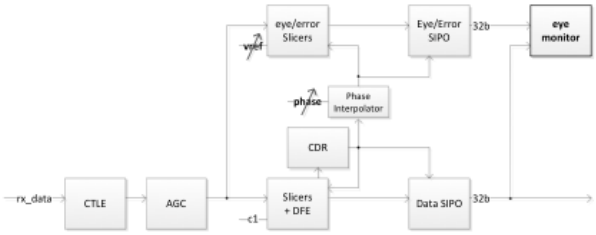
Width (measured in PI Steps) can be read from per_lane.LANE_MM4.best_eye_width.

Steps_per_UI can be obtained from the table below.

Mode	Speed (Gbps)	Steps per UI [PI steps]
CIO	20.625	64
CIO	10.3125	128
USB	10.0	128
USB	5.0	256

8.8.6 CIO Eye Monitor

The PA/PB main Rx phy modules are shown the image below.



The eye monitor is used to sample the input signal after applying CTLE and AGC corrections. It does not monitor the eye after DFE, though has the capabilities to represent such eye diagrams.

The eye monitor slicers sample the signal at a predefined location. It then compares the sampled values to the main data stream decisions, and counts the errors.

The eye monitor uses dedicated slicers, therefore can be used without affecting the main data stream (assuming it's used for limited periods and/or work conditions are kept the same). There are two slicers dedicated for the eye monitor, one sampling odd bits and the other sampling even bits. The slicers have separate voltage reference controls, though typically both should be set to the same value.

The eye monitor is also used for functional tasks during lock stage and afterwards, thus need to request control before using it and to properly release it when done. Note that the eye monitor is useless unless the rx CDR is locked.

The eye monitor sampling point can be moved vertically in both directions, by changing the voltage reference of the related slicers. The vertical resolution is ~2.36mv differential, with a total of 256 steps.

The sample point can also be moved horizontally in both directions. The step size for CIO / USB modes is ~0.76ps / ~0.78ps respectively. For CIO 20Gbps each UI is 64 steps. For CIO or USB at 10Gbps each UI is 128 steps. For USB 5Gbps, each UI is 256 steps.

8.8.6.1 CIO Eye Monitor activation flow

The following steps are required to enable the eye monitor:

1. Make sure rx CDR is locked - verify per_lane.CAR_CTRL.rx_eq_done == 1'b1
2. Request control for the eye monitor, by setting the sw_fw eyemon_request_control command in per_lane.SW_FW_MAILBOX. Wait for ack
3. Read the current horizontal position at per_lane.EYEMON_ANA.pi_phase_monitor. Keep this value, as it must be restored before releasing the eye monitor
4. Position the eye monitor:
   - Horizontal - by default, the eye monitor position is near the middle of the eye. Move the required number of steps by issuing a sw_fw eyemon_move_horizontal command. Wait for ack
   - Vertical - set the required vertical position, by setting per_lane.RX_VREF_VALUE.vrefeo_value and per_lane.RX_VREF_VALUE.vrefee_value

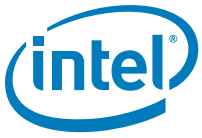
Note that bit 0 is ignored, therefore there are 256 effective steps.

Apply the change: per_lane.RX_SOURCE_SELECT.update_force_value = 1'b1.

5. Set the required data filter at per_lane.EYEMON_CTRL0.mask_select to either 3'h0: compare all, 3'h1: only after 1, or 3'h2: only after 0 (the later are useful for DFE checks)
6. Set the number of samples to check, by setting per_lane.EYEMON_CTRL1.symbol_count. Each symbol is 32 UI. Note that when using certain filters, 32*symbol_count does not indicate the number of compared bits
7. Set search type: per_lane.EYEMON_CTRL0.search_type = 2'b01
8. Enable the eyemon: per_lane.EYEMON_CTRL0.go = 1'b1
9. Wait for done: check per_lane.EYEMON_CTRL0.done == 1'b1
10. Disable the eyemon: per_lane.EYEMON_CTRL0.go = 1'b0.
11. Read the results:
    - Number of compared bits - read per_lane.EYEMON_CHECK_COUNTER.check_count
    - Number of error bits - read per_lane.EYEMON_ERROR_COUNTER.error_count
12. For more checks, repeat from Step 4 as required
13. When completed:
    - Move the eye monitor to its original horizontal position by issuing the sw_fw eyemon_move_horizontal command, as required. Do NOT wrap around to get back to position - the total number of steps moved left must be equal to the total number of steps moved right. Verify that the horizontal location (per_lane.EYEMON_ANA.pi_phase_monitor) is equal to what it originally was
    - Release the eyemon by issuing a sw_fw eyemon_release_control command. Wait for ACK

8.8.7 CIP Phy SW FW Mailboxes

Each cio phy port and each lane have a sw_fw_mailbox register used for various SW interactions.



The mailboxes are located at the first memory mapped offset of each section.

The most significant byte (sw_fw_mailbox[31:24]) holds the command and the rest of the mailbox (sw_fw_mailbox[23:0]) is used for arguments.

Unless otherwise stated, when FW completes a command, it clears the command field (sw_fw_mailbox[31:24]).

8.8.7.1 per port sw_fw_mailbox:

The table below lists the supported commands for the per_port.SW_FW_MAILBOX:

Command Name	Description	Command Encoding [31:24]	Arguments [23:0]
port_controller_halt	Halt the FW, for debug. This command is not cleared by FW. It is acknowledged by FW clearing of bit 0. Command field should be cleared by SW in order to release.		[0] - SW should set this bit when issueing the command. FW will clear it when halted

8.8.7.2 per lane sw_fw_mailbox:

The table below lists the supported commands for the per_lane.SW_FW_MAILBOX:

Command Name	Description	Command Encoding [31:24]	Arguments [23:0]
eyemon_request_control	Request control for the eyemon logic	0x02	
eyemon_release_control	Release the eyemon logic	0x03	
eyemon_move_horizontal	Move the eyemon horizontally	0x04	[8] - 0 Move left, 1 Move right [7:0] number of steps to move

9.0 Testability

9.1 JTAG Test Active Point (TAP)

JTAG Test Active Point (TAP)

Alpine-Ridge JTAG TAP has a Main Tap (mTAP) with 8 bit Instruction register (IR) and some glue logic to connect to Legacy TAP of 6 bit IR. By default (after Power up) the mTAP is connected to JTAG pads of the Alpine-Ridge device working with 8 bit IR.

Main TAP supports the following commands:

Public commands IEEE Std.1149.1 (used for BSDL testing):

BYPASS (11111111)

EXTEST (00001001)

SAMPLE (00000001)

PRELOAD (00000001)

IDCODE (00000010)

User defined commands:

MTAP DISABLE (00110000), Shift DR one bit value 1'b1.

This command can be used to connect Legacy TAP to Alpine-Ridge JTAG pins. Once this command is completed, Alpine Ridge JTAG is working in legacy mode with 6 bit IR, except public BSDL command.

The following procedure can be done by external JTAG agent to recognize Legacy Alpine-Ridge JTAG:

1. Apply MTAP DISABLE command.

2. Apply Legacy DEVID 6-bit command (010101) and Shift DR 16 bit value 0x0. Check received 16 bit data on TDO. If known 16-bit IDCODE recognized (Alpine-Ridge DP - 0x1578), the corresponding chip is recognized and legacy 6-bit JTAG TAP is available.

End of procedure.

In this mode 6 bit IR should be used.

MTAP_NETWORK (00010010) Shift DR 4 bit value 4'b0001

This command used to Access legacy JTAG TAP (6-bit) via TAP network. Once this command is completed, each JTAG instruction has 14 bits length, first 6 bits relates to Legacy TAP and last 8'bFF bypass mTAP, also Data Register need additional 1 bit shifting. This mode used by Tenlira tool.

In this mode 14 bit IR should be used.

9.2 Boundary-Scan Description Language (BSDL) file

Chip supports BSDL and appropriate bsdl file can be provided to customer.

9.3 XOR tree

XOR tree chain:

Activation of XOR testing by JTAG command: set instruction register to 6'b101010

Toggle XOR inputs and sample DPSNK0_HPD.

TDF file is available and can be provided to customer.

9.4 Thermal Junction 1mA Curve

In order to measure the Tj (Junction Temperature) a thermal diode is implemented in Alpine-Ridge DP. See Figure 79.

A DMM should be used in the setup shown in Figure 80. The DMM should be connected using the jumper and AB23/AC23 balls for 10.7x10.7 (Alpine-Ridge DP 4C).

Figure 79. Thermal diode implementation

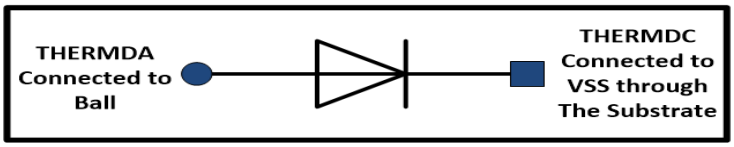
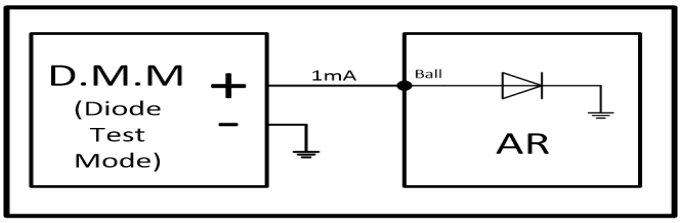
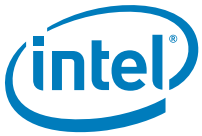


Figure 80. Tj Measurement Setup



10.0 Board Schematics

Please refer to the Reference Design documents that are part of this product collaterals.



Appendix A. External Connection Manager Guidelines

A.1. Sx Entry/ Exit Flow - Implementation Details

Registers relevant for Sx flow:

LC_SX_STATUS

See Table 34 for details.

LC_SX_CTRL

See Table 34 for details.

LC_SX_TIMERS

See Table 34 for details.

POC_MAILBOX (informative. Handled by LC)

[31:16] Reserved

[15] System state at power down: 0=S0, 1=Sx.

[14:12] State before Sx entry: 100 = downstream cio, 101 = upstream cio, 110 = interdomain cio, 010 = dpp, 000 = disconnected.

[11:9] Reserved

[8:0] Sx wake enables. Preserve the latest wake settings.

Connection Manager Responsibilities:

After Sending a Go2Sx Command through the PCIE2TBT Mailbox, CM should back-trace all switches within the domain from the leafs up to the HR (HR is last) and set LC_SX_CTRL[31] (other fields in this register should not be changed) in each of the LCs. CM should then wait for a Ok2Go2Sx approval from the TBT2PCIE Mailbox before proceeding with the Sx flow.

Upon every CIO Port plug event, after CIO enumeration of the plugged switch is complete, CM should set "plugged and configured" bit in respective LC_SX_CTRL[16]/[20] (depending on the port/lane) of both link ends (i.e. father and child switches). CM should also update "Port is upstream" for the upstream port. Upon every CIO Port unplug event, before CIO tunnels teardown of the un-plugged switch is complete, CM has to clear "plugged and configured" bit in respective LC_SX_CTRL[24]/[20] (depending on the port/lane) of both link ends (i.e. father and child switches), if accessible.

After starting the Sx flow, CM should not handle any plug/unplug events (until system is back to S0).

Interdomain considerations:

By default, a port entering Sx with an inter-domain link will be treated as a disconnected port, without any wake event. Alpine-Ridge DP will drive LSTX low in this case.

In order to allow an inter-domain link to enter Sx similar to a regular TBT link, SW should first disable the default functionality by clearing CHICKEN_BITS[5]. SW should also make sure not to enable any lsrx toggle related wake event on the inter-domain port, in order to avoid false wake of the topology.

The non sleeping partner must keep the interdomain plugged and configured bits set (despite the unplug events).

In order to wake the interdomain link, the non sleeping partner should simulate an unplug using SW_FW_MAILBOX_IN[6] (sw_force_lstx_low).

Upon Sx exit, if the interdomain partner is still sleeping, CM must reconfigure the interdomain plugged and configured bits (despite that there won't be any plug events).

A.1.1. A.3.4 Flash read through LC/IECS

Alpine-Ridge DP Flash read can be done through dedicated LC registers: LC_FLASH_ACCESS_DATA, LC_FLASH_ACCESS_CTRL. These registers are accessible either through target as two 32b registers, or through IECS as a single 64b register at offset 0x11.

Flash accesses through these registers are done in DWs (32b), to DW aligned addresses. To Read a DW, SW should set LC_FLASH_ACCESS_CTRL/byte_address, start1_done0. When the start1_done0 bit is cleared (by LC FW), read data is ready at LC_FLASH_ACCESS_DATA. SW must verify that the read_error indication is clear.

Flash access also supports up to 64B read operations, by setting LC_FLASH_ACCESS_CTRL/ data_register_select to 1 and LC_FLASH_ACCESS_CTRL/access_length to the required read length. MSG_OUT_RDATA is used as the read data buffer in this case. The rest of the read flow is as described above. Note that it is SW responsibility to ensure the accessed Flash supports such read bursts.

A.2. Accessing IECS Cmd/Data registers from SW

Several general purpose registers were assigned for communication between CM and LC:

SW_FW_MAILBOX_IN, SW_FW_MAILBOX_DATA_IN0..3 - are used for commands/data from CM to LC.

SW_FW_MAILBOX_OUT, SW_FW_MAILBOX_DATA_OUT0..3 - are used for commands/data from LC to CM.

Sending IECS commands from CM should be done through the SW_FW_MAILBOX, and not through direct access to the IECS register. The IECS register should be used only for UART access.

SW should write the IECS command to SW_FW_MAILBOX_DATA_IN0 and related data (if applicable) to SW_FW_MAILBOX_DATA_IN1..3. Then it should set SW_FW_MAILBOX_IN[0]. LC will clear this bit to indicate it received the command. Output data (if applicable) will be valid at SW_FW_MAILBOX_DATA_OUT0..3, once SW_FW_MAILBOX_DATA_IN0 (the command) is cleared.

A.3. Supported IECS Commands

The IECS Commands (4CC encoded) supported by Alpine-Ridge DP are listed in Table 429. Unless otherwise stated, the commands are supported though both IECS or SW_FW_MAILBOX.

Table 429. IECS Commands

Command	Description	Data
'Lnk0'	disable both lanes	NA
'Lnk1'	enable lane 0, disable lane 1	NA
'Lnk2'	enable lane 1, disable lane 0	NA
'Lnk3'	enable both lanes	NA
'I2CW'	I2C master write. Write data must be ready before the command is issued	MSG_OUT_RDATA0..15 = write data (first byte transmitted is MSG_OUT_RDATA0[7:0]) SW_FW_MAILBOX_DATA_IN1/IECS_DATA[6:0] = i2c address SW_FW_MAILBOX_DATA_IN1/IECS_DATA[7] = no stop (to allow repeated start transactions). SW_FW_MAILBOX_DATA_IN1/IECS_DATA[15:8] = write length (max 64B) 1 – transaction failed/nack'ed. 2 – transaction completed successfully
'I2CR'	I2C master read	SW_FW_MAILBOX_DATA_IN1/IECS_DATA[6:0] = i2c address SW_FW_MAILBOX_DATA_IN1/IECS_DATA[15:8] = read length (max 64B) MSG_OUT_RDATA = read data (first byte received is MSG_OUT_RDATA0[7:0]) 1 – transaction failed/nack'ed. 2 – transaction completed successfully
'I2CF'	I2C frequency change	SW_FW_MAILBOX_DATA_IN1/IECS_DATA[15:0] = value to store in I2C_PRER register
'PPSW'	Write to Port Power Switch	MSG_OUT_RDATA0..15 = write data (first byte transmitted is MSG_OUT_RDATA0[7:0]) SW_FW_MAILBOX_DATA_IN1/IECS_DATA[15:8] = write length (max 64B) SW_FW_MAILBOX_DATA_IN1/IECS_DATA[23:16] = PPS register offset Result in SW_FW_MAILBOX_DATA_OUT0/IECS_DATA: [7:0] return value: 1 - transaction failed/nack'ed. 2 - transaction completed successfully
'PPSR'	Read from Port Power Switch	SW_FW_MAILBOX_DATA_IN1/IECS_DATA[15:8] = read length (max 64B) SW_FW_MAILBOX_DATA_IN1/IECS_DATA[23:16] = PPS register offset MSG_OUT_RDATA0..15 = returns the read data (first byte transmitted is MSG_OUT_RDATA0[7:0]) Result in SW_FW_MAILBOX_DATA_OUT0/IECS_DATA: [7:0] return value: 1 - transaction failed/nack'ed. 2 - transaction completed successfully [15:8] register true length (as reported by the PPS)

A.4. Supported IECS registers

The supported IECS registers are listed in Table 430.

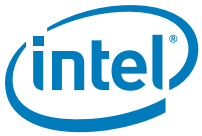


Table 430. Supported IECS Registers

IECS offset	Name	Length (Bytes)	Access (from IECS)	Description	Target offset (within each LC, Table 35)
0	VID	4	RO	As defined in TBT spec	0x0
1	DID	4	RO	As defined in TBT spec	0x1
2	ProtoVer	4	RO	As defined in TBT spec	0x2
3	Mode	4	RO	As defined in TBT spec	0x3
4	Type	4	RO	As defined in TBT spec	0x4
5	UID	16	RO	As defined in TBT spec	0x5-0x8
6	oUID	16	RW	As defined in TBT spec	0x9-0xc
7	Reserved	1	RO	As defined in TBT spec	0x8c[7:0]
8	Cmd	4	RW	As defined in TBT spec	0xe
9	Data	16	RW	As defined in TBT spec	0xa1-0xa4
10	HVREq	1	RO	As defined in TBT spec	0x62[7:0]
11	DescriptorHead	2	RO	As defined in TBT spec	0x11[15:0]
12	LinkEnable	2	RO	As defined in TBT spec	0x8d[15:0]
13	IECS_TXFEE	4	RO	As defined in TBT spec	0x8e
14	Reserved	4	RW	As defined in TBT spec	0x90
15	Version	4	RO	As defined in TBT spec	0x15
16	TargetAccess	8	RW	Vendor specific - Refer to registers LC_TARGET_ACCESS_DATA, LC_TARGET_ACCESS_CTRL for details.	0x9f-0xa0
17	FlashAccess	8	RW	Vendor specific - Refer to A.3.4 FLASH Burning for details.	0x9b-0x9c
18	MSG_OUT_RDATA	64	RW	Vendor specific - General purpose buffer (used by I2C commands, FLASH Access). Also used by the MSG_OUT mechanism	0x74-0x83

A.5. Useful Internal FW registers, for debug purposes

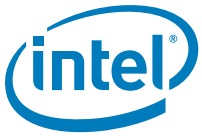
The following internal registers are available for LC/POC/IECS debug. The offsets are likely to change in future projects. Use for debug purpose only.

Table 431. Internal FW registers

Name	Offset	Bits	description
DEBUG_IECS_0	0x1de / 0x2de (PA / PB)	7..0	Iecs handshake state: 0x40=INIT 0x41=READ_O_VENDOR_ID 0x42=WRITE_oUUID 0x43=READ_O_HV_REQ 0x44=READ_CM_HV_CAP 0x45=WAIT_FOR_LT_RISE 0x46=READ_O_LANE_EN 0x4f=FINALIZE
DEBUG_O_VENDOR_ID	0x1da / 0x2da	31..0	Partner's vendor ID (iecs 0)

Table 431. Internal FW registers

Name	Offset	Bits	description
DEBUG_O_LANE_EN	0x1db / 0x2db	7..0 15..8	Partner's lane_en status Partner's lane_en available (iecs 12)
DEBUG_O_HV	0x1dc / 0x2dc	7..0 31..8	Partner's hv request Cable hv capability (iecs 10)
DEBUG_O_LC_TYPE	0x1dd / 0x2dd	31..0	Partner's LC type (EM/ECM)
DEBUG_POC_CSR_LOW	0x1e9 / 0x2e9	31..0	POC_CSR_IN_LOW at last power on
DEBUG_POC_CSR_HIGH	0x1ea / 0x2ea	31..0	POC_CSR_IN_HIGH at last power on
DEBUG_POC_MAILBOX	0x1eb / 0x2eb	31..0	POC_CSR_MAILBOX at last power on
DEBUG_POC_CSR_COMMON	0x1e8 / 0x2e8	31..0	POC_CSR_COMMON at last power on



Appendix B. HDP Configuration Procedures

B.1. DP IN Configuration from Flash Memory

DP tunnel setup requires configuring GPU SSC parameter into DP OUT TMU SSC_PPM_Shift register. As this parameter is GPU dependant, it is bound to DP IN and reported in VSEC_DP_CS_50. CM software is expected to read it, and if GPU is present (VSEC_DP_CS_50. GPU_present), configure DP OUT accordingly. EE2TAR should initialize VSEC_DP_CS_50 depending on system build.

B.2. Forcing HPD high on PA/PB for DP debug

The following flow should be used in order to force hpd high in PA/PB:

1 Connect dp cable, see monitor.

2 Set the relevant IO CTRL REG bits (refer to Table 22). To avoid glitches, first write the required value and then write the required sustain bits.

3 Disconnect the display, connect the test equipment.

When done, in order to restore the system to normal state, either power cycle or clear the relevant IO CTRL REG sustain bits. Do not change the data bits.

B.3. Controlling VS/PE for HDP Tx

The transmit control for all 3 DP transmitters is the same. It is controlled through 3 registers, TX_SW_INV, DP_TX_POST & TX_SW_PRE. In order to fully understand the mechanism and those registers effect, refer to section Transmitter Equalization (TXFFE) for full description. The default (and recommended) values of the above registers are located in the NVM, at the DP_OUT Region. The DP OUT controller uses those NVM settings according to mode of operation and VSPE requested by the monitor

Table 432. The DP_OUT Region is part of the DP_OUT uCode and starts at offset 0x22 from the start of the uCode section. The exact location is referred by a pointer in the digital section HDP_OUT Region fields. **DP OUT Region structure and TXFEE recommended settings for DP**

Mode	VS	PE	Offset	TX_SW_INV	TX_SW_PRE	TX_SW_POST
HDMI			0x0	0	0	0
DP	0	0	0x3	7	0	0
DP	0	1	0x6	4	0	3
DP	0	2	0x9	1	0	6
DP	1	0	0xC	5	0	0
DP	1	1	0xF	3	0	2
DP	1	2	0x12	0	0	5
DP	2	0	0x15	3	0	0
DP	2	1	0x18	0	0	3

B.4. DP Transmitter/Receiver Testing Procedure

Alpine-Ridge DP supplies an ability to transmit various DP patterns from its DP Sources and count mismatches/errors of these patterns on its DP Sink side.

The patterns that can be transmitted are:

- TPS1/TPS2/TPS3
- PRBS7
- Symbol error rate measurement pattern
- Eye pattern. (configurable)
- 80bit configurable pattern

The patterns that can be checked for errors in Alpine-Ridge DP Sink are:

- PRBS7
  - — Counts either symbol or bit errors
- Eye pattern
  - — Configurable
  - — Counts either symbol or bit errors
  - — Requires preceding link training

  Symbol error counter of any stream
  - — Requires preceding link training

Checking the DP Sources could be accomplished in 2 ways:

1. Stand alone:
   - — Set up the transmitter to generate the desired frequency with no reference clock to track from receiver. Those steps are described in Table 433.
   - — Activate the desired test pattern by the Source. Those steps are described in Table 434.
2. Redriver:
   - — Activate the system by plugging a monitor.
   - — Activate the desired test pattern by the Source. Those steps are described in Table 434.

Checking the DP Sinks for Integrity of some patterns, link training (only TPS2/TPS3 stage) should be preceded in this sink. The steps needed to configure the Sink are described in Table 435.

Table 433. DP Tx Standalone configuration

Register space	Register Name	Write Value	Description
Raise SRC HPD			
Device configuration space	Address 0x49 bits [7:6] PA: Address 0x3D bits [31:30] PB: Address 0x49 bits [5:4]	11b	SRC HPD
Choose Phy operation mode			
Misc2	"HDP_CTRL_2" on page 460	0x00	Clear leg_phy_en

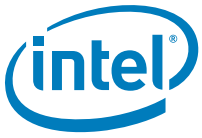


Table 433. DP Tx Standalone configuration (Continued)

Register space	Register Name	Write Value	Description
Force Tx Termination			
DP 8051 (Src)	"CM_TX_RESTUNE_SET - Tx termination resistor settings in bypass mode" on page 510	0x2	
DP 8051 (Src)	"CM_MISC_CTRL- Misc. Phy Common control" on page 510	0x1	
Enable Tx Phy			
DP 8051 (Src)	"CM_DPPLL_CTRL - PLL Misc Control" on page 512	0x0	
Wait 5u Sec Set Tx VSPE			
DP 8051 (Src)	"TX_SW_INV - Lane 0/1/2/3 TX CID swing control" on page 508	0x3	
DP 8051 (Src)	"TX_SW_PRE - Lane 0/1/2/3 TX 1st pre-cursor swing control" on page 508	0x0	
DP 8051 (Src)	"TX_SW_POST - Lane 0/1/2/3 TX 1st post-cursor swing control" on page 508	0x0	
Jumpstart the PLL			
DP 8051 (Src)	"Allow_RTL_DPPLL_CTRL - Switch control over PLL interface" on page 510	0x0	
DP 8051 (Src)	"CM_DPPLL_CTRL - PLL Misc Control" on page 512	0x4	
DP 8051 (Src)	"CM_DPPLL_LOOP_CTRL - PLL third loop control" on page 512	0x0	
DP 8051 (Src)	"CM_DPPLL_CTRL - PLL Misc Control" on page 512	0x0	
Configure PLL params			
DP 8051 (Src)	"CM_DPPLL_CP_RES_SEL - PLL Resistor Select Control" on page 512	0x0A	
Per Speed Control			
DP 8051 (Src)	"Allow_RTL_DPPLL_CTRL - Switch control over PLL interface" on page 510	DP1.62 0x42 DP 2.7 0x58 DP 5.4 0x58	
DP 8051 (Src)	"CM_DPPLL_POSTDIVSEL - PLL post divider settings" on page 512	DP1.62 0x03 DP 2.7 0x00 DP 5.4 0x00	
DP 8051 (Src)	"CM_DPPLL_F_L - PLL fractional multiplication factor, low" on page 512	DP1.62 0x9A DP 2.7 0x00 DP 5.4 0x00	

Table 433. DP Tx Standalone configuration (Continued)

Register space	Register Name	Write Value	Description
DP 8051 (Src)	"CM_DPPLL_F_M - PLL fractional multiplication factor, med" on page 512	DP1.62 0x99 DP 2.7 0x00 DP 5.4 0x00	
DP 8051 (Src)	"CM_DPPLL_F_H - PLL fractional multiplication factor, high" on page 512	DP1.62 0x01 DP 2.7 0x00 DP 5.4 0x00	
DP 8051 (Src)	"CM_DPPLL_RST_B - PLL reset" on page 512	0x1	
DP 8051 (Src)	"CM_DPPLL_CTRL - PLL Misc Control" on page 512	0x4	
DP 8051 (Src)	"CM_DPPLL_CTRL - PLL Misc Control" on page 512	0x2	
DP 8051 (Src)	"CM_DPPLL_CTRL - PLL Misc Control" on page 512	0x0	
At this stage "CM_DPPLL_CTRL - PLL Misc Control" bit 7 should be high (CM_PLL_LOCK) Wait 1u Sec Set D10.2			
Misc	"Register 0h -- LS_RST -- ls_rst setting/resetting. Polarity: positive" on page 496	0x00	
Wait 1u Sec Enable Tx			
DP 8051 (Src)	"Swizzle_1020_EN - Swizzle data towards Phy" on page 510	0x0F	
Misc2	"CAR CTRL" on page 461	0x40	Clock ungating
DP 8051 (Src)	"DP_SPEED - Misc. Phy Common control 2" on page 510	0xF	
DP 8051 (Src)	"TX_SYNC_CTRL- Tx Sync control" on page 510	0x0F	
DP 8051 (Src)	"TX_SYNC_CTRL- Tx Sync control" on page 510	0xFF	

Table 433. DP Tx Standalone configuration (Continued)

Register space	Register Name	Write Value	Description

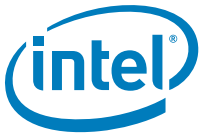
Table 434. DP Tx D10.2/Eye pattern/PRBS/80bit configuration

For Eye pattern transmissio			
DP 8051 (Src)	"TST_PTTRN_SR_1" on page 393	0x3C	Set the 2nd symbol of SR sequence to be K28.1
DP 8051 (Src)	"TST_PTTRN_SR_2" on page 393	0x3C	Set the 3rd symbol of SR sequence to be K28.1
DP 8051 (Src)	"TST_PTTRN_BS_RATIO_0" on page 394	0xFC	Set Eye pattern length to be 252
DP 8051 (Src)	"TST_PTTRN_BS_RATIO_1" on page 394	0x0	
DP 8051 (Src)	"TST_PTTRN_SR_RATIO_0" on page 394	0x0	Send only SR sequences (no BS sequences)
DP 8051 (Src)	"TST_PTTRN_SR_RATIO_1" on page 394	0x0	
DP 8051 (Src)	"TST_PTTRN_CTRL_2" on page 393	0x3	SR sequence length is 4 symbols + count bit errors
DP 8051 (Src)	"TST_PTTRN_CTRL_0" on page 467	(1 << lane_count) – 1	Send Eye pattern on all of the activated lanes.
For PRBS transmission			
DP 8051 (Src)	"TST_PTTRN_CTRL_0" on page 467	((1 << lane_count) – 1)<<4	Send PRBS pattern on all of the activated lanes.
For 80bit pattern transmission			
DP 8051 (Src)	"Register 80h -- SHIFT_PATTERN_IN0" on page 507	80bit_pattern	Configure 10 registers of 80bit pattern
DP 8051 (Src)	"TST_PTTRN_CTRL_1" on page 392	(1 << lane_count) – 1	Send 80bit pattern on all of the activated lanes.

Different lanes can be configured to transmit different test patterns - using TST_PTTRN_CTRL_0 and TST_PTTRN_CTRL_1.

Table 435. DP Rx Eye pattern/PRBS Startup

Space	Register Name	DP 5.4	DP 2.7	DP 1.62	Description
MISC2	HDP_CTRL_0	80	80	80	Reset
CMN	DP_RATE	2	1	0	
AN_IF	CDR0_PD_CNTRL	10	80	0	
MISC	LS_RST	1	1	1	
CMN	SIPO_RST_N	0	0	0	
CMN	RX_RST_N	0	0	0	
CMN	RX_EYEMON_CTRL	0	0	0	
CMN	RX_EN	0	0	0	
MISC2	HDP_CTRL_0	80	80	80	Prepare datapath
CMN	RX_SIPO_10BIT	0	f	f	
CMN	USE_810	1	0	0	
CMN	RX_EYEMON_CTRL	80	80	80	
LANE	EYEMON_EVND_MSK_SEL0	0	1	1	
CMN	RX_EYEMON_CTRL	0	0	0	
CMN	REARNG_EVENODD_RX_DATA	0	55	55	
CMN	REARNG_EVENODD_EYEDATA	0	55	55	
CMN	EYEDATA_SWIZZLE_EN	f0	f0	f0	
CMN	DP_RATE	2	1	0	
LANE	RX_CDR_ICP_SEL0/1/2/3	7	7	3	Set Phy rate
LANE	RX_CDR_RESLP_SEL0/1/2/3	2	4	8	
LANE	RX_PLL_ICP_SEL0/1/2/3	7	7	f	
LANE	RX_PLL_RESLP_SEL0/1/2/3	2	2	1	



Space	Register Name	DP 5.4	DP 2.7	DP 1.62	Description
CMN	RX_EN	f	f	f	Phy out of reset (bit per lane)
CMN	RX_EYEMON_CTRL	f	f	f	
CMN	RX_RST_N	f	f	f	
CMN	SIPO_RST_N	f	f	f	
CMN	RX_EN	f	f	f	PI calibration start
CMN	RX_EYEMON_CTRL	80	80	80	
LANE	EYEMON_MASK_SEL0	0	0	0	
CMN	RX_EYEMON_CTRL	0	0	0	
CMN	RESET_PI_FSMS	ff	ff	ff	
CMN	RESET_PI_FSMS	0	0	0	
CMN	RTL_IN_CTRL_PI0_CTLE1	0	0	0	
CMN	ALLOW_RTL_CTLE_CTRL	0	0	0	
CMN	RX_PLL_MODE_CTRL0/1/2/3	ff	ff	ff	
CMN	PI_PD_EN	f	f	f	
CMN	FINE_SCAN_WIDTH	1e	1e	1e	
CMN	PI_CAL_CTRL	2f	2f	2f	
CMN	PI_CAL_CTRL	20	20	20	
CMN	PI_CAL_EN	f	f	f	
while ((PHY_DIG_CMN[PI_CAL_DONE_ADR] & 0xf) != (PHY_DIG_CMN[PI_PD_EN] & 0xf));					Wait for PI calibration to end

Space	Register Name	DP 5.4	DP 2.7	DP 1.62	Description
CMN	PI_CAL_EN	0	0	0	CTLE selection
CMN	PI_PD_EN	0	0	0	
CMN	CACHE_CTRL1	f	f	f	
CMN	RX_PLL_MODE_CTRL0/1/2/3	f	f	f	
CMN	RTL_IN_CTRL_PI0_CTLE1	f	f	f	
CMN	ALLOW_RTL_CTLE_CTRL	f	f	f	
CMN	SELECT_CTLE	f	f	f	
tmp = ((~PHY_DIG_CMN[RX_EN]) & 0xf0)>>4; while ((PHY_DIG_CMN[CTLE_SELECTED] & tmp) != tmp)					Wait for CTLE to be selected
CMN	RX_EYEMON_CTRL	0	0	0	
MISC2	HDP_CTRL2	0	0	0	
MISC2	RX_STATE	3	2	2	
MISC2	CAR_CONTROL	0	0	0	
MISC	LS_RST	0	0	0	

Table 436. DP Rx Eye pattern/PRBS configuration

Register space	Register Name	Write Value	Description
Wait a couple of msec, or until PHY_CONFIG_REG6.SYMB_LOCKED is set for all of the active lanes in order to verify that the symbol-lock is achieved			
DP 8051 (Snk)	"HDP_CTRL_0" on page 382	0x4	Set DP_STATE to Active
	"TST_PTTRN_SR_1" on page 393	0x80	Enable counter-B to count the errors
Start sending the test pattern to this Sink at this stage			
To **check** Eye pattern			
DP 8051 (Snk)	"TST_PTTRN_SR_1" on page 393	0x3C	Set the 2nd symbol of SR sequence to be K28.1
DP 8051 (Snk)	"TST_PTTRN_SR_2" on page 393	0x3C	Set the 3rd symbol of SR sequence to be K28.1
DP 8051 (Snk)	"TST_PTTRN_BS_RATIO_0" on page 394	0xFC	Set Eye pattern length to be 252
DP 8051 (Snk)	"TST_PTTRN_BS_RATIO_1" on page 394	0x0	

Table 436. DP Rx Eye pattern/PRBS configuration

Register space	Register Name	Write Value	Description
DP 8051 (Snk)	"TST_PTTRN_SR_RATIO_0" on page 394	0x0	Send only SR sequences (no BS sequences)
DP 8051 (Snk)	"TST_PTTRN_SR_RATIO_1" on page 394	0x0	
DP 8051 (Snk)	"TST_PTTRN_CTRL_2" on page 393	0x3	SR sequence length is 4 symbols + count bit errors
DP 8051 (Snk)	"TST_PTTRN_CTRL_0" on page 392	(1 << lane_count) – 1	Enable Eye pattern check on the activated lanes
To check PRBS			
DP 8051 (Snk)	"TST_PTTRN_CTRL_0" on page 392	((1 << lane_count) – 1)<<4	Enable PRBS pattern check on the activated lanes
Start sending Eye/PRBS pattern			
DP 8051 (Snk)	"ERR_LOCK_COUNT_B" on page 432	0xF	Clear the error counter
After a while, verify TST_PTTRN_STATUS . TST_PTTRN_LOCK is set for the activated lanes			
DP 8051 (Snk)	"ERR_LOCK_COUNT_B" on page 432	0xF	Sample the error counter-B
Read ERR_COUNT_STD_(0-3)B_(LO,MD,HI)			

Different lanes can be configured to check different test patterns - using "TST_PTTRN_CTRL_0" on page 392.

The counter can be configured to count in resolution of the bit errors - using "TST_PTTRN_CTRL_2" on page 393.

DP Compliance Spec. defines 3 different Eye patterns -verify that the correct one is configured in "TST_PTTRN_SR_1" on page 393/"TST_PTTRN_SR_2" on page 393.

In order to count 8b10b errors (for example during normal operation):

Register space	Register Name	Write Value	Description
DP 8051 (Snk)	"ERR_LOCK_COUNT_B" on page 432	0xF	Clear the error counter
DP 8051 (Snk)	"ERR_LOCK_COUNT_B" on page 432	0xF	Sample the error counter-B
Read "ERR_COUNT_STD_0B_LO" on page 434			

B.5. DPCD Handling

See Table 437 for DPCD registers implemented in DisplayPort Sinks.

Table 437. DPCD registers

Address	Configuration Register	R/W over AUX	Notes
0000h	DPCD_REV	RO	Pass through, but the reply is Overwritten not to surpass 1.1/1.2 in tunneling/ redriver mode (respectively)
00001h	MAX_LINK_RATE	RO	Pass through, but the reply is overwritten not to surpass 2.7Gbps/5.4Gbps in tunneling/redriver mode (respectively).Reads to this register are passed through to the DisplayPort Sink until training complete notification is received from the DisplayPort OUT. If DisplayPort OUT obtained lower link rate or failed to obtain the link, this register starts being local in order to advertise lower capability and the link is retrained.
00002h	MAX_LANE_COUNT	RO	Pass through, but the reply of TPS3_SUPPORTED field is overwritten to 0, besides redriver mode.
0000Eh	TRAINING_AUX_RD_INTERVAL	RO	For DisplayPort IN it is configurable from flash. DisplayPort OUT reads this DPCD from DisplayPort Sink after HPD plug and uses it during the link training.
00020h	FAUX_CAP	RO	Pass through, but bit 0 is overwritten to 0.
00021h	MSTM_CAP	RO	Pass through, but bit 0 is overwritten to 0 in tunneling mode.
00054h-00057h	RX_GTC_VALUE	RO	Pass through, but the value is updated by the delay through TBT chip
00100h	LINK_BW_SET	R/W	Accesses to this register are always terminated at the DisplayPort IN.
00101h	LANE_COUNT_SET	R/W	Accesses to this register are always terminated at the DisplayPort IN.
00102h	TRAINING_PATTERN_SET	R/W	Accesses to this register are always terminated at the DisplayPort IN.
00103h	TRAINING_LANE0_SET	R/W	Accesses to this register are always terminated at the DisplayPort IN.
00104h	TRAINING_LANE1_SET	R/W	Accesses to this register are always terminated at the DisplayPort IN.
00105h	TRAINING_LANE2_SET	R/W	Accesses to this register are always terminated at the DisplayPort IN.
00106h	TRAINING_LANE3_SET	R/W	Accesses to this register are always terminated at the DisplayPort IN.
00107h	DOWNSPREAD_CTRL	R/W	Accesses to this register are always terminated at the DisplayPort IN.
00108h	MAIN_LINK_CHANNEL_CODING_SET	R/W	Accesses to this register are always terminated at the DisplayPort IN.
0010Bh-0010Eh	LINK_QUAL_LANEx_SET	R/W	Pass through, but the value is influencing the configuration in DisplayPort IN and DisplayPort OUT.
0010Fh-00110h	TRAINING_LANEx_y_SET2	R/W	Accesses to this register are always terminated at the DisplayPort IN.
00154h-00157h	TX_GTC_VALUE	WO	Pass through, but the value is updated by the delay through TBT chip

Table 437. DPCD registers

Address	Configuration Register	R/W over AUX	Notes
00202h/ 0200Ch	LANE0_1_STATUS	RO	Accesses to this register are always terminated at the DisplayPort IN.
00203h/ 0200Dh	LANE2_3_STATUS	RO	Accesses to this register are always terminated at the DisplayPort IN.
00204h/ 0200Eh	LANE_ALIGN_STATUS_UPDATED	RO	Accesses to this register are always terminated at the DisplayPort IN.
00206h	ADJUST_REQUEST_LANE0_1	RO	Accesses to this register are always terminated at the DisplayPort IN.
00207h	ADJUST_REQUEST_LANE2_3	RO	Accesses to this register are always terminated at the DisplayPort IN.
0020Ch	ADJUST_REQUEST_POST_CURSOR2	RO	Accesses to this register are always terminated at the DisplayPort IN replying 0.
00210h-00211h	SYMBOL_ERROR_COUNT_LANE0	RO	This register is configurable (using implementation-defined mechanisms) as pass through to DisplayPort Sink or terminated locally at the DisplayPort IN.
00212h-00213h	SYMBOL_ERROR_COUNT_LANE0	RO	This register is configurable (using implementation-defined mechanisms) as pass through to DisplayPort Sink or terminated locally at the DisplayPort IN.
00214h-00215h	SYMBOL_ERROR_COUNT_LANE0	RO	This register is configurable (using implementation-defined mechanisms) as pass through to DisplayPort Sink or terminated locally at the DisplayPort IN.
00216h-00217h	SYMBOL_ERROR_COUNT_LANE0	RO	This register is configurable (using implementation-defined mechanisms) as pass through to DisplayPort Sink or terminated locally at the DisplayPort IN.
0024Ah-0024Bh	HBR2_COMPLIANCE_SCRAMBLER_RESET	RO	Pass through, but the replied value is influencing the configuration in DisplayPort OUT.
00250h – 00259h	TEST_80BIT_CUSTOM_PATTERN	RO	Pass through, but the replied value is influencing the configuration in DisplayPort OUT.
0600h	SET_POWER	R/W	Accesses to this register are always terminated at the DisplayPort IN. All Write transactions are mirrored by DisplayPort OUT. Also, Whenever DisplayPort OUT initiates training, it first initiates a Write transaction, setting the DisplayPort Sink to D0. When DisplayPort IN is in D0 state, a Read transaction will cause a Write transaction by DisplayPort OUT, setting the DisplayPort Sink to D0.

B.6. DP tunneling

Introducing DP1.2 and 2x10 TBT link requires making some additions to the existing DP tunnel establishment.

DP_IN and DP_OUT have to know the capabilities of each other in order to avoid incompatibility, e.g. DP_IN that supports 5.4GHz and MST should prevent activation of these features in the system if it is paired with a legacy DP_OUT that doesn't support these features. The exchange of the capabilities between DP_IN and DP_OUT should be performed by the Connection Manager.

Having 20Gbps TBT link allows driving more than one DP1.1 stream through such a link. Knowing the status of the existing DP tunnels and the ability to configure DP capabilities allow Connection Manager to better control TBT resource allocation.

The flow:

- Monitor connection ' HPD assertion
- After de-bouncing of 100ms DP_OUT reads the monitor capabilities (DPCD Rev, link-rate, lane-count, enhanced framing and TPS3 support) and updates its DP_LOCAL_CAP. (DP_LOCAL_CAP reflects the minimal values between its eeprom/flash and the monitor capabilities)
- Plug event is triggered towards CM
- CM exchanges the capabilities of DP_IN and DP_OUT by copying DP_LOCAL_CAP of DP_IN/ DP_OUT to DP_REMOTE_CAP of DP_OUT/DP_IN (respectively):
  - If needed, CM can downgrade the read value of DP_OUT(DP_LOCAL_CAP) before writing it to DP_IN(DP_REMOTE_CAP), e.g. in order to prevent overbooking of TBT link resources
- Continue with the tunnel building

Note:

- The only field in DP_REMOTE_CAP that interests DP_OUT is "Remote DP Capability ID", i.e. DP Capability ID of DP_IN
- "DP Capability ID" should be copied by CM as is, without changing it
- DP_REMOTE_CAP is zeroed upon aux_enable clearing (i.e. parking the capabilities of its remote DP partner in the legacy mode)
- Without making this exchange DP adapters will work in the legacy mode, i.e. DP_IN won't advertise to GPU capabilities higher than DP1.1
- Reading DP_LOCAL_CAP from a legacy device will return value of 0, that will cause the new adapter to realize that it has a legacy DP remote partner.
- CM can check the status of the existing DP tunnel in DP_STATUS register of the new adapter

DP tunneling